User Manual

APM32F107xBxC

APM32F105x8xBxC

Arm® Cortex® -M3 core-based 32-bit MCU

Version: V0.3(The current manual is draft and official version will be released in April)

Contents

1 Introduction and Document Description Rules

1.1 Introduction

This *User Manual* provides application developers with all the information about how to use MCU (micro-controller) system architecture, memory and peripherals.

For information about Arm® Cortex®-M3 core, please refer to *Arm® Cortex®-M3 Technical Reference Manual*; please refer to the corresponding datasheet for detailed data such as model information, dimension and electrical characteristics of the device; for all MCU series models, please refer to the corresponding data manual for memory mapping, peripheral existence and their number.

It is hereby declared that Geehy Semiconductor Co., Ltd., hereinafter refer to as "Geehy".

1.2 Document Description Rules

1.2.1 "Register Functional Description" Rules

（1） Control (CTRL) registers are all "set 1 and clear 0 by software", unless otherwise specified.

（2） The control registers are usually followed by verb abbreviations to make a distinction. The verbs can be: EN-Enable, CFG-Configure, D-Disable, SET-Setup and SEL-Select

（3） The state register abbreviation is usually followed by FLG to make a difference.

（4） The value and data registers usually include V, VALUE, D and DATA, which are not followed by verbs, such as: xxPSC and CNT.

1.2.2 Full Name and Abbreviation Description of Terms

Table 1 Abbreviation and Description of R/W Modes

R/W mode	Description	Abbreviation
read/write	Software can read and write this bit.	R/W
read-only	Software can only read this bit.	R
write-only	Software can only write this bit, and after reading this bit, the reset value will be returned.	W
read/clear	The software can read this bit and clear it by writing 1. Writing 0 has no effect on this bit.	RC_W1
read/clear	The software can read this bit and clear it by writing 0. Writing 1 has no effect on this bit.	RC_W0

R/W mode	Description	Abbreviation
read/clear by read	The software can read this bit and reading this bit will automatically clear it to 0, and writing this bit is invalid.	RC_R
read/set	The software can read and set this bit, and writing 0 has no effect on this bit.	R/S
read-only write trigger	The software can read this bit and writing 0 or 1 can trigger an event but has no effect on the value of this bit.	RT_W
toggle	The software can flip this bit only by writing 1 and writing 0 has no effect on this bit.	T

Table 2 Functional Description and Full Name and Abbreviation of Terms of Commonly Used Registers

Full name in English	English abbreviation
Enable	EN
Disable	D
Clear	CLR
Select	SEL
Configure	CFG
Contrl	CTRL
Controller	C
Reset	RST
Stop	STOP
Set	SET
Load	LD
Calibration	CAL
Initialize	INIT
Error	ERR
Status	STS
Ready	RDY
Software	SW
Hardware	HW
Source	SRC
System	SYS
Peripheral	PER
Address	ADDR
Direction	DIR

Full name in English	English abbreviation
Clock	CLK
Input	I
Output	O
Interrupt	INT
Data	DATA
Size	SIZE
Divider	DIV
Prescaler	PSC
Multiplier	MUL
Period	PRD

Table 3 Full Name and Abbreviation of Modules

Full name in English	English abbreviation
External Memory Controller	EMMC
Static Memory Controller	SMC
Dynamic Memory Controller	DMC
Reset and Clock Management Unit	RCM
Power Management Unit	PMU
Backup Register	BAKPR
Nested Vector Interrupt Controller	NVIC
External Interrupt /Event Controller	EINT
Direct Memory Access	DMA
Debug MCU	DBG MCU
General-Purpose Input Output Pin	GPIO
Alternate Function Input Output Pin	AFIO
Timer	TMR
Watchdog Timer	WDT
Independent Watchdog Timer	IWDT
Windows Watchdog Timer	WWDT
Real-Time Clock	RTC
Universal Synchronous Asynchronous Receiver Transmitter	USART
Inter-Integrated Circuit Interface	I2C
Serial Peripheral Interface	SPI

Full name in English	English abbreviation
Inter-IC Sound Interface	I2S
Quad Serial Peripheral Interface	QSPI
Controller Area Network	CAN
Secure Digital Input and Output	SDIO
Universal Serial Bus Full-Speed Device	USBD
Analog-to-Digital Converter	ADC
Digital-to-Analog Converter	DAC
Cyclic Redundancy Check Calculation Unit	CRC
Float Point Unit	FPU

2 System Architecture

2.1 Full Name and Abbreviation Description of Terms

Table 4 Full Name and Abbreviation Description of Terms

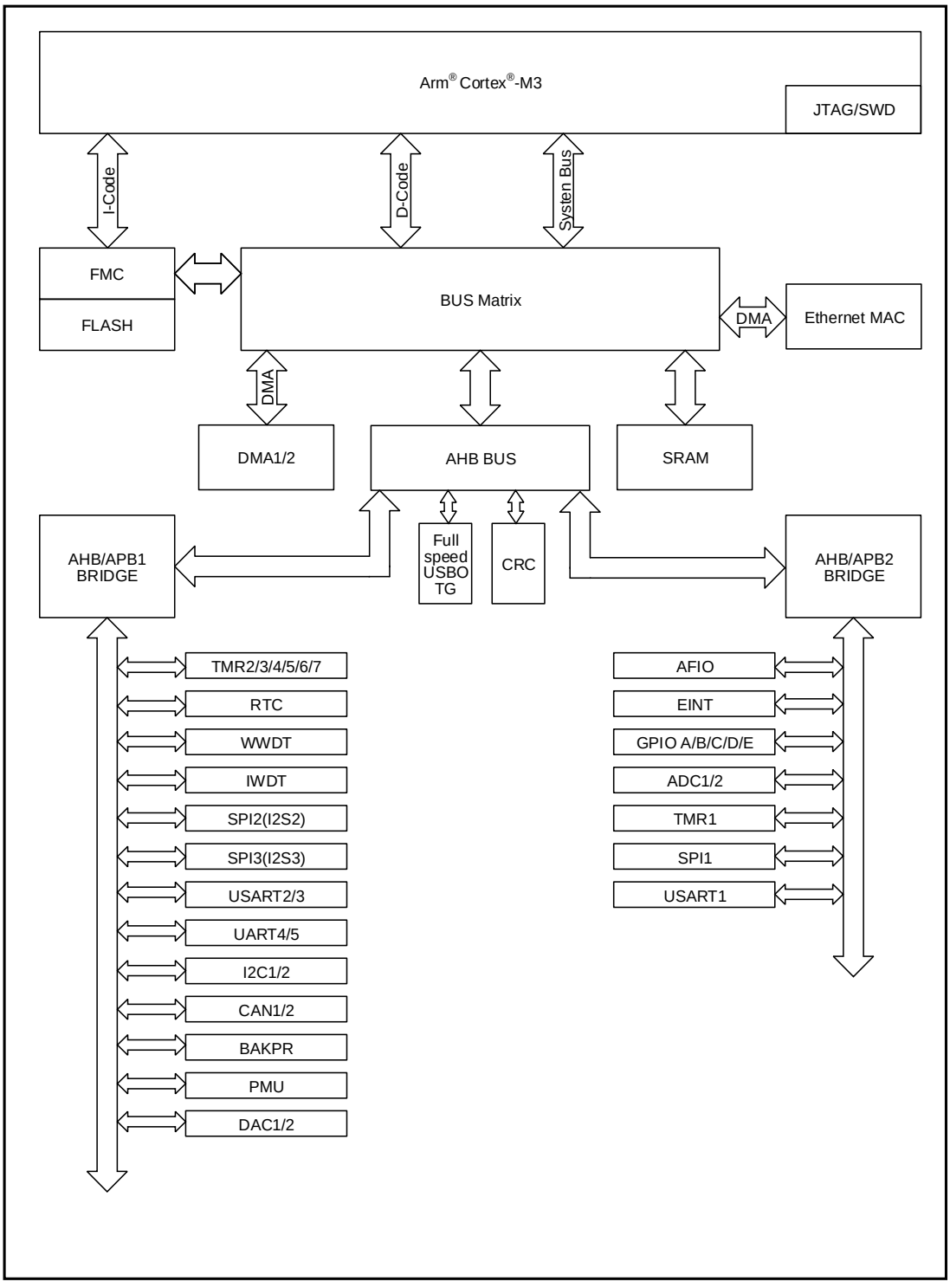
Full name in English	English abbreviation
Advanced High-Performance Bus	AHB
Advanced Peripheral Bus	APB
Device Firmware Update	DFU

2.2 System Architecture Block Diagram

The main system consists of five driving units and three passive units. The five driving units are DCode bus (D-bus), system bus (S-bus), general DMA1, DMA2 and Ethernet DMA, which are connected to the core of Arm® Cortex®-M3. The three passive units are internal SRAM, internal flash memory and bridge from AHB to APB (AHB/APBx), where AHB/APBx connects all APB devices.

These are connected through a multi-level AHB bus architecture, as shown in the figure below:

Figure 1 APM32F107 105xx System Architecture Block Diagram



Note:

(1) F107 product only has one I2C; F105 product has two I2Cs

(2) F107 product has Ethernet unit; The F105 product does not have an Ethernet unit.

Table 5 Bus Name

Name	Instruction
ICode Bus	Connect the instruction bus of Arm® Cortex®-M3 core and the flash instruction interface. Used for prefetched instructions.
DCode Bus	Connect the DCode bus of Arm® Cortex®-M3 core and the data interface of flash memory. Used for constants loading and access debugging.
System bus	Connect the system bus (peripheral bus) of Arm® Cortex®-M3 core and the bus matrix.
DMA bus	Connect AHB master control interface of DMA and the bus matrix.
Bus matrix	Coordinate the access to the core and DMA; coordinate the access of CPU's DCode and DMA to SRAM, Flash and peripherals. AHB peripheral is connected with the system bus through the bus matrix and is allowed to access DMA.
AHB/APB bridge	The two bridges provide a synchronous connection between AHB and the two APB buses. The maximum operating speed of APB1 and APB2 is different. The non-32-bit access to APB register will be converted into 32 bits automatically.

2.3 Memory Mapping

The memory mapping address is totally 4GB address. The assigned addresses include the core (including core peripherals), on-chip Flash (including main memory area, system memory area and option bytes), on-chip SRAM, EMMC and bus peripherals (including AHB and APB peripherals). Please refer to the data manual of the corresponding model for specific information of various addresses.

2.3.1 Embedded SRAM

Built-in static SRAM. It can access by byte, half word (16 bits) or full word (32 bits). The start address of SRAM is 0x2000 0000.

2.3.2 Bit band

Arm® Cortex®-M3 memory is mapped with two bit-band areas, and it maps each word in the alias memory area to one bit in the bit-band memory. Write a word to the alias memory and there will be the same effect as the read-change-write operation on the target of the bit-band area. Both peripheral register and SRAM are mapped into one bit band area, and it is allowed to perform single bit-band write and read operations.

The following gives a mapping formula:

bit_word_addr=bit_band_base+（byte_offset×32）+（bit_number×4）

Please see *Arm® Cortex®-M3 Technical Reference Manual* for details

2.4 Startup Configuration

Since the CPU of Arm® Cortex®-M3 core obtains reset vector from ICode Bus

(instruction bus), the startup can only start from the code area, and the typical is Flash memory boot. However, APM32F MCU series realizes a special mechanism. By configuring the BOOT[1:0] pin parameters, there are three different startup modes, namely, the system can not only start from Flash memory or system memory, but also start from the built-in SRAM. The memory selected as the start zone is determined by the selected startup mode.

Table 6 Startup Mode Configuration and Access Mode

Startup mode selection pin		Startup mode	Access mode
BOOT1	BOOT0		
X	0	Main flash memory（Flash）	The main flash memory is mapped to the boot space, but it can still be accessed at its original address, that is, the contents of the flash memory can be accessed in two address areas.
0	1	System memory	The system memory is mapped to the boot space (0x0000 0000), but it can still be accessed at its original address.
1	1	Built-in SRAM	SRAM can be accessed only at the starting address.

Note:

(1) The boot space address is 0x0000 0000

(2) The original address of Flash is 0x0800 0000

(3) The original address of system memory is 0x1FFF B000

(4) The starting address of SRAM is 0x2000 0000

The user can select the startup mode after reset by setting the states of BOOT1 and BOOT0 pins.

BOOT pin should keep the user's required startup configuration in standby mode. When exiting from the standby mode, the value of boot pin will be latched.

If you choose to start from built-in SRAM, you must use NVIC's exception table and offset register to remap the vector table to SRAM when writing the application code.

Embedded startup program

The embedded startup program is written by Geehy on the production line and stored in the system storage area. The Flash memory can be reprogrammed by using USRAT1, USART2 (remapped), CAN2 (remapped) or USB OTG_FS device mode (DFU) to enable the startup program. After leaving the factory, this area is locked to prevent users from erasing and writing.

Note: Since the use of USB OTG_FS device mode requires a pull-up resistor, the user can activate the internal pull-up resistor by connecting a high level to the PA9 pin, or connect an external pull-up resistor.

3 FLASH Memory

This chapter mainly introduces the storage structure, read, erase, write, read/write protection, unlock/lock characteristics of Flash, and the involved register functional description.

3.1 Full Name and Abbreviation Description of Terms

Table 7 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Flash Memory Controller	FMC

3.2 Main Characteristics

（1） Flash memory structure

- Contain main memory area and information block
- The capacity of main memory area is up to 256KB
- The information block is divided into system memory area and option byte
- The capacity of the system memory area is 18KB, for storing BootLoader program, 96-bit unique UID, and main memory area capacity information
- The capacity of the option byte area is 16Bytes

（2） Functional Description

- Read Flash
- Page/Mass erase Flash
- Write Flash
- Read/Write protection Flash
- Configure option bytes

3.3 Flash Memory Structure

Table 8 Flash Memory Structure of APM32F107 105xx Series Products

Block	Name	Address range	Size (byte)
Main memory block	Page 0	0x0800 0000–0x0800 07FF	2K
Main memory block	Page 1	0x0800 0800–0x0800 0FFF	2K
Main memory block	Page 2	0x0800 1000–0x0800 17FF	2K
Main memory block	Page 3	0x0800 1800–0x0800 1FFF	2K
Main memory block	…	…	…
Main memory block	Page 127	0x0803 F800–0x0803 FFFF	2K

Block	Name	Address range	Size (byte)
Information block	System memory area	0x1FFF B000–0x1FFF F7FF	18K
Information block	Option byte	0x1FFF F800–0x1FFF F80F	16

Note: The number of pages in the main memory block of APM32F107 105xx series products is related to the Flash capacity of specific product.

3.4 Flash Memroy Functional Description

Describe the operation of main memory and information block (including system memory area and option byte), including read, write, erase and read/write protection.

Reading Flash includes main memory block and information block, while the erase, write, read/write protection will be introduced separately; the system memory area has been written before the product leaves the factory and cannot be modified by the user. The erase, write, and read/write protection of the module will not be introduced.

3.4.1 Read Flash

Flash memory can be directly addressed, and reading Flash is affected by the following configuration:

Wait cycle

Different wait cycles should be configured for different system clocks:

- 0 wait cycle: 0<system clock≤24MHz
- 1 wait cycle: 24MHz<system clock≤48MHz
- 2 wait cycles: 48MHz<system clock≤72MHz
- 3 wait cycles: 72MHz<system clock≤96MHz

Prefetch buffer

It can improve the reading speed and the prefetch buffer will be automatically opened every time it is reset; the read interface with prefetch buffer is 2×128 bits for APM32F107 105xx series. Only the system clock and AHB clock consistent and system clock less than 24 MHz to configure open or closed.

Half-cycle access

When the power consumption needs to be optimized, half-cycle access can be used; at this time, the system clock and AHB clock are consistent, and the system clock is 8MHz or less than 8MHz, then half-cycle access to Flash can be used, otherwise, it must be turned on.

3.4.2 Main Memory Block

3.4.2.1 Erase main memory block

FMC supports page erase and mass erase (full erase) to initialize the contents of the main memory area to high level (the data is represented as 0xFFFF). Before writing to Flash, users are advised to erase the write address page. If the data of write address is not 0xFFFF, a programming error will be triggered.

Main memory page erase

Page erase is an independent erase according to the main memory area page selected by the program, which will not have any impact on the page not selected for erasure.

After the correct page erase (or flash write operation) is completed, OCF of FMC_STS register will be set. If OCIE interrupt is enabled, an operation completion interrupt will be triggered. Users need to note that the page to be erased must be a valid page (the valid address of the main memory area and the address not protected by write).

Main memory mass erase

The mass erase operation will erase all the contents in the main storage area of Flash, and the mass erase operation will erase all the data in the main memory area, so the users need to pay special attention when using it to avoid the loss of important data caused by misoperation.

3.4.2.2 Write Main memory block

FMC supports the writing of 16-bit (half word) data in the main memory area. You can select Debug, BootLoader, program running in SRAM, and directly reading the erased page to judge whether the erasing is successful.

In order to ensure correct writing, it is necessary to check whether the destination address has been erased before writing; if it is not erased, the written data will be invalid and PEF bit of FMC_STS register will be set to "1". If the destination address has write protection, the written data is invalid and a write protection error will be triggered (WPEF bit of FMC_STS is set to "1").

3.4.2.3 Main memory block of read/write protection

Read/Write protection of the flash is used to prevent illegal reading/modification of the main memory area code or data, and it is controlled by the read/write protection configuration byte of option byte. For APM32F107 105xx series products, the basic unit of read/write protection is 2 pages (i.e. 4KBytes).

Read protection

Internal Flash protection level can be set by modifying the value of option byte

READPROT. The debugger is always connected to JTAG/SWD interface to set read protection, which takes effect after power-on reset. When the READPROT value is any value except 0xA5, enable read protection and the content of main memory block cannot be read; when the READPROT value is 0xA5, the protection is released and the content of main memory block can be read; when the read protection is removed, a main memory mass erase operation will be triggered to prevent illegal read after the protection is degraded.

Write protection

Write protection control can be conducted for the corresponding page of the main memory block by configuring the value of write protection option byte WRP0/1/2/3. After the write protection is turned on, the content on the corresponding page of the main memory area cannot be modified in any way.

3.4.2.4 Main memory block of unlock/lock

If FMC_CTRL1 register is locked, the main memory block is also locked, so FMC_CTRL1 register should be unlocked if erase/write the main memory block.

FMC_CTRL1 of the reset FMC will be locked by hardware after reseted, and then FMC_CTRL1 can't be directly written, and the corresponding value must be written to FMC_KEY according to the correct sequence to unlock FMC. The KEY value is as follows:

- KEY1=0x45670123
- KEY2=0xCDEF89AB

The wrong writing sequence or wrong value will cause the program to enter the hardware wrongly. At this time, FMC will be locked, and all FMC operations will be invalid until it is reset next time. The users can also lock FMC through software by writing "1" to LOCK bit of the control register 2 (FMC_CTRL2).

In each Flash programming operation, the users must follow the steps of "Flash unlocked - program by user - Flash locked", so as to avoid the risk that user code/data is accidentally modified due to the Flash unlocking after the Flash programming operation.

3.4.3 Option Byte

3.4.3.1 Erase option byte

Support erase function. After the correct option byte erase (or option byte write operation) is completed, OCF of FMC_STS register will be set. If OCIE interrupt is enabled, an operation completion interrupt will be triggered.

3.4.3.2 Write option byte

Eight configurable bytes of option bytes all support writing function.

3.4.3.3 Option byte of write protection

By default, the option byte is always readable and write protected. To perform write operation (program/erase) for the option byte block, first write the correct key sequence (the same as that of locking) in FMC_OBKEY, and then allow the write operation of option byte block; the OBWEN bit of FMC_CTRL2 register indicates write enabled; clear this bit and write operation will be disabled.

3.4.3.4 Unlock/Lock option byte

After the system reset, the option byte is locked by default. Only when the option byte is unlocked correctly, can it be modified. The difference between option byte unlocking and flash unlocking is that FMC_OBKEY register rather than FMC_KEY register writes the KEY value. The option byte does not support "software lock". The user should pay special attention to that every time after the value of the option byte is modified, the system must be reset to make it effective.

3.5 Option Byte Register Functional Description

The option byte provides some optional functions for users, and it mainly consists of 8 configurable bytes and corresponding complementary codes. Every time the system is reset, the option byte area will be reloaded to the FMC_ OBCS and FMC_WRTPROT register (the option byte will only take effect each time they are reloaded to FMC). In the process of reloading, if a certain configurable byte does not match its inverse code, an option byte error (OBE bit of FMC_OBCS register is set to "1") will be triggered, and this byte will be set to "0xFF". The information of 16 bytes in the option byte area is shown in the table below.

Table 9 Option Bytes

Address	Option byte	Initial value	R/W	Functional description
0x1FFF F800	READPROT	0xA5	R/W	Read protection configuration
0x1FFF F801	nREADPROT	0x5A	R	READPROT complementary code
0x1FFF F802	UOB	0xFF	R/W	User option byte Bit 0: WDTSEL 0: Hardware watchdog 1: Software watchdog Bit 1: nRSTSTOP 0: Reset occurs when entering the Stop mode 1: Reset does not occur when entering the Stop mode Bit 2: nRSTSTB 0: Reset occurs when entering the Standby mode

Address	Option byte	Initial value	R/W	Functional description
				1: Do not generate reset when entering Standby mode [3:7]: Reserved
0x1FFF F803	nUOB	0x00	R	UOB complementary code
0x1FFF F804	Data0	0xFF	R/W	User data byte 0
0x1FFF F805	nData0	0x00	R	Data0 complementary code
0x1FFF F806	Data1	0xFF	R/W	User data byte 1
0x1FFF F807	nData1	0x00	R	Data1 complementary code
0x1FFF F808	WRP0	0xFF	R/W	Write protection configuration 0
0x1FFF F809	nWRP0	0x00	R	WRP0 complementary code
0x1FFF F80A	WRP1	0xFF	R/W	Write protection configuration 1
0x1FFF F80B	nWRP1	0x00	R	WRP1 complementary code
0x1FFF F80C	WRP2	0xFF	R/W	Write protection configuration 2
0x1FFF F80D	nWRP2	0x00	R	WRP2 complementary code
0x1FFF F80E	WRP3	0xFF	R/W	Write protection configuration 3
0x1FFF F80F	nWRP3	0x00	R	WRP3 complementary code

Note: When the configurable byte and its complementary value are "0xFF", the match will not be verified in the reloading process

Table 10 Write Protection WRPx Function Description of Main Memory Area

Product capacity	Functional description
APM32F107 105xx series products (2KB/page)	Each bit in WRPx controls the write protection of 4KB (2 pages) address of the main memory area, But pages 62-127 provide protection at the same time. 0: Write protection is turned on 1: Write protection is not turned on WRP0: Page 0-15 WRP1: Page 16-31 WRP2: Page 32-47 WRP3: Bit0-Bit6 controls Page 48-61; Bit7 controls Page 62-127

Note: Flash read/write protection configuration is independent of each other. Removing the write protection will not force the loss of the contents of the main memory area, but keep them as they are.

3.6 FMC Register Address Mapping

Base address: 0x40022000

Table 11 FMC Register Address Mapping

Register name	Description	Offset address
FMC_CTRL1	Control register 1	0x00

Register name	Description	Offset address
FMC_KEY	Key register	0x04
FMC_OBKEY	Option byte register	0x08
FMC_STS	State register	0x0C
FMC_CTRL2	Control register 2	0x10
FMC_ADDR	Flash address register	0x14
FMC_OBCS	Option byte control/state register	0x1C
FMC_WRTPROT	Write protection register	0x20

3.7 FMC Register Functional Description

3.7.1 Control register 1 (FMC_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0030

Field	Name	R/W	Description
2:0	WS	R/W	Wait State Configure 000: 0 wait cycle, 0<system clock≤24MHz 001: 1 wait cycle: 24MHz<system clock≤48MHz 010: 2 wait cycles, 48MHz<system clock≤72MHz 011: 3 wait cycles, 72MHz<system clock≤96MHz
3	HCAEN	R/W	Flash Half Cycle Access Enable 0: Disable 1: Enable
4	PBEN	R/W	Prefetch Buffer Enable 0: Disable 1: Enable
5	PBSF	R	Prefetch Buffer Status Flag 0: In disabled state 1: In enabled state
31:6	Reserved		

3.7.2 Key register (FMC_KEY)

Offset address: 0x04

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
31:0	KEY	W	FMC Key Writing the keys represented by these bits can unlock FMC. These bits can only perform write operation, and 0 is returned when read operation is performed.

3.7.3 Option byte key register (FMC_OBKEY)

Offset address: 0x08

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
31:0	OBKEY	W	Option Byte Key Writing the keys represented by these bits can unlock the option byte write operation. These bits can only perform write operation and 0 is returned when read operation is performed.

3.7.4 State register (FMC_STS)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	BUSYF	R	Busy Flag This bit indicates that a flash operation is in progress. These bits can only perform write operation, and 0 is returned when read operation is performed.
1	Reserved		
2	PEF	R/W	Programming Error Flag This bit will be set by software when the value before the address is edited is not "0xFFFF".
3	Reserved		
4	WPEF	R/W	Write Protection Error Flag This bit will be set by hardware when programming the write protection address in FLASH.
5	OCF	R/W	Operation Complete Flag This bit will be set by hardware when read/write operation in FLASH is completed.
31:6	Reserved		

3.7.5 Control register 2 (FMC_CTRL2)

Offset address: 0x10

Reset value: 0x0000 0080

Field	Name	R/W	Description
0	PG	R/W	Program Set this bit to 1 to program Flash
1	PAGEERA	R/W	Page Erase Set this bit to 1 to erase the page
2	MASSERA	R/W	Mass Erase Set this bit to 1 to erase the mass.
3	Reserved		
4	OBP	R/W	Option Byte Program Set this bit to 1 to program the option byte.
5	OBE	R/W	Option Byte Erase Set this bit to 1 to erase the option byte.
6	STA	R/W	Start Erase This bit can be only set to 1 by software, and can be reset by clearing STS_BUSYF bit.

Field	Name	R/W	Description
7	LOCK	R/W	Lock This bit can be written to 1 only, and when this bit is set to 1, it means that FMC and CTRL2 registers are locked.
8	Reserved		
9	OBWEN	R/W	Option Byte Write Enable When this bit is set to 1, the option byte can be programmed.
10	ERRIE	R/W	Error Interrupt Enable 0: Interrupt is disabled 1: Interrupt is enabled When STS_PEF=1 or STS_WPEF=1, set this bit to generate an interrupt.
11	Reserved		
12	OCIE	R/W	Operation Complete Interrupt Enable 0: Operation completion interrupt is disabled 1: Operation completion interrupt is enabled When STS_OCF=1, set this bit to generate an interrupt.
31:13	Reserved		

3.7.6 Address register (FMC_ADDR)

Offset address: 0x14

Reset value: 0x0000 0000

The register is changed to currently/finally used address by hardware; in page erasing, the register needs to be configured by software.

Field	Name	R/W	Description
31:0	ADDR	W	Flash Address In programming operation, the bit is written to the address to be programmed; in page erasing, this bit is written to the page to be erased.

3.7.7 Option byte control/state register (FMC_OBCS)

Offset address: 0x1C

Reset value: 0x03FF FFFC

The reset value of the register is related to the value in the written option byte; the reset value of OBE bit is related to the result whether the value of the loaded option byte is consistent with its reverse code.

Field	Name	R/W	Description
0	OBE	R	Option Byte Error 1: The loaded option byte does not match its complementary code. The option byte and its complementary code are forced to write to 0xFF
1	READPROT	R	Read Protect 1: Indicate that the flash memory is in read protection state

Field	Name	R/W	Description
9:2	UOB	R	User Option Byte Here includes the user option bytes loaded by OBL Bit 2: WDTSEL Bit 3: RSTSTOP Bit 4: RSTSTDB Bit [9:5]: Unused
17:10	DATA0	R	Data0
25:18	DATA1	R	Data1
31:26	Reserved		

3.7.8 Write protection register (FMC_WRTPROT)

Offset address: 0x20

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	WRTPROT	R	Write Protect 0: Valid 1: Invalid

4 Reset and Clock Management (RCM)

4.1 Full Name and Abbreviation Description of Terms

Table 12 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Reset and Clock Management	RCM
Reset	RST
Power-On Reset	POR
Power-Down Reset	PDR
High Speed External Clock	HSECLK
Low Speed External Clock	LSECLK
High Speed Internal Clock	HSICLK
Low Speed Internal Clock	LSICLK
Phase Locked Loop	PLL
Main Clock Output	MCO
Calibrate	CAL
Trim	TRIM
Wakeup	WUP
Automatic Wakeup	AWUP
Backup	BAKP
Low Power	LPWR
Clock Security System	CSS
Non Maskable Interrupt	NMI

4.2 Reset Functional Description

The supported reset is divided into three forms, namely, system reset, power reset and backup area reset.

4.2.1 System Reset

4.2.1.1 "System reset" reset source

The reset source is divided into external reset source and internal reset source.

External reset source:

- Low level on NRST pin.

Internal reset source:

- Window watchdog termination count (WWDT reset)
- Independent watchdog termination count (IWDT reset)
- Software reset (SW reset)
- Low-power management reset
- Power reset

A system reset will occur in case of any of the above events. Besides, the reset event source can be identified by viewing the reset flag bit in RCM_CSTS (control/state register).

Generally, when the system is reset, all registers except the registers in RCM_CSTS (control/state register) reset flag bit and backup area will be reset to the reset state.

Software reset

Software can be reset by putting SYSRESETREQ in Arm® Cortex®-M3 interrupt application and reset control register to "1".

Low-power management reset

Low-power management may reset in two cases, one is when entering the standby mode, and the other is when entering the stop mode. In these two cases, if RSTSTDB bit (in standby mode) or RSTSTOP bit (in stop mode) in user selection byte is cleared, the system will be reset rather than entering the standby or stop mode.

For more information about user option bytes, refer to "Flash memory".

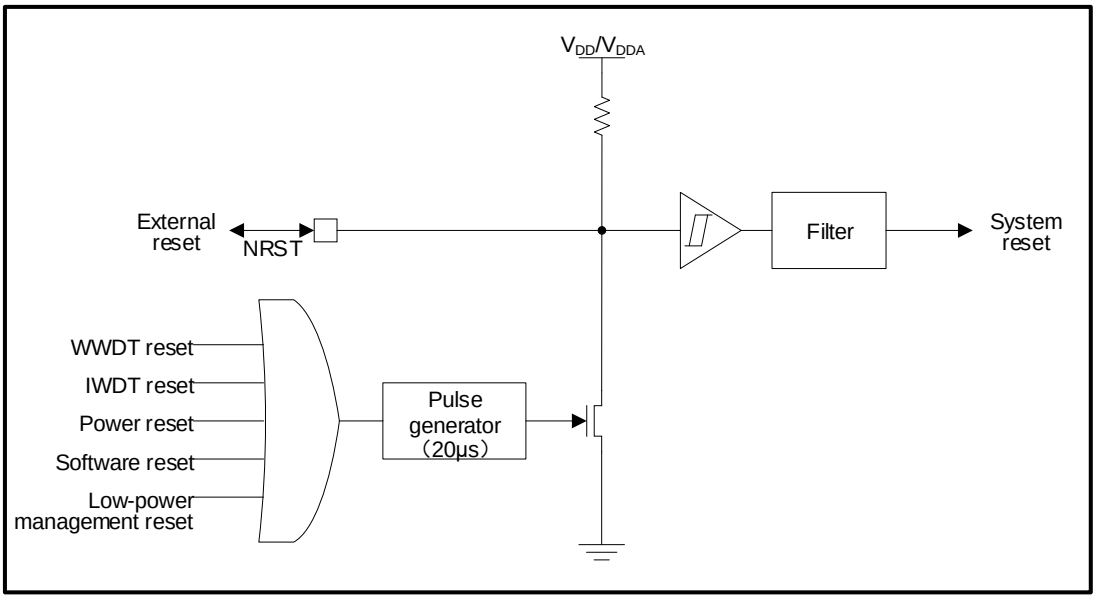
4.2.1.2 "System Reset" reset circuit

The reset source is used in the NRST pin, which remains low in reset process.

The internal reset source generates a delay of at least 20μs pulse on the NRST pin through the pulse generator, which causes the NRST to maintain the level to generate reset; the external reset source directly pulls down the NRST pin level to generate reset.

The "system reset" reset circuit is shown in the figure below.

Figure 2 "System Reset" Reset Circuit



4.2.2 Power Reset

"Power reset" reset source

"Power reset" reset source is as follows:

- Power-on reset (POR reset)
- Power-down reset (PDR reset)
- Wake up from standby mode

A power reset will occur in case of any of the above events.

Power reset will reset all registers except that in backup area.

4.2.3 Backup Domain Reset

"Backup domain reset" reset source

"Backup domain reset" reset source is as follows:

- Software resets and sets the BDRST bit in RCM_BDCTRL (backup domain control register)
- V_{DD} or V_{BAT} is powered on when V_{DD} and V_{BAT} is powered down

A backup domain reset will occur in case of any of the above events.

The backup area reset has two special resets, which only affect backup area.

4.3 Functional Description of Clock Management

Clock sources of the whole system are: HSECLK, LSECLK, HSICLK, LSICLK, PLL. For the characteristics of the clock source, please refer to the relevant chapter of "Electrical Characteristics" in the data manual.

4.3.1 External Clock Source

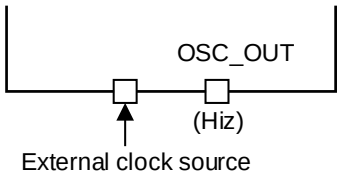
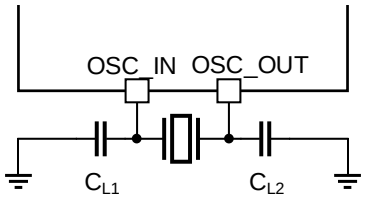
The external clock signal includes HSECLK (high-speed external clock signal) and LSECLK (low-speed external clock signal).

There are two kinds of external clock sources:

- External crystal/ceramic resonator
- External clock of user

The hardware configuration of the two kinds of clock sources is shown in the figure below.

Figure 3 HSECLK/LSECLK Clock Source Hardware Configuration

Clock source	Hardware configuration
External clock	
Crystal/Ceramic resonator	

In order to reduce the distortion of clock output and shorten the start-up stabilization time, the crystal/ceramic resonator and load capacitor must be as close to the oscillator pin as possible. The value of load capacitance (C_{L1}, C_{L2}) must be adjusted according to the selected oscillator.

4.3.1.1 HSECLK high-speed external clock signal

HSECLK clock signal is generated by HSECLK external crystal/ceramic resonator and HSECLK external clock two kinds of clock sources.

Table13 Clock Source Generting HSECLK

Name	Instruction
External clock source (HSECLK bypass)	Provide clock to MCU through OSC_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the maximum frequency is up to 25MHz. For hardware connection, it must be connected to OSC_IN pin, ensuring OSC_OUT pin is suspended; for MCU configuration, the user can select this mode by setting HSEBCFG and HSEEN bits in RCM_CTRL.

Name	Instruction
External crystal/ceramic resonator (HSECLK crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency range is 3-25MHz. When needing to connect OSC_IN and OSC_OUT to the resonator , start and close by setting the HSEEN bit in RCM_CTRL. HSERDYFLG bit in clock control register RCM_CTRL is used to indicate whether the high-speed external oscillator is stable. After startup, the clock is not released until this bit is set to "1" by hardware. If interrupt is allowed in RCM_INT (clock interrupt register), corresponding interrupt will be generated.

4.3.1.2 LSECLK low-speed external clock signal

LSECLK clock signal is generated by LSECLK external crystal/ceramic resonator and LSECLK external clock two kinds of clock sources.

Table 14 Clock Source Generting LSECLK

Name	Instruction
External clock source (LSECLK bypass)	The cock is provided to to MCU through OSC32_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the signal frequency needs to be 32.768kHz. For hardware connection, it must be connected to OSC32_IN pin, ensuring OSC32_OUT pin is suspended; for MCU configuration, the user can select this mode by setting LSEBCFG and LSEEN bits in RCM_BDCTRL.
External crystal/ceramic resonator (LSECLK crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency is 32.768kHz. OSC32_IN、OSC32_OUT needs to be connected to the oscillator which can be enabled and disabled through LSEEN bit in RCM_BDCTRL. LSERDYFLG in RCM_BDCTRL indicates whether LSECLK crystal oscillator is stable. At startup stage, LSECLK clock signal is not released until this bit is set to "1" by hardware. If it is allowed in the clock interrupt register, an interrupt request can be generated.

4.3.2 Internal Clock Source

The internal clock includes HSICLK (high-speed internal clock signal) and LSICLK (low-speed internal clock signal).

4.3.2.1 HSICLK high-speed internal clock signal

HSICLK clock signal is generated by internal 8MHz RC oscillator.

The RC oscillator frequency of different chips is different, and that of the same chip may be different with the change of temperature and voltage; the HSICLK clock frequency of each chip has been calibrated to 1% (25 ℃, V_{DD}=V_{DDA}=3.3V) by the manufacturer before leaving the factory. When the system is reset, the value calibrated by the manufacturer will be loaded to

HSICAL bit of the RCM_CTRL; in addition, the users can further adjust the frequency by setting HSITRM in RCM_CTRL according to the application environment (temperature and voltage) of the site.

HSIRDYFLG bit can be used to indicate whether HSICLK RC oscillator is stable. In the clock startup process, HSICLK RC output clock is not released until the HSIRDYFLG bit is set to 1 by hardware. HSICLK RC can be started or closed by HSIEN bit in RCM_CTRL.

Compared with HSECLK crystal oscillator, RC oscillator can provide system clock without any external device; the start time of RC oscillator is shorter than that of HSECLK crystal oscillator; even after calibration, its clock frequency accuracy is still inferior to that of HSECLK crystal oscillator.

4.3.2.2 LSICLK low-speed internal clock signal

Main characteristics of LSICLK

LSICLK is generated by RC oscillator, within the range of 40kHz (30kHz and 60kHz). The frequency may change along with the change of temperature and voltage. It can keep running in stop and standby mode and provide clock for independent watchdog and automatic wake-up unit.

LSICLK can be started or closed by LSIEN bit in RCM_CSTS. LSIRDYFLG bit in RCM_CSTS indicates whether the low-speed internal oscillator is stable. At startup stage, the clock is not released until this bit is set to "1" by hardware. If allowed in RCM_INT, LSICLK interrupt application will be generated.

LSICLK calibration

The purpose of calibrating LSICLK oscillator is to compensate its frequency offset. After calibration, it can get RTC clock base with certain precision and IWDT timeout period.

First, set the channel 4 of TMR5 to the input capture mode, connect the LSICLK clock and measure its clock frequency. Then set the 20-bit prescaler of RTC according to the required RTC time base and the IWDT timeout period with the HSECLK clock frequency as the accuracy guarantee.

4.3.3 PLL (Phase Locked Loop)

The main PLL1 could multiply the HSICLK/2, a divided HSECLK or a divided PLL2CLK.

The input source of PLL2 and PLL3 is the divided HSECLK.

Clock source and multiplication factor should have been selected before enable PLL1/2/3, the selection can’t be changed if PLL1/2/3 is (are) enabled.

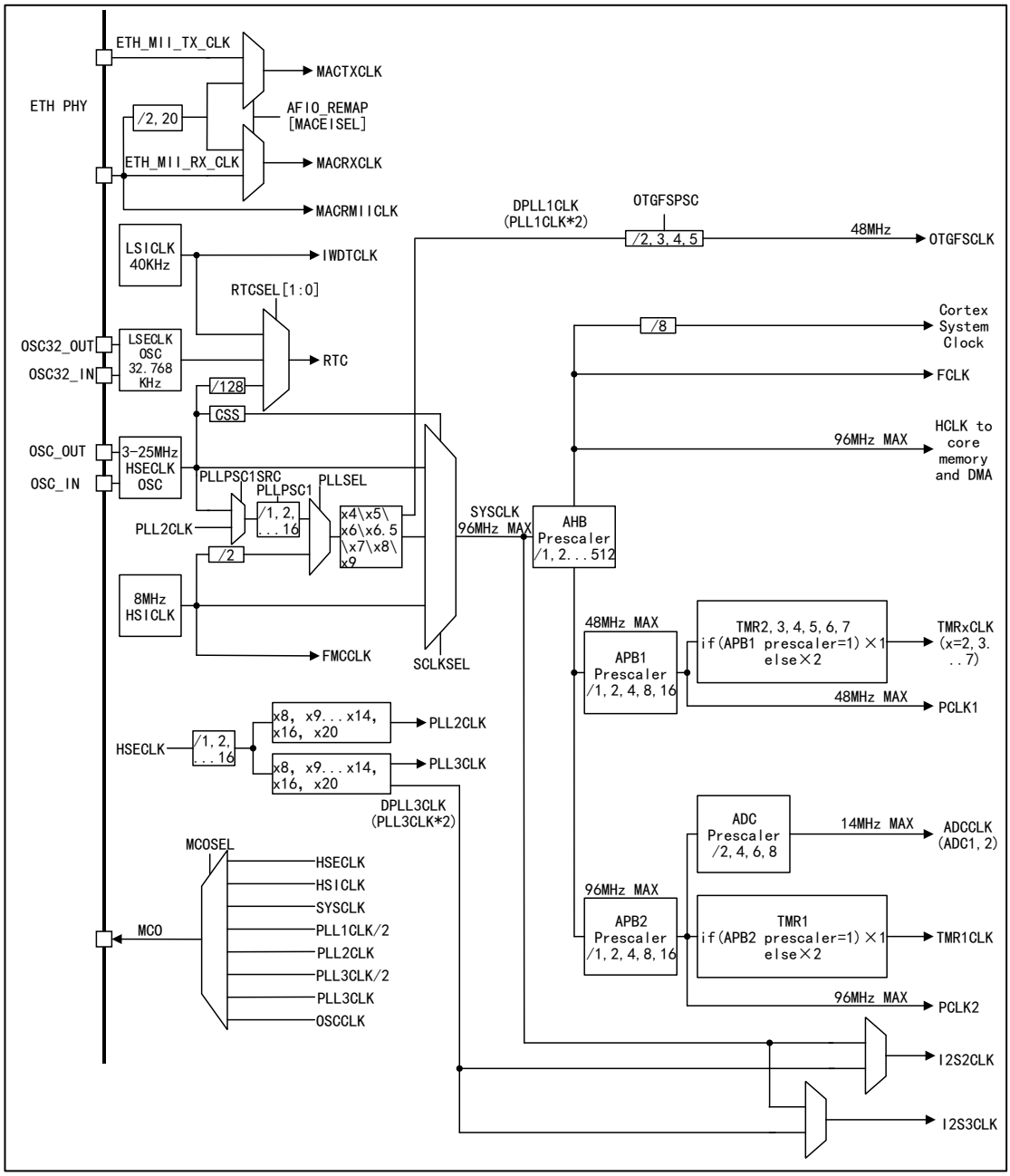
When switching the clock source, make sure that a new clock source is selected

before turning off the previous clock source.

When PLL is ready and PLL interrupt is allowed in RCM_INT, PLL can issue interrupt request.

4.3.4 Clock Tree

Figure 4 APM32F107 105xx Clock Tree



Note:

(1) HCLK means AHB clock.

(2) PCLK1 and PCLK2 are clock signal connected to the peripheral of APB1 and APB2 respectively.

(3) FCLK is running clock of Arm® Cortex®-M3.

(4) The frequency of AHB, APB2 (high-speed APB) and APB1 (low-speed APB) domains can be configured through multiple prescalers. Besides, the maximum frequency of AHB and APB2 domain is 96MHz, while the maximum allowable frequency of APB1 is 48MHz.

(5) When HSICLK is used as the input of PLL clock, the maximum frequency of the system clock is 36MHz.

(6) It must supply 48MHz clock frequency to USB OTG FS.

(7) When needing to run the peripheral connected to AHB and APB, it is required to turn on the corresponding enable end to make the peripheral get the clock signal.

(8) SysTick (system timer) can be provided by the clock signal after frequency division of HCLK8. Different clock sources can be selected by setting SysTick control and status register.

(9) Frequency assignment of all TMRxCLK (timer clocks) is automatically set by the hardware according to the following two situations:

- If the corresponding APB prescaler factor is 1, the clock frequency of the timer is the same as that of the APB bus.
- Otherwise, the clock frequency of the timer will be set to twice the frequency of the APB bus connected to it.

(10) Moreover, the TMRx (x=2,3,4,5,6,7) clock signals is from PCLK1 divided, and the TMR1 clock signals is from PCLK2 dividied.

4.3.5 Clock Source Selection of RTC

HSECLK/128, LSECLK or LSICLK can be selected as RTCCLK clock source by setting RTCSRCSEL bit in RCM_BDCTRL. The selection of clock source can be changed only when the backup domain is reset.

Because LSECLK is in the backup domain, and HSECLK and LSICLK are not in the backup domain, different clocks will be selected as the clock source; the working condition of RTCs are different, and see the following table for details:

Table 15 Working Condition of RTC When RTC Selects Different Clock Sources

Clock source	Working condition
LSECLK is selected as RTC clock	As long as V_{BAT} maintains power supply, RTC will continue to work even if V_{DD} is powered off
LSICLK is selected as automatic wake-up unit clock	If V_{DD} is powered off, AWUP state cannot be guaranteed.
HSECLK/128 as RTC clock	If the V_{DD} is powered off or the internal voltage regulator is turned off (the power supply of 1.3V domain is cut off), the RTC state is uncertain, so the BPWEN bit (cancel the write protection of backup area) of PMU_CTRL (power control register) must be set to "1".

4.3.6 Clock Source Selection of IWDT

When IWDT (independent watchdog) is opened, LSICLK oscillator will be opened by force, and when it is stable, the clock signal will be provided to IWDT. After LSICLK is opened by force, it will always be open and cannot be closed.

4.3.7 Clock Source Selection of MCO

When the corresponding GPIO port register is configured with corresponding function, the clock signal can be selected to be output to MCO pin by MCOSEL in configuration register RCM_CFG (clock configuration register). See the clock tree or MCOSEL bit instructions for specific clock signal.

4.3.8 Clock Source Selection of SYSCLK

After system reset, HSICLK oscillator is selected as the system clock, which cannot be stopped. If you want to switch the SYSCLK clock source, you must wait until the destination clock source is ready (i.e. the destination clock source is stable). The target clock source can be HSECLK and PLLCLK.

The state bit of RCM_CFG can indicate the ready clock and selected SYSCLK clock source.

4.3.9 CSS Clock Security System

In order to prevent MCU from normal operation due to external crystal oscillator short circuit, MCU can activate CSS clock security system through software. After the security system is activated, if the HSECLK oscillator is used as the system clock directly or indirectly (used as the PLL input clock and PLL is used as the system clock), the external HSECLK oscillator will be turned off when the HSECLK clock fails, and the system clock will automatically switch to HSICLK. At this time, the PLL which selects HSECLK as the clock input and as the system clock input source will also be turned off.

Note: When CSS is activated by software and HSECLK clock fails, CSS interrupt and NMI (non-maskable interrupt) will be generated. Since NMI is executed continuously before CSS interrupt is cleared, CSSIF bit in RCM_INT register shall be set to clear the interrupt.

4.4 Register Address Mapping

Table16 RCM Register Address Mapping

Register name	Description	Offset address
RCM_CTRL	Clock control register	0x00
RCM_CFG1	Clock configuration register1	0x04
RCM_INT	Clock interrupt register	0x08
RCM_APB2RST	APB2 peripheral reset register	0x0C
RCM_APB1RST	APB1 peripheral reset register	0x10

Register name	Description	Offset address
RCM_AHBCLKEN	AHB peripheral clock enable register	0x14
RCM_APB2CLKEN	APB2 peripheral clock enable register	0x18
RCM_APB1CLKEN	APB1 peripheral clock enable register	0x1C
RCM_BDCTRL	Backup domain control register	0x20
RCM_CSTS	Control/State register	0x24
RCM_AHBRST	AHB peripheral reset register	0x28
RCM_CFG2	Clock configruation register2	0x2C

4.5 Register Functional Description

4.5.1 Clock control register (RCM_CTRL)

Offset address: 0x00

Reset value: 0x0000 XX83; X means undefined

Access: Access in the form of word, half word and byte, without wait cycle

Field	Name	R/W	Description
0	HSIEN	R/W	High Speed Internal Clock Enable Set 1 or clear 0 by software. HSICLK is an RC oscillator. When one of the following conditions occurs, it will be set to 1 by the hardware: power-on start, software reset, wake-up from standby mode, wake-up from stop mode, failure of external high-speed clock source (as system clock). When HSICLK is used as system clock or provides system clock through PLL1, this bit cannot be cleared. 0: HSICLK RC oscillator is disabled 1: HSICLK RC oscillator is turned on
1	HSIRDYFLG	R	High Speed Internal Clock Ready Flag 0: HSICLK RC oscillator is not stable 1: HSICLK RC oscillator is stable
2	Reserved		
7:3	HSITRM	R/W	High Speed Internal Clock Trim The product has been calibrated to 8MHz±1% when leaving the factory. However, it changes as the temperature and voltage changes, but the frequency of HSICLK RC oscillator can be adjusted by HSITRM.
15:8	HSICAL	R	High Speed Internal Clock Calibrate When the system is started up, the calibration parameters will be automatically written to the register.
16	HSEEN	R/W	High Speed External Clock Enable When entering the standby or stop mode, this bit is cleared by hardware and HSECLK is turned off; when HSECLK is used as system clock source or the system clock is provided through PLL1, this bit cannot be cleared. 0: HSECLK is disabled

Field	Name	R/W	Description
			1: HSECLK is enabled
17	HSERDYFLG	R	High Speed External Clock Ready Flag When HSECLK is stable, this bit is set to 1 by hardware and cleared by software. 0: HSECLK is not stable 1: HSECLK is stable
18	HSEBCFG	R/W	High Speed External Clock Bypass Configure Bypass mode refers to the mode in which external clock is used as the HSECLK clock source; otherwise the resonator is used as the HSECLK clock source. 0: Non-bypass mode 1: Bypass mode
19	CSSEN	R/W	Clock Security System Enable 0: Disable 1: Enable (When the HSECLK oscillator is ready)
23:20	Reserved		
24	PLL1EN	R/W	PLL1 Enable When entering the standby and stop mode, this bit is cleared by the hardware; when PLL1CLK has been configured (or in the process of configuration) as the clock source of the system clock, this bit cannot be cleared; in other cases, it can be set to 1 or cleared to 0 by the software. 0: PLL1 is disabled 1: PLL1 is enabled
25	PLL1RDYFLG	R	PLL1 Clock Ready Flag PLL1 is set to 1 by hardware after it is locked. 0: PLL1 is unlocked 1: PLL1 is locked
26	PLL2EN	R/W	PLL2 Enable When entering the standby and stop mode, this bit is cleared by the hardware; when PLL2CLK has been configured as the clock source of the system clock, this bit cannot be cleared. 0: PLL2 is disabled 1: PLL2 is enabled
27	PLL2RDYFLG	R	PLL2 Clock Ready Flag PLL2 is set to 1 by hardware after it is locked. 0: PLL2 is unlocked 1: PLL2 is locked
28	PLL3EN	R/W	PLL3 Enable Set or clear by software. When entering the standby and stop mode, this bit is cleared by the hardware. 0: PLL3 is disabled 1: PLL3 is enabled
29	PLL3RDYFLG	R	PLL3 Clock Ready Flag PLL3 is set to 1 by hardware after it is locked. 0: PLL3 is unlocked

Field	Name	R/W	Description
			1: PLL3 is locked
31:30	Reserved		

4.5.2 Clock configuration register1 (RCM_CFG1)

Offset address: 0x04

Reset value: 0x0000 0000

All bits of this register are set or cleared by software.

Access: Access in the form of word, half word and byte, with 0 to 2 wait cycles. 1 or 2 wait cycles are inserted only when the access occurs during clock switching.

Field	Name	R/W	Description
1:0	SCLKSEL	R/W	System Clock Source Select Select system clock source. When returning from stop or standby mode or the HSE directly or indirectly used as system clock fails, the hardware selects HSICLK as system clock by force (if the clock security system has been started) 00: HSICLK is used as system clock 01: HSECLK is used as system clock 10: PLL1CLK is used as system clock 11: Unavailable
3:2	SCLKSELSTS	R	System Clock Selection Status Indicate which clock source is used as system clock. 00: HSICLK is used as system clock 01: HSECLK is used as system clock 10: PLL1CLK output is used as system clock 11: Unavailable
7:4	AHBPSC	R/W	AHB Clock Prescaler Factor Configure Control the prescaler factor of AHB clock. 0xxx: No frequency division for SYSCLK 1000: SYSCLK 2-divided frequency 1001: SYSCLK 4-divided frequency 1010: SYSCLK 8-divided frequency 1011: SYSCLK 16-divided frequency 1100: SYSCLK 64-divided frequency 1101: SYSCLK 128-divided frequency 1110: SYSCLK 256-divided frequency 1111: SYSCLK 512-divided frequency Note: When the prescaler factor of AHB clock is greater than 1, the prefetch buffer must be enabled. AHB clock frequency shall be at least 25MHz if use Ethernet MAC.
10:8	APB1PSC	R/W	APB1 Clock Prescaler Factor Configure Control the prescaler factor of low-speed APB1 clock (PCLK1) Warning: Softwre must ensure APB1 clock frequency is not greater than 48MHz. 0xx: No frequency division for HCLK

Field	Name	R/W	Description
			100: HCLK 2-divided frequency 101: HCLK 4-divided frequency 110: HCLK 8-divided frequency 111: HCLK 16-divided frequency
13:11	APB2PSC	R/W	APB1 Clock Prescaler Factor Control the prescaler factor of high-speed APB2 clock (PCLK2) 0xx: No frequency division for HCLK 100: HCLK 2-divided frequency 101: HCLK 4-divided frequency 110: HCLK 8-divided frequency 111: HCLK 16-divided frequency
15:14	ADCPSC	R/W	ADC Clock Prescaler Factor Configure Determine ADC clock frequency 00: PCLK2 is used as ADCCLK after two divided frequency 01: PCLK2 is used as ADCCLK after four divided frequency 10: PCLK2 is used as ADCCLK after six divided frequency 11: PCLK2 is used as ADCCLK after eight divided frequency
16	PLL1SRCSEL	R/W	PLL1 Clock Source Select Select PLL1 input clock source. 0: HSICLK RC oscillator clock is used as PLL1 input clock after 2 divided frequency 1: HSECLK is used as PLL1 input clock Note: This bit can be written only when PLL1 is disabled.
17	PLLPSC1L	R/W	LSB of PLLPSC1 This bit is the LSB of PLLPSC1. It could be set by software which is the same as bit (0) in the RCM_CFG2 register, so modifying bit(0) in the RCC_CFGR2 register changes this bit accordingly. Note: This bit can be written only when PLL1 is disabled.
21:18	PLL1MULCFG	R/W	PLL1 Multiplication Factor Configure Determine PLL1 multiplication factor. This bit can be written only when PLL1 is disabled. 000x: Reserved 0010: PLL1CLK 4-multiple frequency output 0011: PLL1CLK 5-multiple frequency output 0100: PLL1CLK 6-multiple frequency output 0101: PLL1CLK 7-multiple frequency output 0110: PLL1CLK 8-multiple frequency output 0111: PLL1CLK 9-multiple frequency output 10xx: Reserved 1100: Reserved 1101: PLLCLK 6.5-multiple frequency output 111x: Reserved Note: The output frequency of PLL1CLK cannot be greater than 96MHz.
23:22	OTGFSPSC	R/W	USB OTG_FS Prescaler Factor Configure This bit is configured to generate the 48MHz OTG_FS clock.

Field	Name	R/W	Description
			It must be vaild before enabling the OTG_FS clock. If OTG_FS clock is enabled, this bit cannot be cleared. 00: DPLL1CLK (PLL1CLK x 2) is divided by 3 as OTG_FS clock. 01: DPLL1CLK (PLL1CLK x 2) is divided by 2 as OTG_FS clock 10: DPLL1CLK (PLL1CLK x 2) is divided by 4 as OTG_FS clock 11: DPLL1CLK (PLL1CLK x 2) is divided by 5 as OTG_FS clock Note: (1) The OTG_FS clock frequency must be 48MHz. (2) The bit 23 is write-only
27:24	MCOSEL	R/W	Main Clock Output Select Set or clear by software. 00xx: No clock output 0100: System clock (SYSCLK) output 0101: Internal RC oscillator clock (HSICLK) output 0110: External oscillator clock (HSECLK) output 0111: PLL1CLK is output after being divided by 2 1000: PLL2CLK output 1001: PLL3CLK is output after being divided by 2 1010: OSCCLK output (for Ethernet) 1011: PLL3CLK output (for Ethernet) Others: Reserved Note: 1. The clock output may be truncated when starting and switching the MCO clock source. 2. When the system clock is output to the MCO pin, please ensure that the output clock frequency is not greater than 50MHz (maximum frequency of I/O port).
31:28	Reserved		

4.5.3 Clock interrupt register (RCM_INT)

Offset address: 0x08

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

Field	Name	R/W	Description
0	LSIRDYFLG	R	LSICLK Ready Interrupt Flag When the internal low-speed clock is ready and the LSIRDYEN bit is set to 1, it is set to 1 by the hardware. The software clears the bit by setting 1LSIRDYCLR. 0: No LSICLK ready interrupt 1: LSICLK ready interrupt occurred
1	LSERDYFLG	R	LSECLK Ready Interrupt Flag When the external low-speed clock is ready and the LSERDYEN bit is set to 1, it is set to 1 by the hardware. The software clears the bit by setting 1LSERDYCLR. 0: No LSECLK ready interrupt 1: LSECLK ready interrupt occurred

Field	Name	R/W	Description
2	HSIRDYFLG	R	HSICLK Ready Interrupt Flag When the internal high-speed clock is ready and the HSIRDYEN bit is set to 1, it is set to 1 by the hardware. The software clears the bit by setting 1HSIRDYCLR. 0: No HSICLK ready interrupt 1: HSICLK ready interrupt occurred
3	HSERDYFLG	R	HSECLK Ready Interrupt Flag When the external low-speed clock is ready and the HSERDYCLR bit is set to 1, it is set to 1 by the hardware. The software clears the bit by setting 1 HSERDYCLR. 0: No HSECLK ready interrupt 1: HSECLK ready interrupt occurred
4	PLL1RDYFLG	R	PLL1 Ready Interrupt Flag When PLL1 is ready and PLL1RDYEN bit is set to 1, it is set to 1 by the hardware. The software clears the bit by setting 1 PLL1RDYCLR. 0: No clock ready interrupt caused by PLL1 locked 1: Clock ready interrupt caused by PLL1 locked
5	PLL2RDYFLG	R	PLL2 Ready Interrupt Flag When PLL2 is ready and PLL2RDYEN bit is set to 1, it is set to 1 by the hardware. The software clears the bit by setting 1 PLL2RDYCLR. 0: No clock ready interrupt caused by PLL2 locked 1: Clock ready interrupt caused by PLL2 locked
6	PLL3RDYFLG	R	PLL3 Ready Interrupt Flag When PLL3 is ready and PLL3RDYEN bit is set to 1, it is set to 1 by the hardware. The software clears the bit by setting 1 PLL3RDYCLR. 0: No clock ready interrupt caused by PLL3 locked 1: Clock ready interrupt caused by PLL3 locked
7	CSSFLG	R	Clock Security System Interrupt Flag When the external 3-25MHz oscillator clock fails, it is set to 1 by hardware. The software clears the bit by setting CSSCLR bit. 0: No security system interrupt caused by HSECLK failure 1: Clock security system interrupt is caused by HSECLK failure
8	LSIRDYEN	R/W	LSICLK Ready Interrupt Enable Enable or disable internal 40kHz RC oscillator ready interrupt. 0: Disable 1: Enable
9	LSERDYEN	R/W	LSECLK Ready Interrupt Enable Enable external 32kHz RC oscillator ready interrupt. 0: Disable 1: Enable

Field	Name	R/W	Description
10	HSIRDYEN	R/W	HSICLK Ready Interrupt Enable Enable the internal 8MHz RC oscillator ready interrupt. 0: Disable 1: Enable
11	HSERDYEN	R/W	HSECLK Ready Interrupt Enable Enable external 3-25MHz oscillator ready interrupt. 0: Disable 1: Enable
12	PLL1RDYEN	R/W	PLL1 Ready Interrupt Enable Enable PLL1 ready interrupt. 0: Disable 1: Enable
13	PLL2RDYEN	R/W	PLL2 Ready Interrupt Enable Enable PLL2 ready interrupt. 0: Disable 1: Enable
14	PLL3RDYEN	R/W	PLL3 Ready Interrupt Enable Enable PLL3 ready interrupt. 0: Disable 1: Enable
15	Reserved		
16	LSIRDYCLR	W	LSICLK Ready Interrupt Clear Clear LSICLK ready interrupt flag bit LSIRDYFLG. 0: No effect 1: Clear
17	LSERDYCLR	W	LSECLK Ready Interrupt Clear Clear LSECLK ready interrupt flag bit LSERDYFLG. 0: No effect 1: Clear
18	HSIRDYCLR	W	HSICLK Ready Interrupt Clear Clear HSICLK ready interrupt flag bit HSIRDYFLG. 0: No effect 1: Clear
19	HSERDYCLR	W	HSECLK Ready Interrupt Clear Clear HSECLK ready interrupt flag bit HSERDYFLG. 0: No effect 1: Clear
20	PLL1RDYCLR	W	PLL1 Ready Interrupt Clear Clear PLL1 ready interrupt flag bit PLL1RDYFLG. 0: No effect 1: Clear
21	PLL2RDYCLR	W	PLL2 Ready Interrupt Clear Clear PLL2 ready interrupt flag bit PLL2RDYFLG. 0: No effect 1: Clear

Field	Name	R/W	Description
22	PLL3RDYCLR	W	PLL3 Ready Interrupt Clear Clear PLL3 ready interrupt flag bit PLL3RDYFLG. 0: No effect 1: Clear
23	CSSCLR	W	Clock Security System Interrupt Clear Clear the security system interrupt flag bit CSSFLG. 0: No effect 1: Clear
31:24	Reserved		

4.5.4 APB2 peripheral reset register (RCM_APB2RST)

Offset address: 0x0C

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

All bits can be reset or cleared by software.

Field	Name	R/W	Description
0	AFIORST	R/W	Alternate Function I/O Reset 0: No effect 1: Reset
1	Reserved		
2	PARST	R/W	IO Port A Reset 0: No effect 1: Reset
3	PBRST	R/W	IO Port B Reset 0: No effect 1: Reset
4	PCRST	R/W	IO Port C Reset 0: No effect 1: Reset
5	PDRST	R/W	IO Port D Reset 0: No effect 1: Reset
6	PERST	R/W	IO Port E Reset 0: No effect 1: Reset
8:7	Reserved		
9	ADC1RST	R/W	ADC1 Reset 0: No effect 1: Reset
10	ADC2RST	R/W	ADC2 Reset 0: No effect 1: Reset

Field	Name	R/W	Description
11	TMR1RST	R/W	TMR1 Timer Reset 0: No effect 1: Reset
12	SPI1RST	R/W	SPI1 Reset 0: No effect 1: Reset
13	Reserved		
14	USART1RST	R/W	USART1 Reset 0: No effect 1: Reset
31:15	Reserved		

4.5.5 APB1 peripheral reset register (RCM_APB1RST)

Offset address: 0x10

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle

Field	Name	R/W	Description
0	TMR2RST	R/W	Timer 2 Reset 0: No effect 1: Reset
1	TMR3RST	R/W	Timer 3 Reset 0: No effect 1: Reset
2	TMR4RST	R/W	Timer 4 Reset Set 1 or clear 0 by software 0: No effect 1: Reset
3	TMR5RST	R/W	Timer 5 Reset 0: No effect 1: Reset
4	TMR6RST	R/W	Timer 6 Reset 0: No effect 1: Reset
5	TMR7RST	R/W	Timer 7 Reset 0: No effect 1: Reset
10:6	Reserved		
11	WWDTRST	R/W	Window Watchdog Reset 0: No effect 1: Reset
13:12	Reserved		

Field	Name	R/W	Description
14	SPI2RST	R/W	SPI2 Reset 0: No effect 1: Reset
15	SPI3RST	R/W	SPI3 Reset 0: No effect 1: Reset
16	Reserved		
17	USART2RST	R/W	USART2 Reset 0: No effect 1: Reset
18	USART3RST	R/W	USART3 Reset 0: No effect 1: Reset
19	UART4RST	R/W	UART4 Reset 0: No effect 1: Reset
20	UART5RST	R/W	UART5 Reset 0: No effect 1: Reset
21	I2C1RST	R/W	I2C1 Reset 0: No effect 1: Reset
22	I2C2RST	R/W	I2C2 Reset 0: No effect 1: Reset
24:23	Reserved		
25	CAN1RST	R/W	CAN1 Reset 0: No effect 1: Reset
26	CAN2RST	R/W	CAN2 Reset 0: No effect 1: Reset
27	BAKPRST	R/W	Backup Interface Reset 0: No effect 1: Reset
28	PMURST	R/W	Power Interface Reset 0: No effect 1: Reset
29	DACRST	R/W	DAC Reset 0: No effect 1: Reset
31:30	Reserved		

4.5.6 AHB peripheral clock enable register (RCM_AHBCLKEN)

Offset address: 0x14

Reset value: 0x0000 0014

Access: Access in the form of word, half word and byte, without wait cycle

All bits can be reset or cleared by software.

Note: When the peripheral clock is not enabled, the software cannot read the value of the peripheral register, and the value returned is always 0x0.

Field	Name	R/W	Description
0	DMA1EN	R/W	DMA1 Clock Enable 0: Disable 1: Enable
1	DMA2EN	R/W	DMA2 Clock Enable 0: Disable 1: Enable
2	SRAMEN	R/W	SRAM Interface Clock Enable Enable SRAM clock in sleep mode. 0: Disable 1: Enable
3	Reserved		
4	FMCEN	R/W	FMC Clock Enable Enable the flash interface circuit clock in sleep mode. 0: Disable 1: Enable
5	Reserved		
6	CRCEN	R/W	CRC Clock Enable 0: Disable 1: Enable
11:7	Reserved		
12	OTGFSEN	R/W	OTG_FS Clock Enable 0: Disable 1: Enable
13	Reserved		
14	MACEN	R/W	Ethernet MAC Clock Enable 0: Disable 1: Enable
15	MACTXEN	R/W	Ethernet MAC TX Clock Enable 0: Disable 1: Enable
16	MACRXEN	R/W	Ethernet MAC RX Clock Enable 0: Disable 1: Enable
31:17	Reserved		

4.5.7 APB2 peripheral clock enable register (RCM_APB2CLKEN)

Offset address: 0x18

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte

Usually there is no access waiting cycle. However, when the peripheral on the APB2 bus is accessed, the waiting state will be inserted until the APB2 peripheral access ends.

All bits can be reset or cleared by software.

Note: When the peripheral clock is not enabled, the software cannot read the value of the peripheral register, and the value returned is always 0x0.

Field	Name	R/W	Description
0	AFIOEN	R/W	Alternate Function I/O Clock Enable 0: Disable 1: Enable
1	Reserved		
2	PAEN	R/W	I/O Port A Clock Enable 0: Disable 1: Enable
3	PBEN	R/W	I/O Port B Clock Enable 0: Disable 1: Enable
4	PCEN	R/W	I/O Port C Clock Enable 0: Disable 1: Enable
5	PDEN	R/W	I/O Port D Clock Enable 0: Disable 1: Enable
6	PEEN	R/W	I/O Port E Clock Enable 0: Disable 1: Enable
8:7	Reserved		
9	ADC1EN	R/W	ADC 1 Interface Clock Enable 0: Disable 1: Enable
10	ADC2EN	R/W	ADC 2 Interface Clock Enable 0: Disable 1: Enable
11	TMR1EN	R/W	TMR1 Timer Clock Enable 0: Disable 1: Enable
12	SPI1EN	R/W	SPI 1 Clock Enable 0: Disable 1: Enable
13	Reserved		

Field	Name	R/W	Description
14	USART1EN	R/W	USART1 Clock Enable 0: Disable 1: Enable
31:15	Reserved		

4.5.8 APB1 peripheral clock enable register (RCM_APB1CLKEN)

Offset address: 0x1C

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte

Usually there is no access waiting cycle. However, when the peripheral on the APB1 bus is accessed, the waiting state will be inserted until the APB1 peripheral access ends.

All bits can be reset or cleared by software.

Note: When the peripheral clock is not enabled, the software cannot read the value of the peripheral register, and the value returned is always 0x0.

Field	Name	R/W	Description
0	TMR2EN	R/W	Timer 2 Clock Enable 0: Disable 1: Enable
1	TMR3EN	R/W	Timer 3 Clock Enable 0: Disable 1: Enable
2	TMR4EN	R/W	Timer 4 Clock Enable 0: Disable 1: Enable
3	TMR5EN	R/W	Timer 5 Clock Enable 0: Disable 1: Enable
4	TMR6EN	R/W	Timer 6 Clock Enable 0: Disable 1: Enable
5	TMR7EN	R/W	Timer 7 Clock Enable 0: Disable 1: Enable
10:6	Reserved		
11	WWDTEN	R/W	Window Watchdog Clock Enable 0: Disable 1: Enable
13:12	Reserved		
14	SPI2EN	R/W	SPI 2 Clock Enable 0: Disable 1: Enable

Field	Name	R/W	Description
15	SPI3EN	R/W	SPI 3 Clock Enable 0: Disable 1: Enable
16	Reserved		
17	USART2EN	R/W	USART 2 Clock Enable 0: Disable 1: Enable
18	USART3EN	R/W	USART 3 Clock Enable 0: Disable 1: Enable
19	UART4EN	R/W	UART 4 Clock Enable 0: Disable 1: Enable
20	UART5EN	R/W	UART 5 Clock Enable 0: Disable 1: Enable
21	I2C1EN	R/W	I2C1/3 Clock Enable 0: Disable 1: Enable
22	I2C2EN	R/W	I2C2/4 Clock Enable 0: Disable 1: Enable
24:23	Reserved		
25	CAN1EN	R/W	CAN1 Clock Enable 0: Disable 1: Enable
26	CAN2EN	R/W	CAN2 Clock Enable 0: Disable 1: Enable
27	BAKPEN	R/W	Backup Interface Clock Enable 0: Disable 1: Enable
28	PMUEN	R/W	Power Interface Clock Enable 0: Disable 1: Enable
29	DACEN	R/W	DAC Interface Clock Enable 0: Disable 1: Enable
31:30	Reserved		

4.5.9 Backup domain control register (RCM_BDCTRL)

Offset address: 0x20

Reset value: 0x0000 0000, which can be reset effectively only by backup domain

Access: Access in the form of word, half word and byte, with 0 to 3 wait cycles When the register is accessed continuously, the waiting state will be inserted.
Note: Only when BPWEN bit in PMU_CTRL is set to 1, can LSEEN, LSEBCFG, RTCSRCSEL and RTCCLKEN be changed.

Field	Name	R/W	Description
0	LSEEN	R/W	Low-Speed External Clock Enable 0: Disable 1: Enable
1	LSERDYFLG	R	Low-Speed External Oscillator Oscillator Ready Flag When LSECLK is stable, this bit is set to 1 by hardware, and when it is unstable, it is cleared by hardware. This bit is cleared after 6 external low speed oscillator clock cycles after the LSEEN bit is cleared. 0: Not ready 1. Ready
2	LSEBCFG	R/W	Low-Speed External Clock Bypass Mode Configure Bypass mode refers to the mode in which external clock is used as the LSECLK clock source; otherwise the resonator is used as the LSECLK clock source. 0: Non-bypass mode 1: Bypass mode
7:3	Reserved		
9:8	RTCSRCSEL	R/W	RTC Clock Source Select First set the BDRST bit to reset the backup domain, and then select the RTC clock source. It is impossible to directly configure the register to modify. 00: No clock 01: LSECLK oscillator is used as RTC clock 10: LSICLK oscillator is used as RTC clock 11: HSECLK oscillator is used as RTC clock after being divided by 128
14:10	Reserved		
15	RTCCLKEN	R/W	RTC Clock Enable 0: Disable 1: Enable
16	BDRST	R/W	Backup Domain Software Reset Set 1 or clear 0 by software 0: Reset is not activated 1: Reset the whole backup domain
31:17	Reserved		

4.5.10 Control/State register (RCM_CSTS)

Offset address: 0x24

Reset value: 0x0C00 0000, except reset flag, all are cleared by system reset, and reset flag can only be cleared by power reset.

Access: Access in the form of word, half word and byte, with 0 to 3 wait cycles. When the register is accessed continuously, the waiting state will be inserted.

Field	Name	R/W	Description
0	LSIEN	R/W	Low-Speed Internal Oscillator Enable Set 1 or clear 0 by software. 0: Disable 1: Enable
1	LSIRDYFLG	R	Low-Speed Internal Oscillator Ready Flag When LSICLK is stable, this bit is set to 1 by hardware, and when it is unstable, it is cleared by hardware. This bit is cleared after 3 internal RC oscillator clock cycles after the LSIEN bit is cleared. 0: Not ready 1. Ready
23:2	Reserved		
24	RSTFLGCLR	R/W	Reset Flag Clear The reset flag is cleared by setting to 1 by software, including RSTFLGCLR. 0: No effect 1: Clear the reset flag
25	Reserved		
26	NRSTFLG	R/W	NRST PIN Reset Occur Flag When NRST pin is reset, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit. 0: No NRST pin reset occured 1: NRST pin reset occurred
27	PODRSTFLG	R/W	POR/PDR Reset Occur Flag This bit can be set to 1 by hardware; and cleared by software by writing RSTFLGCLR bit. 0: No power-on/power-down reset occurs 1: Power-on/power-down reset occurs
28	SWRSTFLG	R/W	Software Reset Occur Flag This bit can be set to 1 by hardware; and cleared by software by writing RSTFLGCLR bit. 0: No occurrence 1: Occurred
29	IWDTRSTFLG	R/W	Independent Watchdog Reset Occur Flag When independent watchdog reset occurs in V_{DD} area, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit. 0: No occurrence 1: Occurred
30	WWDTRSTFLG	R/W	Window Watchdog Reset Occur Flag When window watchdog is reset, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit. 0: No occurrence 1: Occurred

Field	Name	R/W	Description
31	LPWRRSTFLG	R/W	Low Power Reset Occur Flag When low-power management is reset, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit. 0: No occurrence 1: Occurred

4.5.11 AHB peripheral reset register (RCM_AHBRST)

Offset address: 0x28

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

Field	Name	R/W	Description
11:0	Reserved		
12	OTGFSRST	R/W	OTG_FS Reset 0: No effect 1: Reset
13	Reserved		
14	MACRST	R/W	Ethernet MAC Reset 0: No effect 1: Reset
31:15	Reserved		

4.5.12 Clock configuration register2 (RCM_CFG2)

Offset address: 0x2C

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

Field	Name	R/W	Description
3:0	PLLPSC1	R/W	PLLPSC1 Factor Configure 0000: No division factor 0001: Factor is 2 0010: Factor is 3 0011: Factor is 4 0100: Factor is 5 0101: Factor is 6 0110: Factor is 7 0111: Factor is 8 1000: Factor is 9 1001: Factor is 10 1010: Factor is 11 1011: Factor is 12 1100: Factor is 13 1101: Factor is 14 1110: Factor is 15 1111: Factor is 16 Note: These bits could be set only when PLL1 is disabld.

Field	Name	R/W	Description
7:4	PLLPSC2	R/W	PLLPSC2 Factor Configure 0000: No division factor 0001: Factor is 2 0010: Factor is 3 0011: Factor is 4 0100: Factor is 5 0101: Factor is 6 0110: Factor is 7 0111: Factor is 8 1000: Factor is 9 1001: Factor is 10 1010: Factor is 11 1011: Factor is 12 1100: Factor is 13 1101: Factor is 14 1110: Factor is 15 1111: Factor is 16 Note: These bits could be set only when both PLL2 and PLL3 are disabld.
11:8	PLL2MUL	R/W	PLL2 Multiplication Factor 00xx: Reserved 010x: Reserved 0110: Factor is 8 0111: Factor is 9 1000: Factor is 10 1001: Factor is 11 1010: Factor is 12 1011: Factor is 13 1100: Factor is 14 1101: Reserved 1110: Factor is 16 1111: Factor is 20 Note: These bits could be configured only when the PLL2 is disabled.
15:12	PLL3MUL	R/W	PLL3 Multiplication Factor 00xx: Reserved 010x: Reserved 0110: Factor is 8 0111: Factor is 9 1000: Factor is 10 1001: Factor is 11 1010: Factor is 12 1011: Factor is 13 1100: Factor is 14 1101: Reserved 1110: Factor is 16 1111: Factor is 20

Field	Name	R/W	Description
			Note: These bits could be configured only when the PLL3 is disabled.
16	PLLPSC1SRC	R/W	PLLPSC1 Clock Sourse Select 0: HSECLK is selected as clock source 1: PLL2CLK is selected as clock source Note: This bit could be configured only when the PLL1 is disabled.
17	I2S2SRCSEL	R/W	I2S2 Clock Sourse Select 0: SYSCLK is selected as clock source 1: DPLL3CLK is selected as clock source
18	I2S3SRCSEL	R/W	I2S3 Clock Sourse Select 0: SYSCLK is selected as clock source 1: DPLL3CLK is selected as clock source
31:19	Reserved		

5 Power Management Unit (PMU)

5.1 Full Name and Abbreviation Description of Terms

Table 17 Full Name and Abbreviation Description of Terms

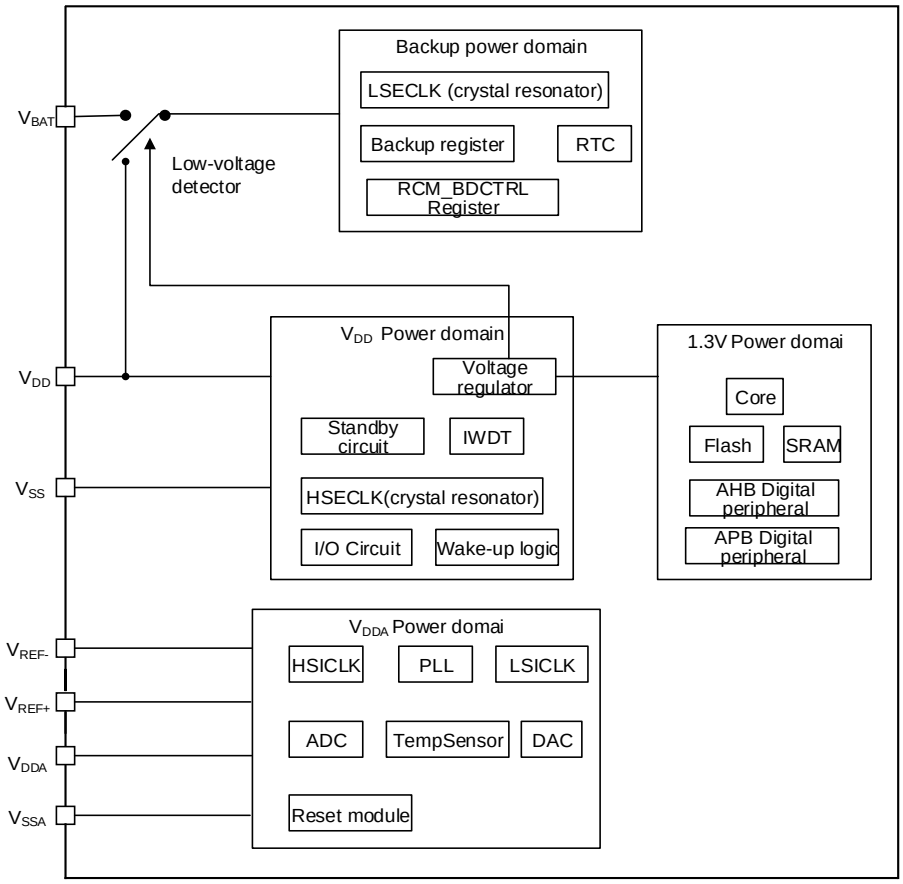
Full name in English	English abbreviation
Power Management Unit	PMU
Power On Reset	POR
Power Down Reset	PDR
Power Voltage Detector	PVD

5.2 Introduction

The power supply is the basis for stable operation of a system. The working voltage is 2.0~3.6V. It can provide 1.3V power supply through the built-in voltage regulator. If the main power V_{DD} is powered down, it can supply power to the backup power supply area through V_{BAT}.

5.3 Structure Block Diagram

Figure 5 Power Supply Control Structure Block Diagram



5.4 Functional Description

5.4.1 Power Domain

The power domain of the product includes: V_{DD} power domain, V_{DDA} power domain, 1.3 power domain and backup power domain.

5.4.1.1 V_{DD} power domain

Power supply is provided through V_{DD}/V_{SS} pins to power the voltage regulator, standby circuit, IWDT, HSECLK, I/O (except PC13, PC14, PC15 pins) and wake-up logic.

Voltage regulator

Power can be supplied to 1.3V power domain in the following operating modes:

- Normal mode: In this mode, 1.3V power supply area runs at full power
- Stop mode: In this mode, 1.3V power supply area works in low power state, all clocks are off, and peripherals stop work

- Standby mode: In this mode, the 1.3V power supply area stops power supply, and Except for backup circuits, the content of register and SRAM will be lost

5.4.1.2 V_{DDA} power domain

Power the ADC, DAC, HSICLK, LSICLK, TempSensor, PLL and reset module through VDDA/VSSA and VREF+/VREF- pins.

Independent ADC power supply and reference voltage

Independent ADC power supply can improve conversion accuracy, and the specific power pins are as follows:

- V_{DDA}: Power pin of ADC
- V_{SSA}: Independent power ground pin
- V_{REF+}/V_{REF-}: ADC reference voltage pin

5.4.1.3 1.3V power domain

The core, Flash, SRAM and digital peripherals are powered by voltage regulator.

5.4.1.4 Backup power domain

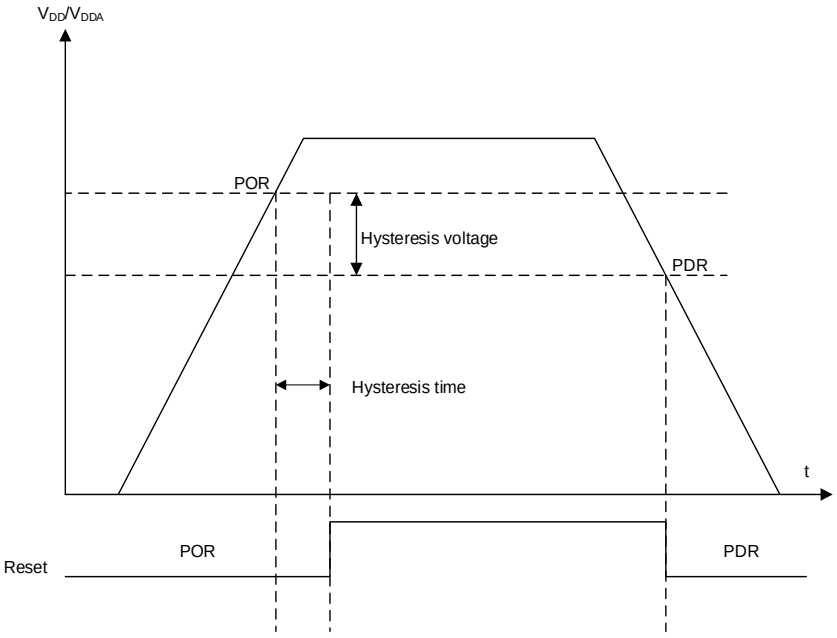
When V_{DD} exists, the backup power supply area is powered by V_{DD}. When V_{DD} is powered down, the backup power supply area is powered by V_{BAT}, which is used to save the content of backup register and maintain RTC function. Power the LSECLK crystal oscillator, RTC, backup register and RCM_BDCTRL register, PC13, PC14 and PC15.

5.4.2 Power Management

5.4.2.1 Power-on/power-down reset (POR and PDR)

When the V_{DD}/V_{DDA} is detected to be lower than the threshold voltage V_{POR} and V_{PDR}, the chip will automatically maintain the reset state. The waveform diagrams of power-on reset and power-down reset are as follows. For POR, PDR, hysteresis voltage and hysteresis time, please refer to the "Datasheet".

Figure 6 Power-on Reset and Power-down Reset Oscillogram



5.4.2.2 Power voltage detector (PVD)

A threshold can be set for PVD to monitor whether V_{DD}/V_{DDA} is higher or lower than the threshold. If interrupt is enabled, the interrupt can be triggered to process VDD/VDDA exceeding the threshold in advance. The usage of PVD is as follows:

（1） Set the PVDEN bit of the configuration register PMU_CTRL to 1 to enable PVD

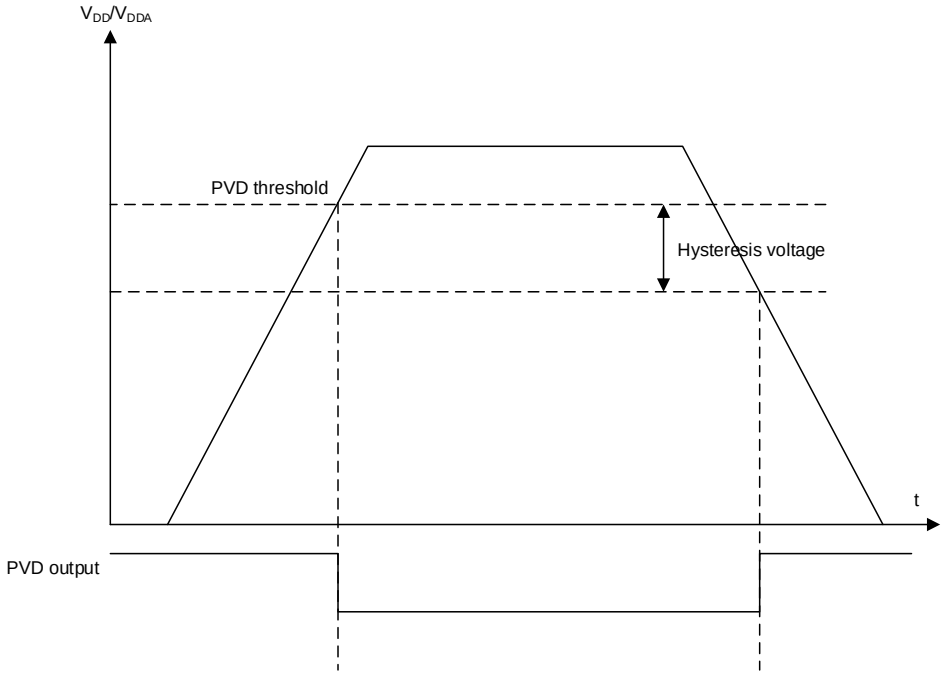
（2） Select the voltage threshold of PVD for the PLSEL [2:0] bit of the configuration register PMU_CTRL

（3） The PVDOFLG bit of the configuration register PMU_CSTS indicates the value of V_{DD} is higher or lower than the threshold of PVD

（4） When it is detected that V_{DD}/V_{DDA} is lower or higher than the threshold of PVD, PVD interrupt will be generated

The threshold waveform of PVD is shown below. Please see "Datasheet" for PVD threshold and hysteresis voltage.

Figure7 PVD Threshold Oscillogram



5.4.3 Power Consumption Control

5.4.3.1 Reduce the power consumption in low-power mode

There are three low-power modes: sleep mode, stop mode and standby mode. The power consumption is reduced by closing the core and clock source and setting the voltage regulator.

The power consumption, wake-up start time, wake-up mode and data storage of each low-power mode are different; the lower the power consumption is, the longer the wake-up time is, the less the wake-up mode is, the less the data saved are after wake-up; users can choose the most appropriate low-power mode according to their needs. The following table shows the difference among three low-power modes.

Table 17 Difference among "Sleep Mode, Stop Mode and Standby Mode"

Mode	Instruction	Entry mode	Wake-up mode	Voltage regulator	Effect on 1.5V area clock	Effect on V_{DD} area clock
Sleep	Arm® Cortex®-M3 core stops, and all peripherals including the core peripheral are still working	Call WFI instruction	Any interrupt	Open	Ony the core clock is turned off and it has no effect on other clocks and ADC clocks	None
		Call WFE instruction	Wake-up event	Open		None

Mode	Instruction	Entry mode	Wake-up mode	Voltage regulator	Effect on 1.5V area clock	Effect on V_{DD} area clock
Stop	All clocks have stopped	PDDSCFG and LPDSCFG bits +SLEEPDEEP bit +WFI or WFE	Any external interrupt	Turn on or be in low-power mode	Close clocks of all 1.3V areas	The oscillator of HSICLK and HSECLK is turned off
Standby	1.3V power off	PDDSCFG bit +SLEEPDEEP bit +WFI or WFE	Rising edge of WKUP pin, RTC alarm event, external reset on NRST pin, IWDT reset	Off		

Sleep mode

The characteristics of sleep mode are shown in the table below

Table 19 Characteristics of Sleep Mode

Characteristics	Instruction
Enter	Enter the sleep mode immediately by executing WFI or WFE instructions; When SLEEPONEINT is set to 0 and WFI or WFE instruction is executed, the system will enter the sleep mode immediately; when SLEEPONEINT is set to 1, the system will exit the interrupt program and then enter the sleep mode immediately.
Wake-up	If WFI instruction is executed to enter the sleep mode, wake up by any interrupt; If WFE instruction is executed to enter the sleep mode, wake up through an event.
Sleep	The core stops working, all peripherals are still running, and the data in the core registers and memory before sleep are saved.
Wake-up delay	None
After wake-up	If the system is woken up by interrupt, it will first enter the interrupt, then exit the interrupt, and then execute the program after WFI instruction. If the system is woken up by event, it will directly execute the program after WFE instruction.

Stop mode

The characteristics of stop mode are shown in the table below:

Table 18 Characteristics of Stop Mode

Characteristics	Instruction
Enter	SLEEPDEEP bit of the core register is set to 1, PDDSCFG bit of the register PMU_CTRL is set to 0, and when executing WFI or WFE instruction, the system will enter the stop mode immediately; When LPDSCFG bit of the register PMU_CTRL is set to 0, the voltage regulator is working in normal mode; when LPDSCFG bit of the register PMU_CTRL is set to 1, the voltage regulator is working in low-power mode.

Characteristics	Instruction
Wake-up	If WFI instruction is executed to enter the sleep mode, wake up by any interrupt; If WFE instruction is executed to enter the sleep mode, wake up through an event.
Stop	The core will stop working, the peripheral will stop working, and the data in the core register and memory before stop will be saved.
Wake-up delay	HSICLK oscillator wake-up time + voltage regulator wake-up time from low-power mode.
After wake-up	If the system is woken up by interrupt, it will first enter the interrupt, then exit the interrupt, and then execute the program after WFI instruction. If the system is woken up by event, it will directly execute the program after WFE instruction.

Standby mode

The characteristics of standby mode are shown in the table below:

Table 19 Standby Mode

Characteristics	Instruction
Enter	SLEEPDEEP bit of the core register is set to 1, PDDSCFG bit of the register PMU_CTRL is set to 1, WUEFLG bit is set to 0 and when executing WFI or WFE instruction, the system will enter the standby mode immediately.
Wake-up	Wake up by rising edge of WKUP pin, RTC alarm, wake-up, tamper event or NRST pin external reset and IWDT reset.
Standby	The core will stop working, the peripheral will stop working, and the data in the core register and memory will be lost.
Wake-up delay	Chip reset time.
After wake-up	The program starts executing from the beginning.

5.4.3.2 Reduce the power consumption in run mode

In the run mode, the power consumption can be reduced by reducing the system clock, closing or reducing the peripheral clock on the APB/AHB bus.

5.5 Register Address Mapping

Table 20 PMU Register Address Mapping Table

Register name	Description	Offset address
PMU_CTRL	Power control register	0x00
PMU_CSTS	Power control/state register	0x04

5.6 Register Functional Description

5.6.1 Power control register (PMU_CTRL)

Offset address: 0x00

Reset value: 0x0000 0000 (cleared when waking up from standby mode)

Field	Name	R/W	Description
0	LPDSCFG	R/W	Low Power Deepsleep Configure Configure the working state of the voltage regulator in stop mode. 0: Enable 1: Low-power mode
1	PDDSCFG	R/W	Power Down Deep Sleep Configure When the CPU enters deep sleep, configure the voltage regulator state in standby and stop modes. 0: The voltage regulator is controlled by LPDSCFG bit when entering the stop mode 1: Enter standby mode
2	WUFLGCLR	RC_W1	Wakeup Flag Clear 0: Invalid 1: Clear the wake-up flag after 2 system clock cycles by writing 1
3	SBFLGCLR	RC_W1	Standby Flag Clear 0: Invalid 1: Write 1 to clear the standby flag
4	PVDEN	R/W	Power Voltage Detector Enable 0: Disable 1: Enable
7:5	PLSEL	R/W	PVD Level Select 0x0：2.2V 0x1：2.3V 0x2：2.4V 0x3：2.5V 0x4：2.6V 0x5：2.7V 0x6：2.8V 0x7：2.9V Note: See "Datasheet" for detailed instructions
8	BPWEN	R/W	Backup Domain Write Access Enable Backup area refers to RTC and backup register; write access is disabled after reset, and is allowed after writing 1. 0: Write is disabe 1: Write is enable
31:9	Reserved		

5.6.2 Power control/state register (PMU_CSTS)

Offset address: 0x04

Reset value: 0x0000 0000 (not cleared when waking up from standby mode)

Compared with the standard APB read, it requires extra APB cycle to read this register

Field	Name	R/W	Description
0	WUEFLG	R	Wakeup Event Flag This bit is set by hardware, indicating whether wake-up event or RTC alarm wake-up event occurs on WKUP pin 0: Not occur

Field	Name	R/W	Description
			1: Occurred Note: Enable the WKUP pin, and an event will be detected when the WKUP pin is at high level.
1	SBFLG	R	Standby Flag This bit is set to 1 by hardware, and can only be cleared by POR/PDR (power-on/power-down reset) or by setting the SBFLGCLR bit of the power supply control register (PMU_CTRL). 0: Not enter the standby mode 1: Have entered the standby mode
2	PVDOFLG	R	PVD Output Flag Indicate whether VDD/VDDA is higher than the PVD threshold selected by PLSEL [2:0] This bit is valid only when PVD is enabled by PVDEN bit. 0: V_{DD}/V_{DDA} higher than PVD threshold 1: V_{DD}/V_{DDA} lower than PVD threshold Note: This bit is 0 after reset or when entering the standby mode (PVD stops work).
7:3	Reserved		
8	WKUPCFG	R/W	WKUP Pin Configure When WKUP is used as a normal I/O, the event on WKUP pin cannot wake up the CPU in standby mode; it can wake up CPU only when it is not used as a normal I/O. 0: Configure normal I/O 1: Can wake MCU Note: Clear this bit in system reset
31:9	Reserved		

6 Backup Register (BAKPR)

6.1 Introduction

The backup register can be used to store 84 bytes of data, including 42 16-bit registers. When V_{DD} is closed, the backup domain will be maintained power-on by V_{BAT}.

Wake up the system in standby mode. If the system is reset or the power supply is reset, the backup register will not be reset. BAKPR control register manages tamper detection and RTC check.

After BAKP is reset, access to the backup register and RTC will be disabled, and the backup domain (BAKPR) will be protected from possible accidental write access. If you want to re-enable the access to the backup register and RTC, operate according to the following steps:

- Enable the power supply and backup interface clock by setting PMU and BAKP bits in RCM_APB1CLKEN register
- Enable the access to the backup register and RTC by setting BPWEN bit in PMU_CTRL power control register

6.2 Main Characteristics

（1） 84-byte data register

（2） The state/control register is used to manage the tamper detection pull-up input with interrupt function

（3） Clock Calibration Register, which can store RTC calibration value

（4） Output the RTC calibration clock, RTC alarm pulse or second pulse on tamper pin PC13 (TAMPER) (when the pin is not used for tamper detection)

6.3 Functional Description

6.3.1 Intrusion Detection

Judge whether tamper event is generated according to whether the signal on the TAMPER pin changes. Intrusion detection event can reset all data backup registers. In order to avoid the loss of tamper events, detect the signal and also detect the edge detection signal and tamper detection enable bit so that the tamper events before detection can be detected. When the TPALCFG bit is set, if the tamper pin is already at an effective level before enabling, an additional tamper event will be generated after the tamper pin is enabled. If TPIEN bit of BAKPR_CSTS register is also set, an interrupt will be generated when an

tamper detection event occurs.

Disable the tamper pin after a tamper event is detected and cleared. If you want to re-enable the tamper detection function, to avoid that there is still intrusion tamper event on tamper pin when the software writes backup data BAKPR_DATAx register, it is required to set TPFCFG bit of BAKPR_CTRL register (equivalent to tamper pin detection) before writing the backup data BAKPR_DATAx register.

Note: The tamper detection is still active when V_{DD} is powered off. The tamper pin should be externally connected to the correct level to prevent the reset data backup register from being reset.

6.3.2 RTC Calibration

Enable RTC calibration by configuring the CALCOEN bit of RTC clock calibration BAKPR_CLKCAL register.

RTC clock can be output to the tamper pin through 64 divided frequency.

6.4 Register Address Mapping

Table 21 BAKPR Register Address Mapping

Register name	Description	Offset address
BAKPR_DATAx(x=1..10)	Backup data register 1	0x04+4(x-1)
BAKPR_CLKCAL	RTC clock calibration register	0x2C
BAKPR_CTRL	Backup control register	0x30
BAKPR_CSTS	Backup control/state register	0x34
BAKPR_DATAx(x=11…42)	Backup data register 11	0x40+4(x-1)

6.5 Register Functional Description

Peripheral registers can be accessed by half word (16 bits) or word (32 bits).

6.5.1 Backup data register x (BAKPR_DATAx) (x=1…10, 11…42)

Offset address: From 0x04 to 0x28, from 0x40 to 0xBC

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	DATA	R/W	User Backup Data In the presence of V_{BAT} power supply, BAKPR_DATAx register cannot be reset through power reset, system reset and standby mode wake-up reset, and can only be reset by resetting the backup domain or tamper event.

6.5.2 RTC clock calibration register (BAKPR_CLKCAL)

Offset address: 0x2C

Reset value: 0x0000 0000

Field	Name	R/W	Description
6:0	CALVALUE	R/W	Calibration Value Setup Reduce RTC clock by skipping the clock pulse count of RTC, to realize calibration. This value indicates the pulse count of multiple clocks that will be ignored every 2^{20} clock pulses, which can be slowed down from 0 to 121ppm.
7	CALCOEN	R/W	Calibration Clock Output Enable 0: No output 1: For the RTC clock after the tamper pin outputs 64 divided frequency, if LSECLK is 32.768KHz, the output signal frequency is 512Hz. When the CALCOEN bit is set, the tamper detection function needs to be disabled to avoid unnecessary tamper signal detected. Note: This bit will be cleared when V_{DD} is powered off.
8	ASPOEN	R/W	Alarm or Second Pulse Output Enable 0: Disable 1: Output RTC entry alarm or second pulse signal on tamper pin The duration of output pulse is 1 RTC clock cycle; when setting the ASPOEN bit, the tamper detection function should be disabled. Note: This bit can be clered only by backup domain reset.
9	ASPOSEL	R/W	Alarm or Second Pulse Output Select This bit can select the tamper pin to output RTC second pulse signal or alarm pulse signal 0: Output RTC alarm pulse 1: Output RTC second pulse Note: This bit can be cleared only by backup domain reset.
31:10	Reserved		

6.5.3 Backup control register (BAKPR_CTRL)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TPFCFG	R/W	TAMPER Pin Function Configure 0: Tamper pin is used as general-purpose IO port 1: Tamper pin multiplexing for tamper detection
1	TPALCFG	R/W	TAMPER Pin Active Level Configure Select the effective level detected by the tamper pin to reset all the data backup registers. 0: High level 1: Low level
31:2	Reserved		

Note: Setting TPALCFG and TPFCFG bits at the same time is always secure. However, a false tamper event will be generated if both are cleared at the same time. Therefore, it is recommended to change the state of TPALCFG bit only when TPFCFG is 0.

6.5.4 Backup control/state register (BAKPR_CSTS)

Offset address: 0x34

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TECLR	W	Tamper Event Flag Clear This bit is write-only, and the read-out value is 0 0: Invalid 1: Clear the tamper detection event flag and reset the tamper detection function
1	TICLR	W	Tamper Interrupt Flag Clear This bit is write-only, and the read-out value is 0 0: Invalid 1: Clear the tamper detection interrupt and interrupt flag
2	TPIEN	R/W	TAMPER Pin Interrupt Enable This bit is reset only after system reset or wake-up from standby mode. Tamper interrupt cannot wake up the system core in low-power mode. 0: Disable 1: Enable (TPFCFG bit must be set)
7:3	Reserved		
8	TEFLG	R	TAMPER Event Occur Flag This bit is set by hardware when a tamper event is detected and it can be cleared by writing 1 to TECLR bit 0: No tamper event 1: Tamper event detected Note: The tamper event can reset all backup data registers. If the bit is 1, all backup data registers will remain reset, and the backup data cannot be written successfully.
9	TIFLG	R	TAMPER Interrupt Occur Flag When the TPIEN bit is set and a tamper event is detected, this bit is set by hardware and cleared by writing 1 to the TICLR bit; this bit is reset only after the system is reset or woken up from standby mode. 0: No tamper interrupt 1: Tamper interrupt occurred
31:10	Reserved		

7 Nested Vector Interrupt Controller (NVIC)

7.1 Full Name and Abbreviation Description of Terms

Table 24 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Non Maskable Interrupt	NMI

7.2 Introduction

The Cortex-M3 core in the product integrates nested vectored interrupt controller (NVIC), which is closely coupled with the core, and can handle exceptions and interrupts and power management control efficiently and with low delay. Please see *Cortex-M3 Technical Reference Manual* for more instructions about NVIC.

7.3 Main Characteristics

（1） 68 maskable interrupt channels (excluding 16 Arm® Cortex®-M3 interrupt lines)

（2） 16 programmable priority levels (use 4-bit interrupt priority level)

（3） Low-delay exception and interrupt processing

（4） Power management control

（5） Realization of system control register

7.4 Interrupt and Exception Vector Table

Table 22 APM32F107 105xx Interrupt and Exception Vector Table

Exception type	Vector No.	Priority	Vector address	Description
-	-	-	0x0000_0000	Reserved
Reset	-	-3	0x0000_0004	Reset
NMI	-	-2	0x0000_0008	Non-maskable interrupt
HardFault	-	-1	0x0000_000C	Various hardware faults
MemManage	-	Can be set	0x0000_0010	Memory management
BusFault	-	Can be set	0x0000_0014	-
UsageFault	-	Can be set	0x0000_0018	-
-	-	-	0x0000_001C- 0x0000_002B	Reserved

Exception type	Vector No.	Priority	Vector address	Description
SVCall	-	Can be set	0x0000_002C	SWI instruction realizes system service revoking
Debug Monitor	-	Can be set	0x0000_0030	Debug monitor
-	-	-	0x0000_0034	Reserved
PendSV	-	Can be set	0x0000_0038	Pending system service request
SysTick	-	Can be set	0x0000_003C	System tick timer
WWDT	0	Can be set	0x0000_0040	Window watchdog interrupt
PVD	1	Can be set	0x0000_0044	Power voltage detection interrupt
TAMPER	2	Can be set	0x0000_0048	Tamper detection interrupt
RTC	3	Can be set	0x0000_004C	RTC interrupt
FLASH	4	Can be set	0x0000_0050	Flash memory global interrupt
RCM	5	Can be set	0x0000_0054	RCM interrupt
EINT0	6	Can be set	0x0000_0058	EINT Line 0 interrupt
EINT1	7	Can be set	0x0000_005C	EINT Line 1 interrupt
EINT2	8	Can be set	0x0000_0060	EINT Line 2 interrupt
EINT3	9	Can be set	0x0000_0064	EINT Line 3 interrupt
EINT4	10	Can be set	0x0000_0068	EINT Line 4 interrupt
DMA1_CH1	11	Can be set	0x0000_006C	DMA1 channel 1 global interrupt
DMA1_CH2	12	Can be set	0x0000_0070	DMA1 channel 2 global interrupt
DMA1_CH3	13	Can be set	0x0000_0074	DMA1 channel 3 global interrupt
DMA1_CH4	14	Can be set	0x0000_0078	DMA1 channel 4 global interrupt
DMA1_CH5	15	Can be set	0x0000_007C	DMA1 channel 5 global interrupt
DMA1_CH6	16	Can be set	0x0000_0080	DMA1 channel 6 global interrupt
DMA1_CH7	17	Can be set	0x0000_0084	DMA1 channel 7 global interrupt
ADC1/2	18	Can be set	0x0000_0088	ADC1 and ADC2 global interrupt
CAN1_TX	19	Can be set	0x0000_008C	CAN1 sending interrupt

Exception type	Vector No.	Priority	Vector address	Description
CAN1_RX0	20	Can be set	0x0000_0090	CAN1 receiving 0 interrupt
CAN1_RX1	21	Can be set	0x0000_0094	CAN1 receiving 1 interrupt
CAN1_SCE	22	Can be set	0x0000_0098	CAN1 SCE interrupt
EINT9_5	23	Can be set	0x0000_009C	EINT line [9:5] interrupt
TMR1_BRK	24	Can be set	0x0000_00A0	TMR1 braking interrupt
TMR1_UP	25	Can be set	0x0000_00A4	TMR1 update interrupt
TMR1_TRG_COM	26	Can be set	0x0000_00A8	TMR1 trigger and communication interrupt
TMR1_CC	27	Can be set	0x0000_00AC	TMR1 capture/compare interrupt
TMR2	28	Can be set	0x0000_00B0	TMR2 interrupt
TMR3	29	Can be set	0x0000_00B4	TMR3 interrupt
TMR4	30	Can be set	0x0000_00B8	TMR4 interrupt
I2C1_EV	31	Can be set	0x0000_00BC	I2C1 event interrupt
I2C1_ER	32	Can be set	0x0000_00C0	I2C1 error interrupt
I2C2_EV	33	Can be set	0x0000_00C4	I2C2 event interrupt
I2C2_ER	34	Can be set	0x0000_00C8	I2C2 error interrupt
SPI1	35	Can be set	0x0000_00CC	SPI1 interrupt
SPI2	36	Can be set	0x0000_00D0	SPI2 interrupt
USART1	37	Can be set	0x0000_00D4	USART1 interrupt
USART2	38	Can be set	0x0000_00D8	USART2 interrupt
USART3	39	Can be set	0x0000_00DC	USART3 interrupt
EINT15_10	40	Can be set	0x0000_00E0	EINT line [15:10] interrupt
RTC_Alarm	41	Can be set	0x0000_00E4	RTC alarm interrupt
OTG_FS_WKUP	42	Can be set	0x0000_00E8	Full-speed USB_OTG wakeup interrupt connected to EINT
-	-	-	0x0000_00EC~0x0000_0104	Reserved
TMR5	50	Can be set	0x0000_0108	TMR5 interrupt
SPI3	51	Can be set	0x0000_010C	SPI3 interrupt
UART4	52	Can be set	0x0000_0110	UART4 interrupt
UART5	53	Can be set	0x0000_0114	UART5 interrupt
TMR6	54	Can be set	0x0000_0118	TMR6 interrupt
TMR7	55	Can be set	0x0000_011C	TMR7 interrupt

Exception type	Vector No.	Priority	Vector address	Description
DMA2_CH1	56	Can be set	0x0000_0120	DMA2 channel 1 interrupt
DMA2_CH2	57	Can be set	0x0000_0124	DMA2 channel 2 interrupt
DMA2_CH3	58	Can be set	0x0000_0128	DMA2 channel 3 interrupt
DMA2_CH4	59	Can be set	0x0000_012C	DMA2 channel 4 interrupt
DMA2_CH5	60	Can be set	0x0000_0130	DMA2 channel 5 interrupt
ETH	61	Can be set	0x0000_0134	Ethernet global interrupt
ETH_WKUP	62	Can be set	0x0000_0138	Ethernet wake up interrupt connected to EINT
CAN2_TX	63	Can be set	0x0000_013C	CAN2 sending interrupt
CAN2_RX0	64	Can be set	0x0000_0140	CAN2 receiving 0 interrupt
CAN2_RX1	65	Can be set	0x0000_0144	CAN2 receiving 1 interrupt
CAN2_SCE	66	Can be set	0x0000_0148	CAN2 SCE interrupt
OTG_FS	67	Can be set	0x0000_014C	Full speed USB_OTG global interrupt

8 External Interrupt/Event Controller (EINT)

8.1 Introduction

The interrupts/events contain internal interrupt/event and external interrupt/event. In this manual, external interrupt refers to the interrupt/event caused by I/O pin input signal, which is EINTx in interrupt vector table; other interrupts are internal interrupts/events.

The events can be divided into hardware events and software events. Hardware events are generated by external/core hardware signals, while software events are generated by instructions.

Interrupts need to go through the interrupt handler function to realize the work to be processed, while events do not need to go through interrupt handler function, and the preset work can be triggered by hardware. For example, the external event is to generate GPIO output pulse, and the internal event is the update event of one TMR to trigger another TMR to work.

8.2 Main Characteristics

（1） Support 20 event/interrupt requests

（2） Each event/interrupt line can be masked independently

（3） Each external event/interrupt line can be triggered independently

（4） Each external interrupt line has dedicated state bit

（5） Detects external signals whose pulse width is lower than the APB2 clock width

8.3 Functional Description

8.3.1 "External Interrupt and Event" Classification and Difference Points

"External interrupt and event" can be classified into external hardware interrupt, external hardware event, external software event and external software interrupt according to trigger source, configuration and execution process. The difference points are shown in the table below:

Table 23 "External Interrupt and Event" Classification and Difference Points

Name	Trigger source	Configuration and execution process
External hardware interrupt	External signal	(1) Set the trigger mode, allow the interrupt request, and enable corresponding peripheral interrupt line (enable in NVIC); (2) When an edge consistent with the configuration is generated on the external interrupt line, an interrupt request will be generated, and the corresponding suspend bit will be set to 1. Write 1 to the corresponding bit of the pending register and the interrupt request will be cleared.
External hardware event	External signal	(1) Set the trigger mode and enable the event line; (2) When an edge consistent with the configuration is generated on the external interrupt line, one event request pulse will be generated, and the corresponding pending bit will not be set to 1.
External software event	Software interrupt register/transmission event (SEV) instruction	(1) Enable the event line; (2) Write 1 to the software interrupt event register of the corresponding event line to generate an event request pulse, and the corresponding pending bit will not be set to 1.
External software interrupt	Software interrupt register	(1) Allow interrupt request, and enable the corresponding peripheral interrupt line (enable in NVIC); (2) Write 1 to the software interrupt event register of the corresponding event line to generate an interrupt request, the corresponding pending bit will be set to 1; write 1 to the corresponding bit of the pending register and the interrupt request will be cleared.

8.3.2 Core Wake-up

Using WFI and WFE instructions can make the core stop working. When WFI instruction is used, any interrupt can wake up the core; when WFE instruction is used, the core can be wakened up by event.

When interrupt is used for wake-up, the interrupt handler function will be triggered, and normal interrupt configuration can wake up the core. When an event is used to wake up the core, the interrupt handler function will not be triggered, which will reduce the wake-up time, and the configuration method is:

（1） It can trigger an internal interrupt (internal hardware event) but cannot trigger the interrupt handler function for wake-up

- It can enable an internal interrupt in the peripheral, but cannot enable the corresponding interrupt in NVIC to avoid triggering the interrupt handler function
- Enable SEVONPEND bit in the system controller of the core, and execute WFE instruction to make the core enter sleep mode

- Generate an interrupt to wake up the core; when the core recovers from WFE, it is required to clear the pending bit of corresponding peripheral interrupt and the pending bit of peripheral NVIC interrupt channel (clear the pending register in the NVIC interrupt)

（2） Wake up through EINT line events (external hardware event)
- Configure EINT line as the event mode
- Execute WFE instruction to make the core enter the sleep mode
- Generate an interrupt to wake up the core; when the CPU recovers from WFE, since the pending bit of corresponding event line is not set, it is unnecessary to clear the interrupt pending bit of corresponding peripheral or the NVIC interrupt channel pending bit

8.3.2.1 Event wake-up

It can trigger an internal interrupt (internal hardware event) but cannot trigger the interrupt handler function for wake-up

（1） Enable an internal interrupt in the peripheral, but do not enable the corresponding interrupt in NVIC to avoid triggering the interrupt handler function;

（2） Enable SEVONPEND bit in the system controller of the core, and execute WFE instruction to make the core enter sleep mode;

（3） Generate an interrupt to wake up the core; when the core recovers from WFE, it is required to clear the pending bit of corresponding peripheral interrupt and the pending bit of peripheral NVIC interrupt channel (clear the pending register in the NVIC interrupt).

Wake up through EINT line events (external hardware event)

（1） Configure EINT line as the event mode;

（2） Execute WFE instruction to make the core enter the sleep mode;

（3） Generate an interrupt to wake up the core; when the CPU recovers from WFE, since the pending bit of corresponding event line is not set, it is unnecessary to clear the interrupt pending bit of corresponding peripheral or the NVIC interrupt channel pending bit.

8.3.3 External Interrupt and Event Line Mapping

Table 24 External Interrupt and Event Line Mapping

External Interrupt and Event Channel Name	External Interrupt and Event Line No.
PA0/PB0/PC0/PE0/PF0/PG0	EINT 0
PA1/PB1/PC1/PE1/PF1/PG1	EINT 1
…	…
PA15/PB15/PC15/PE15/PF15/PG15	EINT 15
PVD output	EINT 16
RTC Alarm event	EINT 17

External Interrupt and Event Channel Name	External Interrupt and Event Line No.
USB_OTG wake-up event	EINT 18
Ethernet wake-up event	EINT 19
Reserved	EINT 20
Reserved	EINT 21
Reserved	EINT 22
Reserved	EINT 23
Reserved	EINT 24
Reserved	EINT 25
Reserved	EINT 26
Reserved	EINT 27
Reserved	EINT 28
Reserved	EINT 29
Reserved	EINT 30
Reserved	EINT 31

8.4 Register Address Mapping

Table 25 EINT Register Address Mapping

Register name	Description	Offset address
EINT_IMASK	Interrupt mask register	0x00
EINT_EMASK	Event mask register	0x04
EINT_RTEN	Enable the rising edge trigger selection register	0x08
EINT_FTEN	Enable the falling edge trigger selection register	0x0C
EINT_SWINTE	Software interrupt event register	0x10
EINT_IPEND	Interrupt pending register	0x14

8.5 Register Functional Description

8.5.1 Interrupt mask register (EINT_IMASK)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
19:0	IMASKx	R/W	Interrupt Request Mask on Line x 0: Mask 1: Open

Field	Name	R/W	Description
31:20	Reserved		

8.5.2 Event mask register (EINT_EMASK)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
19:0	EMASKx	R/W	Event Request Mask on Line x 0: Mask 1: Open
31:20	Reserved		

8.5.3 Enable the rising edge trigger selection register (EINT_RTEN)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
19:0	RTENx	R/W	Rising Trigger Event and Interrupt Enable of Line x 0: Disable 1: Enable
31:20	Reserved		

Note: Since the external wake-up lines are edge triggered, there should be no burr signal on these lines; when writing EINT_RTEN register, if the rising edge signal is on the external interrupt line, it will not be recognized and the set pending bit will not be set; in the same interrupt line, the rising edge trigger and falling edge trigger can be set at the same time.

8.5.4 Enable the falling edge trigger selection register (EINT_FTEN)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
19:0	FTENx	R/W	Falling Trigger Event Enable of Line x 0: Disable (interrupt and event) 1: Enable (interrupt and event)
31:20	Reserved		

Note: Since the external wake-up lines are edge triggered, there should be no burr signal on these lines; when writing EINT_FTEN register, if the rising edge signal is on the external interrupt line, it will not be recognized and the set pending bit will not be set; in the same interrupt line, the rising edge trigger and falling edge trigger can be set at the same time.

8.5.5 Software interrupt event register (EINT_SWINTE)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
19:0	SWINTEx	R/W	Software Interrupt Event on Line x This bit can be set to 1 by software, and be cleared by writing 1 to the corresponding bit of EINT_IPEND. When this bit is 0, the pending bit of EINT_IPEND can be set by writing 1. If EINT_IMASK (EINT_EMASK) is set to open the interrupt (event) request, an interrupt (event) will be generated. 0: No effect 1: Software generates an interrupt (event)
31:20	Reserved		

8.5.6 Interrupt pending register (EINT_IPEND)

Offset address: 0x14

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
19:0	IPENDx	RC_W1	Interrupt Pending Occur of Line x Flag When a trigger request on the corresponding edge of EINT_RTEN/EINT_FTEN occurs on an external interrupt line, it will be set to 1 by hardware; it can be cleared by changing the polarity of the edge detection or by writing 1 to this bit.
31:20	Reserved		

9 Direct Memory Access (DMA)

9.1 Full Name and Abbreviation Description of Terms

Table 26 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Global	G
Transfer	T
Half	H
Complete	C
Error	E
Channel	CH
Circular	CIR
Peripheral	PER
Increment	I
Memory	M
Priority	PRI
Number	N
Address	ADDR

9.2 Introduction

DMA (Direct Memory Access) can realize high-speed data transmission between peripheral devices and memory or between memory and memory without CPU intervention, thus saving CPU resources for other operations.

The product has two DMA controllers, DMA1 has 7 channels and DMA2 has 5 channes. Each channel can manage multiple DMA requests, but each channel can only respond to one DMA request at the same time. Each channel can set priority, and the arbiter can coordinate the priority of corresponding DMA requests of each DMA channel according to the priority of the channels.

9.3 Main Characteristics

（1） DMA1 has 7 channels, and DMA2 has 5 channels

（2） There are three data transmission modes: peripheral to memory, memory to peripheral, memory to memory

（3） Each channel has a dedicated hardware DMA request for connection

（4） Support software priority and hardware priority when multiple requests occur at the same time

（5） Each channel has three event flags and independent interrupts

（6） Support circular transmission mode

（7） The number of data transmission is programmable, up to 65535

9.4 Functional Description

9.4.1 DMA Request

If the peripheral or memory needs to use DMA to transmit data, it is required to first send DMA request and wait for DMA approval before data transmission.

DMA has 12 channels, DMA1 has 7 and DMA2 has 5. Each channel is connected with different peripherals, and each channel has three event flags (DMA half transmission, DMA transmission completion and DMA transmission error). The logic of the three event flags may become a separate interrupt request, and they all support software triggering.

When multiple peripherals request the same channel, it is required to configure the corresponding register to turn on or off the request of each peripheral, so as to ensure that only one peripheral request can be turned on in a channel.

Table 30 DMA1 Request Mapping Table

Peripheral	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7
TMR1	—	TMR1_CH1	TMR1_CH2	TMR1_CH4 TMR1_TRIG TMR1_COM	TMR1_UP	TMR1_CH3	—
TMR2	TMR2_CH3	TMR2_UP	—	—	TMR2_CH1	—	TMR2_CH2 TMR2_CH4
TMR3	—	TMR3_CH3	TMR3_CH4 TMR3_UP	—	—	TMR3_CH1 TMR3_TRIG	—
TMR4	TMR4_CH1	—	—	TMR4_CH2	TMR4_CH3	—	TMR4_UP
ADC1	ADC1	—	—	—	—	—	—
SPI/I2S	—	SPI1_RX	SPI1_TX	SPI/I2S2_RX	SPI/I2S2_TX	—	—
USART	—	USART3_TX	USART3_RX	USART1_TX	USART1_RX	USART2_RX	USART2_TX
I2C	—	—	—	I2C2_TX	I2C2_RX	I2C1_TX	I2C1_RX

Table 27 DMA2 Request Mapping Table

Peripheral	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
TMR5	TMR5_CH4 TMR5_TRIG	TMR5_CH3 TMR5_UP	—	TMR5_CH2	TMR5_CH1

Peripheral	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
TMR6/DAC channel 1	—	—	TMR6_UP/ DAC channel 1	—	—
TMR7/DAC channel 2	—	—	—	TMR7_UP/ DAC channel 2	—
SPI/I2S3	SPI/I2S3_RX	SPI/I2S3_TX	—	—	—
UART4	—	—	UART4_RX	—	UART4_TX

9.4.2 DMA Channel

9.4.2.1 Transmission data are programmable

The data transmitted by DMA are programmable, up to 65535, and the transmission data bit width of peripherals and memory can be set by configuring PERSIZE bit and MEMSIZE bit of DMA_CHCFGx register.

9.4.2.2 Transmission width and alignment method are programmable

Programmable data transmission width DMA transmission operations:

Figure 8 Transmission Width with Source of 8bits and Target of 8bits

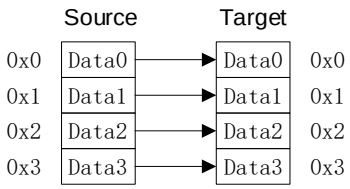


Figure 9 Transmission Width with Source of 8bits and Target of 16bits

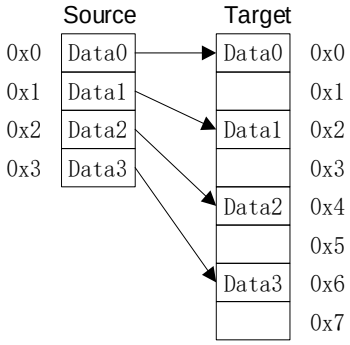


Figure 10 Transmission Width with Source of 8bits and Target of 32bits

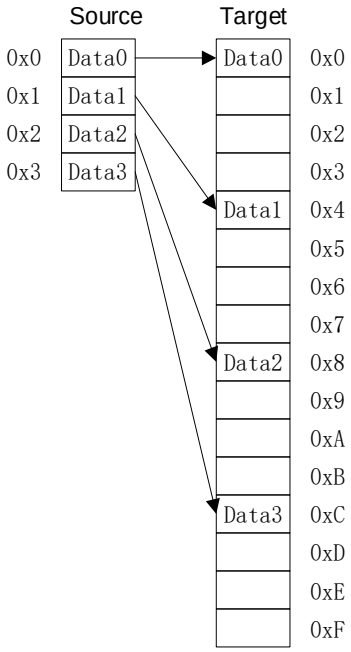


Figure 11Transmission Width with Source of 32bits and Target of 8bits

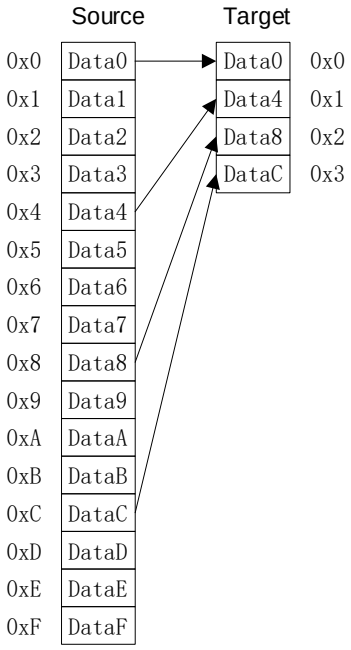


Figure 12Transmission Width with Source of 16bits and Target of 16bits

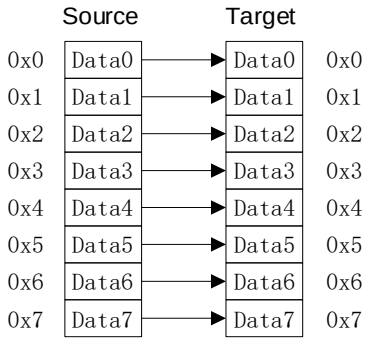


Figure 13 Transmission Width with Source of 16bits and Target of 32bits

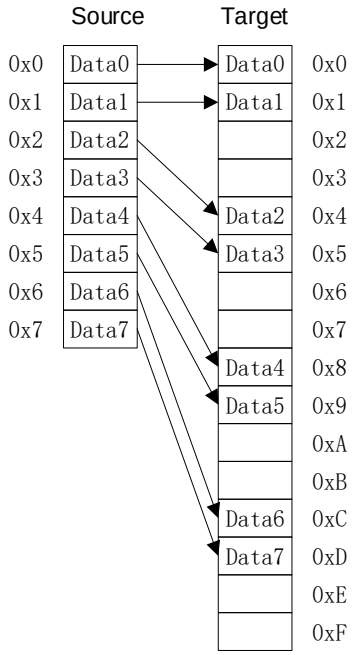
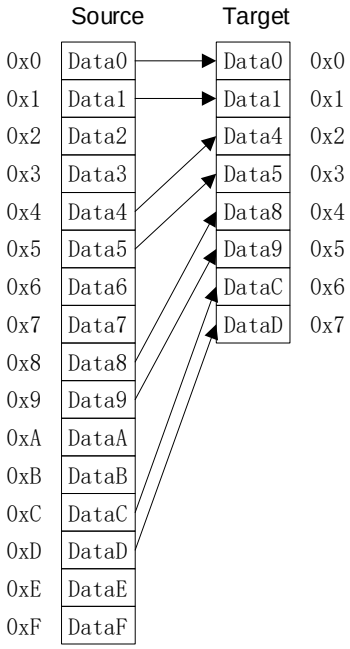


Figure 14 Transmission Width with Source of 32bits and Target of 16bits



9.4.2.3 Address setting

The transmission address supports two modes: fixed mode and pointer increment mode.

Transmission address pointer increment mode

The automatic pointer increment of peripheral and memory is completed through the PERIMODE bit and MIMODE bit of configuration register DMA_CHCFGx. The next address to be transmitted is the one by adding the increment to the previous address. The increment depends on the selected data width.

9.4.2.4 Transmission mode

There are two channel configuration modes: non-circular mode and circular mode.

Non-circular mode

When the data transmission is finished, the DMA operation will not be performed any more, and the new DMA transmission will be started. When the DMA channel is not working, the register DMA_CHNDATAx will rewrite the transmission value.

Circular mode

After data transmission, the content of the register DMA_CHNDATAx will be automatically reloaded to the previously configured value, and the peripheral address register DMA_CHPADDRx and the memory address register

DMA_CHMADDRx will also be reloaded as the initial base address.

The configuration method is as follows:

- Set the CIRMODE bit of the configuration register DMA_CHCFGx to 1 to turn on the circular mode;
- This mode is used to process continuous peripheral requests. When the number of data transmission becomes 0, it will automatically return to the initial value and continue DMA operation until the CIRMODE bit is cleared and the system exits the circular mode.

9.4.2.5 DMA request priority setting

Arbitrator

When multiple DMA channel requests occur, an arbiter is needed to manage the response sequence. Management is divided into two stages: the first stage is software stage, which is divided into the highest, high, medium and low priority; the second stage is hardware stage, and under the condition of the same software priority, the lower the channel number is, the higher the priority is.

9.4.2.6 Transmission direction

Support three directions: from memory to memory, from memory to peripheral, and from peripheral to memory.

If the write operation (target address) is performed on the memory, the memory includes internal SRAM, external RAM supported by EMMC (such as external SRAM, SDRAM) and NORFLASH; if the read operation (source address) is performed on the memory, the address includes internal FLASH, internal SRAM, RAM supported by EMMC, and NORFLASH.

Examples of "from memory to memory" configuration are as follows:

- The M2MMODE bit of the configuration register DMA_CHCFGx enables memory to the memory mode;
- The DMA operation in this mode is performed under the condition of no peripheral request. The CHEN bit of the configuration register DMA_CHCFGx is set to 1, and after the channel is opened, the data transmission will start and when the transmission quantity register DMA_CHNDATAx becomes 0, the transmission is over.

9.4.3 Interrupt

Each DMA channel has three types of interrupt events, which are half transmission (HT), transmission completion (TC) and transmission error (TE).

（1） The interrupt event flag bit for half transmission is HTFLG, and the interrupt enable control bit is HTINTEN

（2） The interrupt event flag bit for transmission completion is TCFLG, and the interrupt enable control bit is TCINTEN

（3） The interrupt event flag bit for transmission error is TERRFLG, and the interrupt enable control bit is TERRINTEN

9.5 Register Address Mapping

Table 28 Register Address Mapping

Register name	Description	Offset address
DMA_INTSTS	DMA interrupt state register	0x00
DMA_INTFCLR	DMA interrupt flag clear register	0x04
DMA_CHCFGx	DMA Channel x configuration register	0x08+20 x
DMA_CHNDATAx	DMA Channel x transmission quantity register	0x0C+20 x
DMA_CHPADDRx	DMA Channel x peripheral address register	0x10+20 x
DMA_CHMADDRx	DMA Channel x memory address register	0x14+20 x

9.6 Register Functional Description

9.6.1 DMA interrupt state register (DMA_INTSTS)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
24,20,16, 12,8,4,0	GINTFLGx	R	Channel x Global Interrupt Occur Flag (x=1…7) Indicate whether TC, HT or TE interrupt is generated on the channel; these bits are set to 1 by hardware; write 1 and clear on the corresponding bit of DMA_INTFCLR. 0: Not generate 1: Generate
25,21,17, 13,9,5,1	TCFLGx	R	Channel x All Transfer Complete Flag (x=1…7) Indicate whether the transmission completion interrupt (TC) is generated on the channel; these bits are set to 1 by hardware; write 1 and clear on the corresponding bit of DMA_INTFCLR. 0: Not completed 1: Completed
26,22,18, 14,10,6,2	HTFLGx	R	Channel x Half Transfer Complete Flag (x=1…7) Indicate whether the half transmission interrupt (HT) is generated on the channel; these bits are set to 1 by hardware; write 1 and clear on the corresponding bit of DMA_INTFCLR. 0: Not generate 1: Generate
27,23,19, 15,11,7,3	TERRFLGx	R	Channel x Transfer Error Occur Flag (x=1…7) Indicate whether the transmission error interrupt (TE) is generated on the channel; these bits are set to 1 by hardware; write 1 and clear on the corresponding bit of DMA_INTFCLR. 0: Not generate 1: Generate

Field	Name	R/W	Description
31:28	Reserved		

9.6.2 DMA interrupt flag clear register (DMA_INTFCLR)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
24,20,16,12, 8,4,0	GINTCLRx	R/W	Channel x Global Interrupt Occur Flag Clear (x=1...7) Clear the corresponding GINTFLG, TCFLG, HTFLG and TERRFLG flags in the interrupt state register. 0: Invalid 1: Clear the GINTFLG flag
25,21, 17,13, 9,5,1	TCCLRx	R/W	Channel x Transfer Complete Clear (x=1...7) Clear the corresponding TCFLG flag in interrupt state register. 0: Invalid 1: Clear the TCFLG flag
26,22 18,14, 10,6,2	HTCLRx	R/W	Channel x Half Transfer Complete Clear (x=1...7) Clear the corresponding HTFLG flag in interrupt state register. 0: Invalid 1: Clear the HTFLG flag
27,23, 19,15, 11,7,3	TERRCLRx	R/W	Channel x Transfer Error Occur Clear (x=1...7) Clear the corresponding TERRFLG flag in interrupt state register. 0: Invalid 1: Clear the TERRFLG flag
31:28	Reserved		

9.6.3 DMA Channel x configuration register (DMA_CHCFGx) (x=1…7)

Offset address: 0x08+20 x (channel number–1)

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CHEN	R/W	DMA Channel Enable 0: Disable 1: Enable
1	TCINTEN	R/W	All Transfer Complete Interrupt Enable 0: Disable 1: Enable
2	HTINTEN	R/W	Half Transfer Complete Interrupt Enable 0: Disable 1: Enable
3	TERRINTEN	R/W	Transfer Error Occur Interrupt Enable 0: Disable 1: Enable
4	DIRCFG	R/W	Data Transfer Direction Configure

Field	Name	R/W	Description
			0: Read from peripheral to memory 1: Read from memory to peripheral
5	CIRMODE	R/W	Circular Mode Enable 0: Disable 1: Enable
6	PERIMODE	R/W	Peripheral Address Increment Mode Enable 0: Disable 1: Enable
7	MIMODE	R/W	Memory Address Increment Mode Enable 0: Disable 1: Enable
9:8	PERSIZE	R/W	Peripheral Data Size Configure 00: 8 bits 01: 16 bits 10: 32 bits 11: Reserved Note: It cannot be configured to 00 when I2C3/4 is used by user.
11:10	MEMSIZE	R/W	Memory Data Size Configure 00: 8 bits 01: 16 bits 10: 32 bits 11: Reserved Note: It cannot be configured to 00 when I2C3/4 is used by user.
13:12	CHPL	R/W	Channel Priority Level Configure 00: Low 01: Medium 10: High 11: Highest
14	M2MMODE	R/W	Memory to Memory Mode Enable 0: Disable 1: Enable
31:15	Reserved		

9.6.4 DMA Channel x transmission quantity register (DMA_CHNDATAx) (x=1…7)

Offset address: 0x0C+20 x (channel number–1)

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	NDATAT	R/W	Number of Data to Transfer Setup This register indicates the number of bytes to be transmitted. The number of data transmission ranges from 0 to 65535. This register can only be written when the channel is not working; once the channel is enabled, the register will be read-only, indicating the number of remaining bytes to be transmitted. The register will decrease after each DMA is transmitted; when the data transmission is completed, the register will change to 0, or when the channel is configured to auto reload mode, it will be automatically reloaded to the previously configured value; if the register is 0, data transmission will not occur regardless of whether the channel is turned on or not.
31:16	Reserved		

9.6.5 DMA Channel x peripheral address register (DMA_CHPADDRx) (x=1…7)

Offset address: 0x10+20 x (channel number–1)

Reset value: 0x0000 0000

This register cannot be written when the channel is turned on (CHEN=1 for DMA_CHCFGx).

Field	Name	R/W	Description
31:0	PERADDR	R/W	Peripheral Basic Address Setup When PERSIZE= '01' (16 bits) and PERADDR[0] bit is not used, it will be aligned with 16-bit address automatically during transmission. When PERSIZE= '10' (32 bits) and PERADDR[1:0] bit is not used, it will be aligned with 32-bit address automatically during transmission.

9.6.6 DMA Channel x memory address register (DMA_CHMADDRx) (x=1…7)

Offset address: 0x14+20 x (channel number–1)

Reset value: 0x0000 0000

This register cannot be written when the channel is turned on (CHEN=1 for DMA_CHCFGx).

Field	Name	R/W	Description
31:0	MEMADDR	R/W	Memory Basic Address Setup When MEMSIZE= '01' (16 bits) and MEMADDR[0] bit is not used, it will be aligned with 16-bit address automatically during transmission. When MEMSIZE= '10' (32 bits) and MEMADDR[1:0] bit is not used, it will be aligned with 32-bit address automatically during transmission.

10 Debug MCU (DBGMCU)

10.1 Full Name and Abbreviation Description of Terms

Table 29 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Frame Clock	FCLK
Serial Wire/JTAG Debug Port	SWJ-DP

10.2 Introduction

APM32F10x MCU series uses Arm® Cortex®-M3 core, and Arm® Cortex®-M3 core includes hardware debug module and supports complex debug operation. During debugging, the module can make the running core stop at breakpoint, and achieve the effect of querying the internal state of the core and the external state of the system, and after the query is completed, the core and peripheral operation can be restored to continue to execute the program.

Two debug interfaces are supported:

- Serial interface
- JTAG debug interface

Note: The hardware debug interface included in Arm® Cortex®-M3 core is subset of Arm CoreSight development tool set. Please refer to *Cortex®-M3 (Version r1p1) Technical Reference Manual (TRM)* and *CoreSight Development Tool Set (Version r1p0) TRM* for more information about debug function of Arm® Cortex®-M3 core.

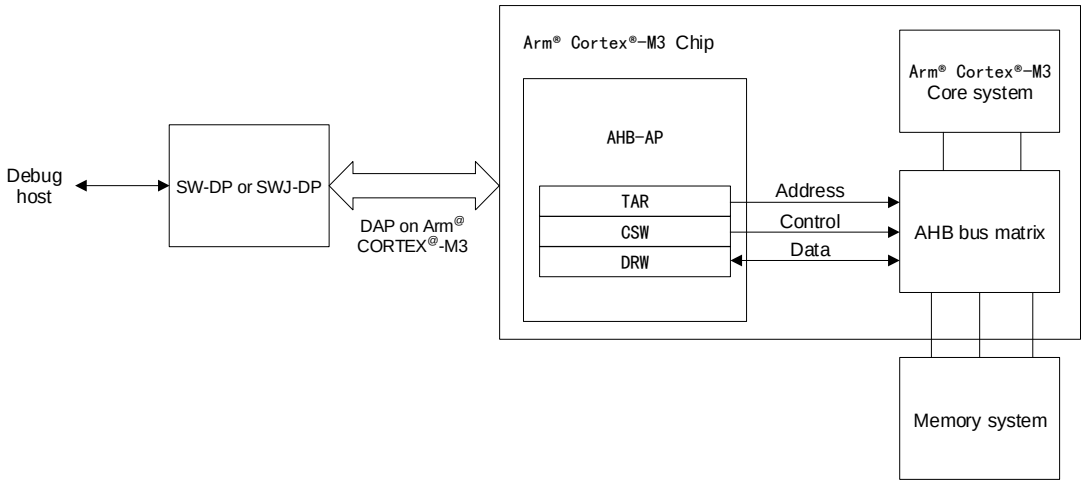
10.3 Main Characteristics

（1） Replace the core to access AHB bus matrix

（2） Flexible debug pin assignment

（3） MCU debug box (support low-power mode, control peripheral clock, etc.)

Figure 15 APM32F10xxx Level and Arm® Cortex®-M3 Level Debugging Block Diagram



10.4 Functional Description

10.4.1 Debug Pin Function Configuration

（1） Realize the on-line programming and debugging of the chip

（2） Using KEIL/IAR and other software to achieve on-line debugging, downloading and programming

（3） Flexible implementation of production of bus-line programmer

Table 30 Pin Function Configuration

SWJ-CFG[2:0]	Configured as dedicated pin for debugging	I/O port assignment of SWJ interface				
		PA13/ JTMS/ SWDIO	PA14/ JTCK/ SWCLK	PA15/ JTDI	PB3/ JTDO	PB4/ JNTRST
Others	Disable	Reserved				
100	Both JTAG-DP interface and SW-DP interface disabled					
010	JTAG-DP interface disabled, SW-DP interface enabled	Dedicated	Dedicated	Reserved		
001	All SWJ pins (JTAG-DP+SW-DP) Except JNTRST pin	Dedicated	Dedicated	Dedicated	Dedicated	Reserved
000	All SWJ pins (JTAG-DP+SW-DP) Reset state	Dedicated	Dedicated	Dedicated	Dedicated	Dedicated

Note: The items that cannot be tested in running mode can be observed and tested in detail

10.4.2 ID Code

10.4.2.1 MCU device ID code

APM32F MCU series incudes a MCU ID code. It can be accessed with JTAG or SW debug interface or user code.

10.4.2.2 Boundary scan TAP

JTAG ID code

The boundary scan TAP of APM32F MCU series integrates JTAG ID code. For APM32F107 105xx series products, its JTAG ID code is 0x06414B47

10.4.2.3 Arm® Cortex®-M3 TAP

Arm® Cortex®-M3 TAP has a JTAG ID code, which is 0x4BA00477.

10.4.2.4 Arm® Cortex®-M3 JEDEC-106 ID code

Arm® Cortex®-M3 has a JEDEC-106 ID code. It is located in 4KB ROM table in which the internal PPB bus address is 0xE00FF000_0xE00FFFFF.

10.5 Register Address Mapping

Table 31 Register Address Mapping

Register name	Description	Address
DBGMCU_IDCODE	Device ID register	0xE004 2000
DBGMCU_CFG	Debug MCU configuration register	0xE004 2004

10.6 Register Functional Description

10.6.1 Device ID register (DBGMCU_IDCODE)

Address: 0xE004 2000

Only support 32-bit access

Reset value: 0xXXXX XXXX, X=undefined bit

Field	Name	R/W	Description
11:0	EQR	R	Equipment Recognition For APM32F10x MCU series: APM32F107 105xx series products: 0x418; The debugger/programming tool identifies chips by QR (11:0).
15:12	Reserved		
31:16	WVR	R	Wafer Version Recognition For APM32F10x MCU series: APM32F107 105xx series products:0x0014; This domain identifies wafer information

10.6.2 Debug MCU configuration register (DBGMCU_CFG)

This register can configure MCU in debug mode. It includes the counter supporting timer and watchdog, low-power mode, CAN communication and assignment tracking pin.

Address: 0xE004 2004

Only support 32-bit access

Reset value: 0x0000 0000 (not affected by system reset, only power-on reset)

Field	Name	R/W	Description
0	SLEEP_CLK_STS	R/W	Configure clock status when MCU is debugged in sleep mode 0: FCLK ON, HCLK OFF 1: FCLK ON, HCLK ON, provided by system clock
1	STOP_CLK_STS	R/W	Configure clock status when MCU is debugged in stop mode 0: FCLK OFF, HCLK OFF 1: FCLK ON, HCLK ON, provided by HSICLK
2	STANDBY_CLK_STS	R/W	Configure clock status when MCU is debugged in standby mode 0: FCLK OFF, HCLK OFF 1: FCLK ON, HCLK ON, provided by HSICLK
4:3	Reserved		
5	TRACE_IOEN	R/W	Trace Debug Pin Enable 0: Tracking debug pin disabled 1: Tracking debug pin enabled
7:6	TRACE_MODE	R/W	Trace Debug Pin Mode Configure Tracking debug pin mode can be configured only when TRACE_IOEN=1: 00: Asynchronous mode 01: Synchronous mode, the data length is 1 10: Synchronous mode, the data length is 2 11: Synchronous mode, the data length is 4
8	IWDT_STS	R/W	Configure Independent Watchdog Work Status When Core Is in Halted 0: Work normally 1: Stop working
9	WWDT_STS	R/W	Configure Window Watchdog Work Status When Core Is in Halted 0: Work normally 1: Stop working
13:10	TMRx_STS	R/W	ConfigureTimer Work Status When Core Is in Halted 0: Work normally 1: Stop working
14	CAN1_STS	R/W	Configure CAN1 Work Status When Core Is in Halted 0: Work normally 1: Freeze the receiver transmitter of CAN1

Field	Name	R/W	Description
15	I2C1_SMBUS_TIMEOUT_STS	R/W	Configure I2C1_SMBUS_TIMEOUT Work Status When Core Is in Halted 0: Work normally 1: Freeze the timeout mode of SMBUS
16	I2C2_SMBUS_TIMEOUT_STS	R/W	Configure I2C2_SMBUS_TIMEOUT Work Status When Core Is in Halted 0: Work normally 1: Freeze the timeout mode of SMBUS
19:17	TMRx_STS	R/W	ConfigureTimer Work Status When Core Is in Halted 0: When the core is halted, the clock can be provided to the counter of related timer, and the timer can output normally 1: When the core is halted, the clock will not be prvovided to the counter of the related timer and the timer output will be disabled
20	Reserved		
21	CAN2_STS	R/W	Configure CAN2 Work Status When Core Is in Halted 0: Work normally 1: Freeze the receiver transmitter of CAN2
31:22	Reserved		

11 General-Purpose Input/Output Pin (GPIO)

11.1 Full Name and Abbreviation Description of Terms

Table 32 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
P-channel Metal Oxide Semiconductor	P-MOS
N-channel Metal Oxide Semiconductor	N-MOS

11.2 Main Characteristics

GPIO port can configure the following functions through 32-bit configuration register (GPIOx_CFGLOW/GPIOx_CFGHIG) and two 32-bit data registers GPIOx_IDATA/GPIOx_ODATA):

（1） Input mode
- Analog input
- Floating input
- Pull-up input
- Pull-down input

（2） Output mode
- Push-pull output
- Open-drain output
- Configurable maximum output rate

（3） Multiplexing mode
- Push-pull multiplexing function
- Open-drain multiplexing function

（4） GPIO can be used as external interrupt/wake-up line

（5） Support locking I/O configuration function

11.3 Structure Block Diagram

Figure 16 GPIO Structure Block Diagram

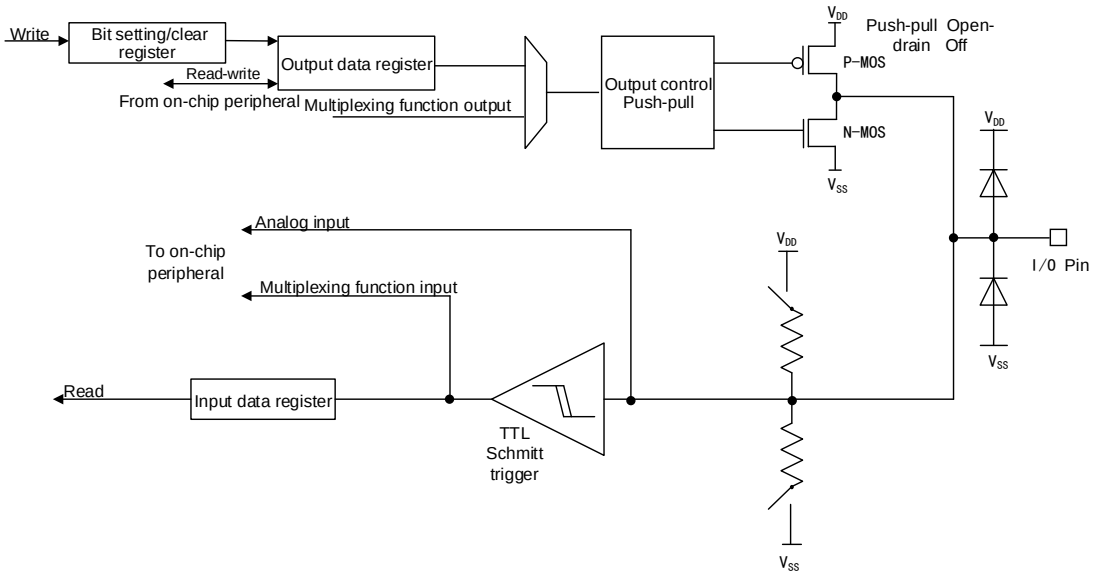
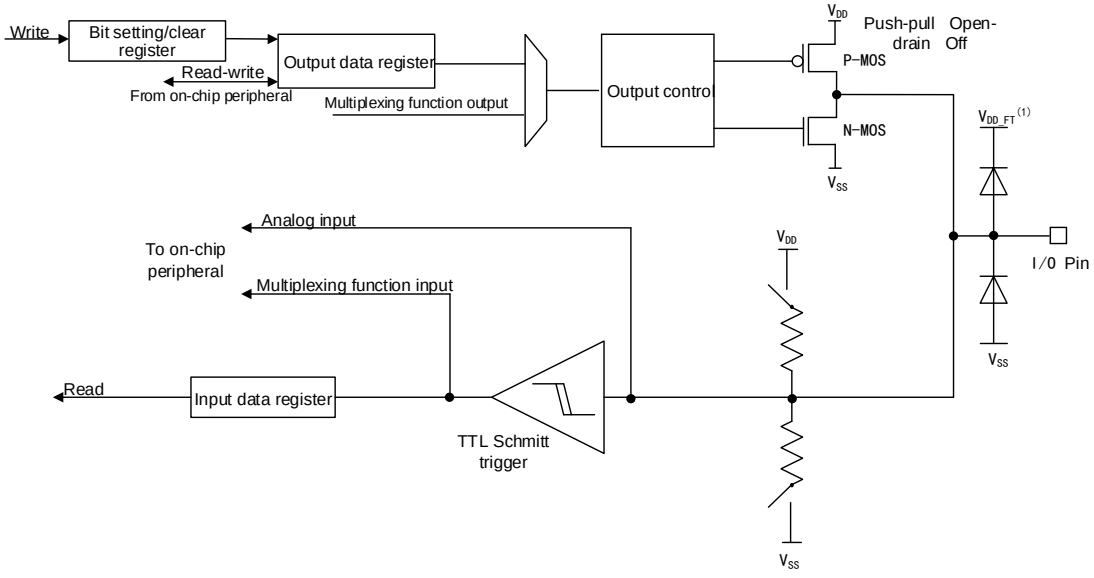


Figure 17 5V GPIO-compatible Structure Block Diagram



(1) V_{DD_FT} is different from V_{DD}, and V_{DD_FT} is special for FT GPIO pin.

11.4 Functional Description

Each pin of GPIO can be configured as pull-up, pull-down, floating and analog input, or push-pull/open-drain output input mode and multiplexing function through software. All GPIO interfaces have external interrupt capability.

11.4.1 IO status during Reset and just after Reset

If the multiplexing function is not enabled during and after GPIO reset, the I/O port will be configured as floating input mode, and in such case the pull-up/pull-

down resistor is disabled in input mode. After reset, the JTAG pin is put in the input pull-up or pull-down mode, and the specific configuration is as follows:

- PA15: JTDI in pull-up mode
- PA14: JTCK in pull-down mode
- PA13: JTMS in pull-up mode
- PB4: JNTRST in pull-up mode

11.4.2 Input Mode

In the input mode, it can be set as pull-up, pull-down, floating and analog input.

When GPIO is configured as input mode, all GPIO pins have internal weak pull-up and weak pull-down resistors, which can be activated or disconnected.

Pull-up, pull-down, and floating modes

In (pull-up, pull-down, floating) input mode

- Schmitt trigger is opened,
- Disable output buffer
- Connect weak pull-up and pull-down resistors according to different input configurations
- The input data register GPIOx_IDATA captures the data on I/O pin in each APB2 clock cycle
- Read I/O state through the input data register GPIOx_IDATA

The initial level state of the floating input mode is uncertain and is easy to be disturbed by the outside; when connecting the equipment, it is determined by the external input level (except for the very high impedance).

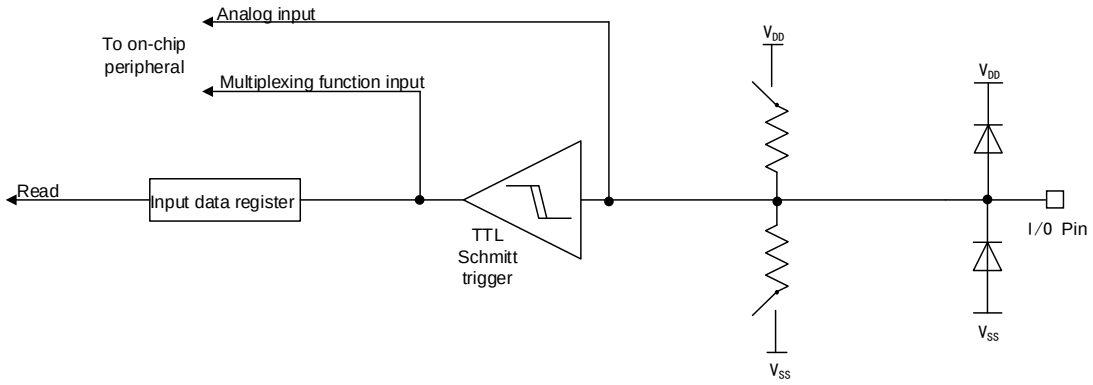
The initial level state of pull-up/pull-down input mode is high level if pull-up, and low level if pull-down; when connecting the equipment, it is determined by the external input level and load impedance.

Analog input mode

In analog input mode

- Disable output buffer
- The input of Schmitt trigger is disabled, and the output value of Schmitt trigger is forced to be 0
- Weak pull-up and pull-down resistors are disabled
- The value of port input state register is 0

Figure 18 Input Mode Structure



11.4.3 Output Mode

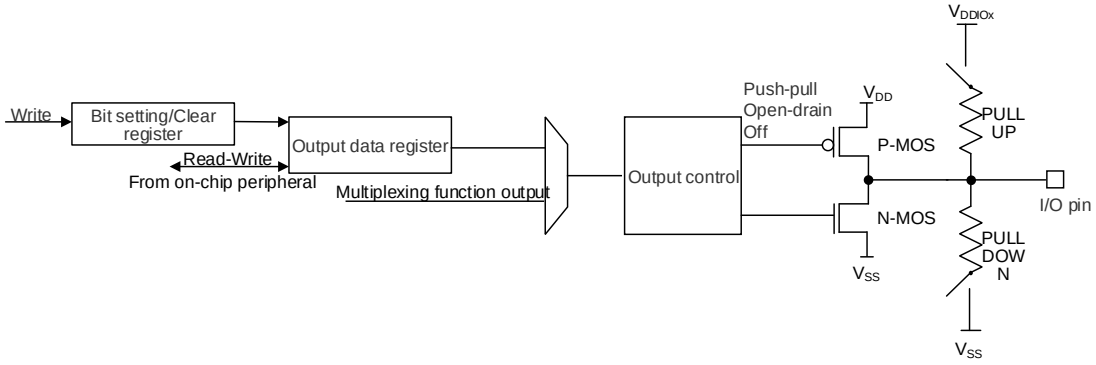
In the output mode, it can be set as push-pull output and open-drain output.

When GPIO is configured as the output pin, the output speed of the port can be configured and the output drive mode (push-pull / open-drain) can be selected.

In output mode

- Schmitt trigger is opened,
- Activate output buffer
- Weak pull-up and pull-down resistors are disabled
- Push-pull mode:
  - Double MOS transistor works by turns and the output data register can control the high and low level of I/O output
  - Read the finally written value through the output data register GPIOx_ODATA
- Open-drain mode:
  - Only N-MOS works, and the output data register can control I/O output high resistance state or low level
  - Read the actual I/O state through the input data register GPIOx_IDATA

Figure 19 I/O Structure in Output Mode



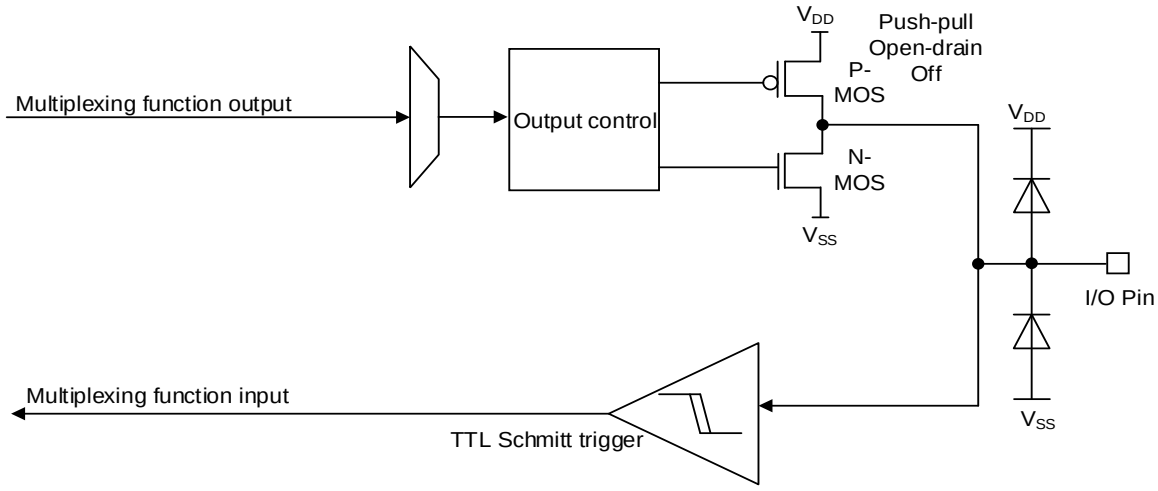
11.4.4 Multiplexing Mode

In multiplexing mode, it can be set as push-pull multiplexing and open-drain multiplexing

In push-pull/open-drain multiplexed mode

- Open the output buffer
- Output buffer is driven by peripheral
- Activate Schmitt trigger input
- Weak pull-up and pull-down resistors are disabled
- The data on the I/O pin is sampled in each APB2 clock cycle and stored in the port input state register
- In open-drain mode, the actual state of I/O can be read through input data register GPIOx_IDATA
- In push-pull mode, the last written value is read through output data register GPIOx_ODATA

Figure 20 I/O Structure in Multiplexing Mode



11.4.5 External Interrupt/Wake-up Line

All GPIO ports have external interrupt function. If you want to use external interrupt line, the port must be configured as input mode.

11.4.6 Bit Set and Bit Clear

Software does not need to disable interrupt when programming some bits of GPIOx_IDATA. (The function of changing one or more bits in APB2 write operation can be implemented by setting the bit to be changed in GPIOx_BSC 和 BSC register to 1.

11.4.7 GPIO Locking Function

Locking function can be used in power driver module. The locking mechanism of GPIO can protect the configuration of I/O port. I/O configuration can be locked by configuring the lock register (GPIOx_LOCK). When a port bit

executes the locking program, the configuration of port bit cannot be modified before the next reset.

11.5 Register Address Mapping

Table 33 GPIO Register Address Mapping

Register name	Description	Offset address
GPIOx_CFGLOW	Low-8-bit port configuration low register	0x00
GPIOx_CFGHIG	High-8-bit port configuration high register	0x04
GPIOx_IDATA	Port input data register	0x08
GPIOx_ODATA	Port output data register	0x0C
GPIOx_BSC	Port bit set/clear register	0x10
GPIOx_BC	Port bit clear register	0x14
GPIOx_LOCK	Port configuration lock register	0x18

11.6 Register Functional Description

These peripheral registers must be operated by word (32 bits).

11.6.1 Low 8-bit port configuration register (GPIOx_CFGLOW) (x=A..E)

Offset address: 0x00

Reset value: 0x4444 4444

Field	Name	R/W	Description
29:28 25:24 21:20 17:16 13:12 9:8 5:4 1:0	MODEy[1:0]	R/W	Port x mode Configure (y=0…7) 00: Input mode (state after reset) 01: Output mode, the maximum output speed is 10MNz 10: Output mode, the maximum output speed is 2MNz 11: Output mode, the maximum output speed is 50MNz See the *Data Manual* for the definition of maximum output speed.
31:30 27:26 23:22 19:18 15:14 11:10 7:6 3:2	CFGy[1:0]	R/W	Port x Function Configure (y=0…7) The software configures corresponding I/O ports through these bits. In input (MODE[1:0]=00) mode 00: Analog input mode 01: Floating input mode (state after reset) 10: Pull-up/Pull-down input mode 11: Reserved In output mode (MODE[1:0]>00) 00: General push-pull output mode 01: General open-drain output mode 10: Push-pull output mode of multiplexing function

Field	Name	R/W	Description
			11: Open-drain output mode of multiplexing function

11.6.2 High 8-bit port configuration register (GPIOx_CFGHIG) (x=A...E)

Offset address: 0x04

Reset value: 0x4444 4444

Field	Name	R/W	Description
29:28 25:24 21:20 17:16 13:12 9:8 5:4 1:0	MODEy[1:0]	R/W	Port x mode Configure (y=8…15) The software configures corresponding I/O ports through these bits. 00: Input mode (state after reset) 01: Output mode, the maximum output speed is 10MNz 10: Output mode, the maximum output speed is 2MNz 11: Output mode, the maximum output speed is 50MNz See the *Data Manual* for the definition of maximum output speed.
31:30 27:26 23:22 19:18 15:14 11:10 7:6 3:2	CFGy[1:0]	R/W	Port x Function Configure (y=8…15) The software configures corresponding I/O ports through these bits. In input (MODE[1:0]=00) mode 00: Analog input mode 01: Floating input mode (state after reset) 10: Pull-up/Pull-down input mode 11: Reserved In output mode (MODE[1:0]>00) 00: General push-pull output mode 01: General open-drain output mode 10: Push-pull output mode of multiplexing function 11: Open-drain output mode of multiplexing function

11.6.3 Port input data register (GPIOx_IDATA) (x=A...E)

Offset address: 0x08

Reset value: 0x0000 XXXX

Field	Name	R/W	Description
15:0	IDATAy	R	Port input data (y=0…15) These bits are read-only and can be read out only in the form of word. 0: Output signal is at low level 1: Output signal is at high level
31:16	Reserved		

11.6.4 Port output data register (GPIOx_ODATA) (x=A…E)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	ODATAy	R/W	(Port output data) (y=0…15)

Field	Name	R/W	Description
			These bits are readable and writable and can be operated only in the form of word. 0: Output low level 1: Output high level Note: For PIOx_BSC (x=A…E), each ODATAy bit can be set/cleared independently respectively.
31:16	Reserved		

11.6.5 Port bit setup/clear register (GPIOx_BSC) (x=A…E)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	BSy	W	Port x Set bit y (y=0…15) These bits are used to affect the corresponding ODATAy bits. 0: No effect 1: Set the corresponding ODATAy bits to 1 These bits are write-only and can be operated only in the form of word.
31:16	BCy	W	Port x Clear bit y (y=0…15) These bits are used to affect the corresponding ODATAy bits. 0: No effect 1: Corresponding ODATAy bit is cleared Note: BSy bit will work if the corresponding bits of both BSy and BCy are set. These bits are write-only and can be operated only in the form of word.

11.6.6 Port bit clear register (GPIOx_BC) (x=A…E)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	BCy	W	Port x Clear bit y (y=0…15) These bits are used to affect the corresponding ODATAy bits. 0: No effect 1: Corresponding ODATAy bit is cleared These bits are write-only and can be operated only in the form of word.
31:16	Reserved		

11.6.7 Port configuration lock register (GPIOx_LOCK) (x=A…E)

This register protects the configuration of GPIO from being modified by mistake during the running of the program. If the GPIO configuration is modified again, it can be modified only after the system is reset. When configuring GPIO configuration, it is necessary to write the specified sequence to the register to start the GPIO locking function.

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	LOCKy	R/W	Port x Pin y Lock bit y Configure (y=0…15) These bits decide whether to lock the port configuration. 0: The configuration of Port x Pin y is not locked 1: The configuration of Port x Pin y is locked These bits can be read and written, but can only be written when LOCKKEY=0.
16	LOCKKEY	R/W	Lock key value This bit determines whether the port configuration lock key bit is activated 0: Not activated 1: Activated; GPIOx_LOCK register is locked before the system is reset next time This bit can be read out at any time, and it can be written into the sequence modification through the lock key Write sequence of lock key: Write 1 Write 0 Write 1 Read 0 Read 1 (The last read can be ignored, but can be used to confirm that the lock key has been activated.) Note: In the lock key value sequence, the value of LOCKy cannot be changed, and no error (sequence error, read error) can activate the lock protection.
31:17	Reserved		

12 Alternate Function Input and Output Pin (AFIO)

12.1 Introduction

In addition to the general I/O function, the I/O port can also be used as the interface of various peripheral functions. In order to make full use of the peripheral I/O pins of the product, the product supports the multiplexing function. It can not only realize multiple functions on the same pin (only one function can be realized at the same time), but also remap a certain function to other I/O (the originally supported function is no longer supported).

12.2 Functional Description

12.2.1 Alternate Function of I/O Pin

In order to make full use of peripheral I/O pins, some multiplexing functions can be remapped to other idle pins to maximize the utilization of pin resources.

Table 34 Corresponding Port Configuration of Multiplexing Function

Multiplexing function	**Configure for port bit configuration register**
Multiplexing input function	Configure as input mode and the input pin must be driven externally
Multiplexing output function	Configure as multiplexing function output mode
Bidirectional multiplexing function	Configure as multiplexing function output function, and the input driver is configured as floting input mode

Note:

(1) Through the GPIO controller programming, use the software to simulate the multiplexing function input pin, then the port is set to the multiplexing function output mode, and the pin is driven by software through the GPIO controller.

(2) When the multiplexing function is output, the pin is disconnected from the output register and connected with the output signal of the on-chip peripheral. If the peripheral is not activated after connection, the output of the pin will be uncertain.

12.2.1.1 Input mode configuration

When I/O port is used as input mode of multiplexing function, except that the weak pull-up and pull-down resistors are disabled, the port configuration is the same as that of general input function.

See corresponding chapters in GPIO for details of corresponding mode configuration.

12.2.1.2 Output mode configuration

When the I/O port is used as the output mode of multiplexing function (push-pull or open-drain), like the general output function, the output mode can be set as push-pull output and open-drain output, but the output buffer is driven by the signal of the built-in peripheral.

See corresponding chapters in GPIO for details of corresponding mode configuration.

Note: When software simulates multiplexing function input pin, the I/O port should be configured as multiplexing function output mode.

12.2.1.3 Bidirectional multiplexing function configuration

When bidirectional multiplexing function is used, the I/O port must be configured as multiplexing function output mode (push-pull or open-drain), while the input driver should be configured as floating input mode.

See corresponding chapters in GPIO for details of corresponding mode configuration.

12.2.2 Peripheral Pin Configuration

At this time, since the peripheral pin may have different functions, the I/O port configuration of the pin is different.

Table 39 TMR Pin Configuration

TMR pin	Configure	I/O port configuration
TMR1_CHx	Input capture channel x	Floating input
	Output compare channel x	Push-pull multiplexing output
TMR1_CHxN	Complementary output channel x	Push-pull multiplexing output
TMR1_BKIN	Braking input	Floating input
TMR1_ETR	External trigger clock input	Floating output
TMR2/3/4/5_CHx	Input capture channel x	Floating input
	Output compare channel x	Push-pull multiplexing output
TMR2/3/4/5_ETR	External trigger clock input	Floating input

Table 40 USART Pin Configuration

USRAT pin	Configure	I/O port configuration
USRATx_TX	Full duplex mode	Push-pull multiplexing output
	Half duplex synchronous mode	Push-pull multiplexing output

USRAT pin	Configure	I/O port configuration
USARTx_RX	Full duplex mode	Floating input or pull-up input
	Half duplex synchronous mode	Unused, can be used as GPIO
USARTx_CK	Synchronous mode	Push-pull multiplexing output
USARTx_RTS	Hardware flow control	Push-pull multiplexing output
USARTx_CTS	Hardware flow control	Floating input or pull-up input

Table 35 SPI Pin Configuration

SPI pin	Configure	I/O port configuration
SPIx_SCK	Master mode	Push-pull multiplexing output
	Slave mode	Floating input
SPIx_MOSI	Full duplex mode/master mode	Push-pull multiplexing output
	Full duplex mode/slave mode	Floating input or pull-up input
	Simple bidirectional data cable/master mode	Push-pull multiplexing output
	Simple bidirectional data cable/slave mode	Unused, can be used as GPIO
SPIx_MISO	Full duplex mode/master mode	Floating input or pull-up input
	Full duplex mode/slave mode	Push-pull multiplexing output
	Simple bidirectional data cable/master mode	Unused, can be used as GPIO
	Simple bidirectional data cable/slave mode	Push-pull multiplexing output
SPIx_NSS	Hardware master/save mode	Floating input or pull-up input or pull-down input
	Hardware master mode/NSS output enable	Push-pull multiplexing output
	Software mode	Unused, can be used as GPIO

Table 42 I2S Pin Configuration

I2S pin	Configure	I/O port configuration
I2Sx_WS	Master mode	Push-pull multiplexing output
	Slave mode	Floating input
I2Sx_CK	Master mode	Push-pull multiplexing output
	Slave mode	Floating input
I2Sx_SD	Transmitter	Push-pull multiplexing output
	Receiver	Floating input or pull-up input or pull-down input
I2Sx_MCK	Master mode	Push-pull multiplexing output
	Slave mode	Unused, can be used as GPIO

Table 43 I2C Pin Configuration

I2C pin	Configure	I/O port configuration
I2Cx_SCL	I2C clock	Open-drain multiplexing output
I2Cx_SDA	I2C data	Open-drain multiplexing output

Table 36 BxCAN Pin Configuration

CAN pin	I/O port configuration
CAN_TX	Push-pull multiplexing output
CAN_RX	Floating input or pull-up input

Table 37 USB OTG_FS Pin Configuration

USB OTG_FS pin	Configuration	I/O port configuration
OTG_FS_SOF	Host	Push-pull multiplexing output, if used
	Device	Push-pull multiplexing output, if used
	OTG	Push-pull multiplexing output, if used
OTG_FS_VBUS	Host	Floating input
	Device	Floating input
	OTG	Floating input
OTG_FS_ID	Host	No need if the force host mode is selected
	Device	No need if the force device mode is selected
	OTG	Pull-up input

USB OTG_FS pin	Configuration	I/O port configuration
OTG_FS_DM	Host	Controlled automatically by the USB power-down
	Device	Controlled automatically by the USB power-down
	OTG	Controlled automatically by the USB power-down
OTG_FS_DP	Host	Controlled automatically by the USB power-down
	Device	Controlled automatically by the USB power-down
	OTG	Controlled automatically by the USB power-down

Note: If the OTG_FS_VBUS pin (PA9) is used by another peripheral or as a general-purpose I/O, the PHY Power-down mode has to be enabled (OTG_FS_GGCCFG[PWEN]=0).

Table 38 ADC/DAC Pin Configuration

ADC/DAC pin	I/O port configuration
ADC/DAC	Analog input

Table 39 Other Pins Configuration

Pins	I/O port configuration
MCO	Push-pull multiplexing output
EINT input lines	Floating input/ pull-up input/ pull-down input

12.2.3 Remapping Function Configuration

Generally, after the system reset, the pin will be given a default function; then if the user needs to multiplex other functions of the pin, as long as the peripheral is enabled, the multiplexing function can be activated. However, in addition that some peripheral functions need to be enabled, software programming is also needed to map the signal to the port, that is, assign the pin address, so that the peripheral function can be used in the pin.

The multiplexing function and remapping address table of pins are shown in the *Data Manual*.

12.2.3.1 OSC32_IN (OUT) pin is configured as GPIO

When not entering the standby mode or V_{DD} is not used for power supply, when LSECLK oscillator is closed, the pin OSC32_IN/OSC32_OUT can be used as general I/O port PC14/PC15, namely, LSECLK function is prior to general I/O function.

12.2.3.2 OSC_IN (OUT) pin is configured as GPIO

In package products with less than 100 pins, the user can set AFIO_REMAP1/2 (multiplexing remapping and debug I/O configuration register) to realize the remapping of general I/O PD0/PD1 to external oscillator pin OSC_IN/OSC_OUT. Then PD0 and PD1 cannot be used to generate external interrupt time.

12.3 Register Address Mapping

Table 48 AFIO Register Address Mapping

Register name	Description	Offset address
AFIO_EVCTRL	Event control register	0x00
AFIO_REMAP	Multiplexing remapping configuration register	0x04
AFIO_EINTSEL1	External interrupt configuration register 1	0x08
AFIO_EINTSEL2	External interrupt configuration register 2	0x0C
AFIO_EINTSEL3	External interrupt configuration register 3	0x10
AFIO_EINTSEL4	External interrupt configuration register 4	0x14

12.4 Register Functional Description

For the register AFIO_EVCTRL, before read and write operation of AFIO_REMAP1/2 and AFIO_EINTSELx, AFIO clock shall be opened first. APB2 peripheral cock enable register (RCM_APB2CLKEN). These peripheral registers must be operated by word (32 bits).

12.4.1 Event control register (AFIO_EVCTRL)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	PINSEL	R/W	Portx Piny Select (x=A…E) Pin y (y=0…15) Select the pin for outputting EVENTOUT signal of the core: 0000: Select Px0 0001: Select Px1 0010: Select Px2 0011: Select Px3 0100: Select Px4 0101: Select Px5 0110: Select Px6 0111: Select Px7 1000: Select Px8 1001: Select Px9 1010: Select Px10 1011: Select Px11 1100: Select Px12 1101: Select Px13 1110: Select Px14 1111: Select Px15

Field	Name	R/W	Description
6:4	PORTSEL	R/W	Portx Select Select the port for outputting EVENTOUT signal of the core (The EVENTOUT signal output capability is not extended to ports PF and PG): 000: Select PA 001: Select PB 010: Select PC 011: Select PD 100: Select PE Others: Reserved
7	EVOEN	R/W	Event Output Enable 0: Disable 1: Enable the EVENTOUT of the core to connect to Port x Pin y selected by PORTSEL and PINSEL.
31:8	Reserved		

12.4.2 Multiplexing remapping configuration register (AFIO_REMAP)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SPI1RMP	R/W	SPI1 Remap Configure 0: No remapping NSS—PA4, SCK—PA5, MISO—PA6, MOSI—PA7 1: Remapping NSS—PA15, SCK—PB3, MISO—PB4, MOSI—PB5
1	I2C1RMP	R/W	I2C1 Remap Configure 0: No remapping SCL—PB6, SDA—PB7 1: Remapping SCL—PB8, SDA—PB9
2	USART1RMP	R/W	USART1 Remap Configure 0: No remapping TX—PA9, RX—PA10 1: Remapping TX—PB6, RX—PB7
3	USART2RMP	R/W	USART2 Remap Configure 0: No remapping CTS—PA0, RTS—PA1, TX—PA2, RX—PA3, CK—PA4 1: Remapping CTS—PD3, RTS—PD4, TX—PD5, RX—PD6, CK—PD7
5:4	USART3RMP	R/W	USART3 Remap Configure 00: No remapping TX—PB10, RX—PB11, CK—PB12, CTS—PB13, RTS—PB14 01: Partial remapping

Field	Name	R/W	Description
			TX—PC10, RX—PC11, CK—PC12, CTS—PB13, RTS—PB14 10: No effect 11: Complete remapping TX—PD8, RX—PD9, CK—PD10, CTS—PD11, RTS—PD12
7:6	TMR1RMP	R/W	TMR1 Remap Configure 00: No remapping ETR—PA12, CH1—PA8, CH2—PA9, CH3—PA10, CH4—PA11, BKIN—PB12, CH1N—PB13, CH2N—PB14, CH3N—PB15 01: Partial mapping ETR—PA12, CH1—PA8, CH2—PA9, CH3—PA10, CH4—PA11, BKIN—PA6, CH1N—PA7, CH2N—PB0, CH3N—PB1 10: No effect 11: Complete mapping ETR—PE7, CH1—PE9, CH2—PE11, CH3—PE13, CH4—PE14, BKIN—PE15, CH1N—PE8, CH2N—PE10, CH3N—PE12
9:8	TMR2RMP	R/W	TMR2 Remap Configure 00: No remapping CH1/ETR—PA0, CH2—PA1, CH3—PA2, CH4—PA3 01: Partial remapping CH1/ETR—PA15, CH2—PB3, CH3—PA2, CH4—PA3 10: Partial remapping CH1/ETR—PA0, CH2—PA1, CH3—PB10, CH4—PB11 11: Complete remapping CH1/ETR—PA15, CH2—PB3, CH3—PB10, CH4—PB11
11:10	TMR3RMP	R/W	TMR3 Remap Configure 00: No remapping CH1—PA6, CH2—PA7, CH3—PB0, CH4—PB1 01: No effect 10: Partial mapping CH1—PB4, CH2—PB5, CH3—PB0, CH4—PB1 11: Complete mapping CH1—PC6, CH2—PC7, CH3—PC8, CH4—PC9 Note: Remapping does not affect TMR3_ETR on PE0.
12	TMR4RMP	R/W	TMR4 Remap Configure 0: No remapping TMR4_CH1—PB6, TMR4_CH2—PB7, TMR4_CH3—PB8, TMR4_CH4—PB9 1: Complete mapping TMR4_CH1—PD12, TMR4_CH2—PD13, TMR4_CH3—PD14, TMR4_CH4—PD15 Note: Remapping does not affect TMR4_ETR on PE0.
14:13	CAN1RMP	R/W	CAN1 Remap Configure

Field	Name	R/W	Description
			00: CAN1_RX mapped to PA11, CAN1_TX mapped to PA12 01: No effect 10: CAN1_RX mapped to PB8, CAN1_TX mapped to PB9 11: CAN1_RX mapped to PD0, CAN1_TX mapped to PD1
15	PD01RMP	R/W	Port D0/Port D1 mapping on OSC_IN/OSC_OUT Configure This function can only be used for Pin 64 package (PD0 and PD1 appear on Pin 100 package without remapping). 0: No remapping for PD0 and PD1 1: PD0 mapped to OSC_IN, PD1 mapped to OSC_OUT When the main oscillator HSECLK is not used (the system runs in internal 8MHz resistance-capacitance oscillator), PD0 and PD1 can be mapped to OSC_IN and OSC_OUT pins.
16	TMR5CH4IRMP	R/W	TMR5CH4 Interrupt Remap This bit can be set to 1 or cleared by software. It controls internal mapping of TMR5 Channel 4. 0: TMR5_CH4 is connected to PA3; 1: LSICLK internal oscillator is connected to TMR5_CH4 for calibration of LSICLK.
20:17	Reserved		
21	MACRMP	R/W	Ethernet MAC Remap Configure 0: No remapping RX_DV-CRS_DV—PA7，RXD0—PC4，RXD1—PC5，PXD2—PB0，RXD3—PB1 1: Remapping RX_DV-CRS_DV—PD8，RXD0—PD9，RXD1—PD10，PXD2—PD11，RXD3—PD12
22	CAN2RMP	R/W	CAN2 Remap Configure 0: No remapping CAN2_RX—PB12, CAN2_TX—PB13 1: Remapping CAN2_RX—PB5, CAN2_TX—PB6
23	MACEISEL	R/W	Ethernet MAC External Interface Select Set 1 or clear 0 by software. 0: Select PHY of external MII interface 1: Select PHY of external RMII interface
26:24	SWJCFG	W	Serial Wire JTAG Configure Configure SWJ and tracking multiplexing function I/O as debugging I/O or normal I/O, applicable when GPIO is not enough. These bits can only be written by software (read these bits and undefined values will be returned). SWJ (serial line JTAG) supports JTAG or SWD to access the debug port of Cortex. The default state after system reset is enabled SWJ without tracking function.

Field	Name	R/W	Description
			000: Complete SWJ (JTAG-DP+SW-DP) 001: Complete SWJ (JTAG-DP+SW-DP) but without NJTRST 010: JTAG-DP disabled, SW-DP enabled 100: JTAG-DP disabled, SW-DP disabled Others: Reserved
27	Reserved		
28	SPI3RMP	R/W	SPI3 Remap Se1 or clear 0 by software. This bit controls the multiplexing of NSS, SCK, MISO and MOSI of SPI3 at ports. 0: No remapping NSS—PA15，SCK—PB3，MISO—PB 4，MOSI—PB5 1: Remapping NSS—PA4，SCK—PC10，MISO—PC11，MOSI—PC12
29	TMR2ITR1RMP	R/W	TMR2 ITR1 Remap Set 1 or clear 0 by software. For calibration, this bit controls the internal remapping of ITR1 of TMR2. 0: TMR2_ITR1 connects to PTP output of Ethernet 1: TMR2_ITR1 is connected to SOF output of USB OTG_FS
30	PTPPPSRMP	R/W	Ethernet MAC PTP_PPS Remap Set 1 or clear 0 by software. This bit controls the remapping of PTP_PPS for Ethernet MACs. 0: No remapping. PTP_PPS is not output from PB5. 1: No remapping. PTP_PPS can be output from PB5.
31	Reserved		

12.4.3 External interrupt configuration register 1 (AFIO_EINTSEL1)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	EINTx[3:0]	R/W	EINTx Input Source Select 0000: PA[x] pin 0001: PB[x] pin 0010: PC[x] pin 0011: PD[x] pin 0100: PE[x] pin Others: Reserved
31:16	Reserved		

12.4.4 External interrupt configuration register 2 (AFIO_EINTSEL2)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	EINTx[3:0]	R/W	EINTx Input Source Select (x=4…7) 0000: PA[x] pin 0001: PB[x] pin 0010: PC[x] pin 0011: PD[x] pin 0100: PE[x] pin Others: Reserved
31:16	Reserved		

12.4.5 External interrupt configuration register 3 (AFIO_EINTSEL3)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	EINTx[3:0]	R/W	EINTx Input Source Select (x=8…11) 0000: PA[x] pin 0001: PB[x] pin 0010: PC[x] pin 0011: PD[x] pin 0100: PE[x] pin Others: Reserved
31:16	Reserved		

12.4.6 External interrupt configuration register 4 (AFIO_EINTSEL4)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	EINTx[3:0]	R/W	EINTx Input Source Select (x=12…15) 0000: PA[x] pin 0001: PB[x] pin 0010: PC[x] pin 0011: PD[x] pin 0100: PE[x] pin Others: Reserved
31:16	Reserved		

13 Timer Overview

13.1 Full Name and Abbreviation Description of Terms

Table 40 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Timer	TMR
Update	U
Request	R
Event	EV
Capture	C
Compare	C
Length	LEN

13.2 Timer Category and Main Difference

In this series of products, there are three types of timers: advanced timer, general-purpose timer and basic timer (watchdog timer and system tick timer are described in other chapters).

The advanced timer includes the functions of general-purpose timer and basic timer. The advanced timer has four capture/compare channels, supports timing function, input capture and output compare function, braking and complementary output function, and is a 16-bit timer that can count up/down.

The function of general-purpose timer is simpler than that of advanced timer. The main differences are the total number of channels, the number of complementary output channel groups and the braking function.

The basic timer is a timer that can only realize timing function and has no external interface.

The main differences of timers included in the products are shown in the table below:

Table 50 Main Differences among Timers Included in the Products

Item	Specific content/Category	Advanced timer		General-purpose timer	Basic timer	
Name	—	TMR1	TMR8	TMR2/3/4/5	TMR6	TMR7
Timebase unit	Counter	16 bits		16 bits	16 bits	
	Prescaler	16 bits		16 bits	16 bits	

Item	Specific content/Category	Advanced timer	General-purpose timer	Basic timer
	Count mode	Up Down Center-aligned	Up Down Center-aligned	Up
Channel	Input channel	4	4	0
	Capture/Compare channel	4	4	0
	Output channel	7	4	0
	Complementary output channel	3 groups	0	0
Function	General DMA request	OK	OK	OK
	PWM mode	Yes	Yes	None
	Single-pulse mode	Yes	Yes	None
	Forced output mode	Yes	Yes	None
	Dead zone insertion	Yes	None	None

Timer term

Table 41 Definitions and Terms of Pins

Name	Description
TMRx_ETR	External trigger signal of Timer x
TMRx_CH1、TMRx_CH2、TMRx_CH3、TMRx_CH4	Channel 1/2/3/4 of Timer x
TMRx_ChyN	Complementary output channel y of Timer x
TMRx_BKIN	Braking signal of Timer x

Table 42 Definitions and Terms of Internal Signals

Name	Description
ETR	TMRx_ETR external trigger signal
ETRF	External trigger filter
ETRP	External trigger prescaler
-	
ITR, ITR0, ITR1	Internal trigger
TRGI	Clock/Trigger/Slave mode controller trigger input

Name	Description
TIF_ED	Timer input filter edge detection
-	
CK_PSC	Prescaler clock
CK_CNT	Counter clock
PSC	Prescaler
CNT	Counter
AUTORLD	Autoload register
-	
TIx, TI1	Timer input
TIxF, TI1F,	Timer input filter
TI1_ED	Timer input edge detection
TIxFPx, TI1FP1	Timer input filter polarity
ICx, IC1	Input capture
ICxPS, IC1PS	Input capture prescaler
TRC	Trigger capture
BRK	Braking signal
-	
OCx, OC1	Timer output coparison channel
OCxREF, OC1REF	Output compare reference signal
-	
TGI	Trigger interrupt
BI	Braking interrupt
CCxI, CC1I	Capture/Compare interrupt
UEV	Update event
UIFLG	Update interrupt flag

14 Advanced Timer (TMR1)

14.1 Introduction

The advanced timer takes the time base unit as the core, and has the functions of input capture, output comparison and braking input, including a 16-bit auto reload counter. Compared with other timers, the advanced timer supports complementary output, repeat count and programmable dead zone insertion function, and is more suitable for motor control.

14.2 Main Characteristics

（1） Timebase unit
- Counter: 16-bit counter, count-up, count-down and Center-aligned count
- Prescaler: 16-bit programmable prescaler
- Repeat counter: 16-bit repeat counter
- Auto reloading function

（2） Clock source selection
- Internal clock
- External input
- External trigger
- Internal trigger

（3） Input capture function
- Counting function
- PWM input mode (measurement of pulse width, frequency and duty cycle)
- Encoder interface mode

（4） Output comparison function
- PWM output mode
- Forced output mode
- Single-pulse mode
- Complementary output and dead zone insertion

（5） Timing function

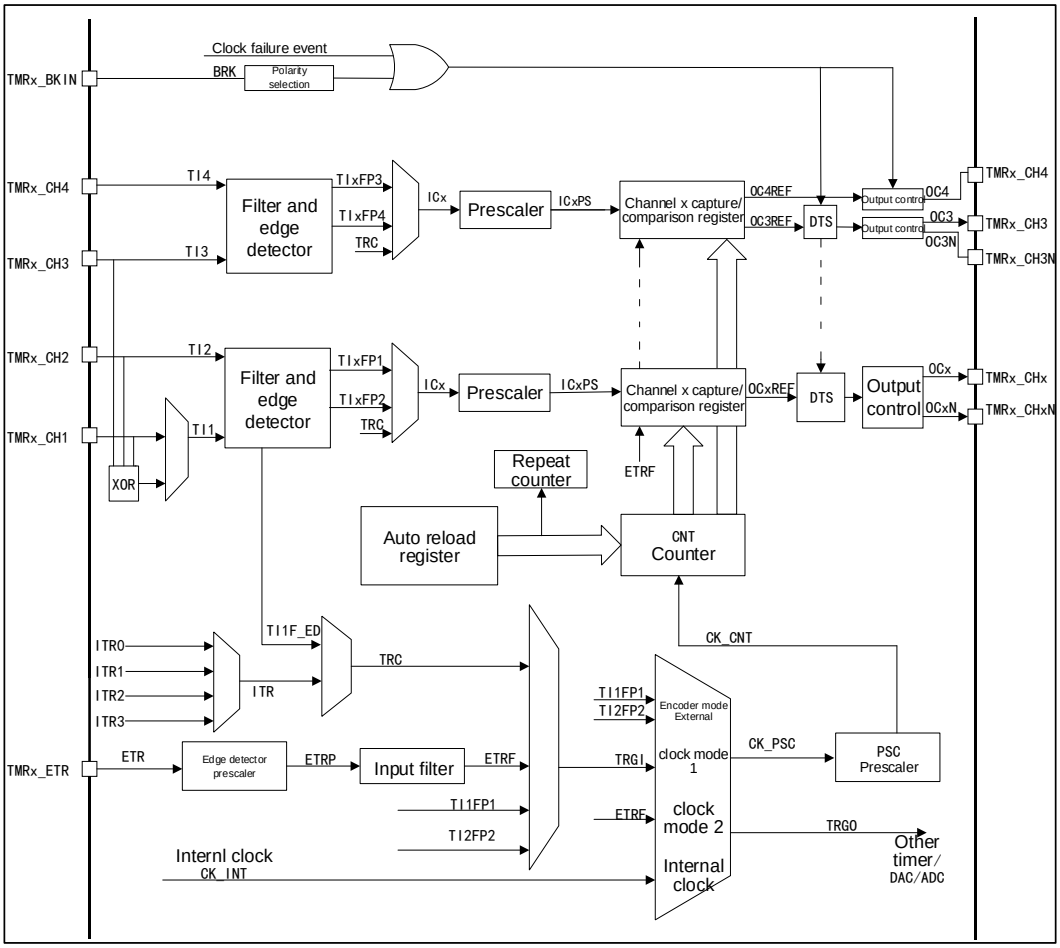
（6） Braking function

（7） Master/Slave mode controller of timer
- Timers can be synchronized and cascaded
- Support multiple slave modes and synchronization signals

（8） Interrupt output and DMA request event
- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Comparison event
- Braking signal input event

14.3 Structure Block Diagram

Figure 21 Advanced Timer Structure Block Diagram



14.4 Functional Description

14.4.1 Clock Source Selection

The advanced timer has four clock sources

Internal clock

It is TMRx_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

External clock mode 1

The trigger signal generated from the input channel TI1/2/3/4 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of Channel 1 after double-edge detection of the rising edge and the falling edge is logically equal or the future signal is TI1F_ED signal, namely double-edge signal of TIF_ED. Specially the PWM input can only be input by TI1/2.

External clock mode 2

After polarity selection, frequency division and filtering, the signal from external trigger interface (ETR) is connected to slave mode controller through trigger input selector to control the work of counter.

Internal trigger input

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

14.4.2 Timebase Unit

The time base unit in the advanced timer contains four registers

- Counter register (CNT) 16 bits
- Auto reload register (AUTORLD) 16 bits
- Prescaler register (PSC) 16 bits
- Repeat count register (REPCNT) 8 bits

Repeat count register is unique to advanced timer.

Counter CNT

There are three counting modes for the counter in the advanced timer

- Count-up mode
- Count-down mode
- Center-aligned mode

Count-up mode

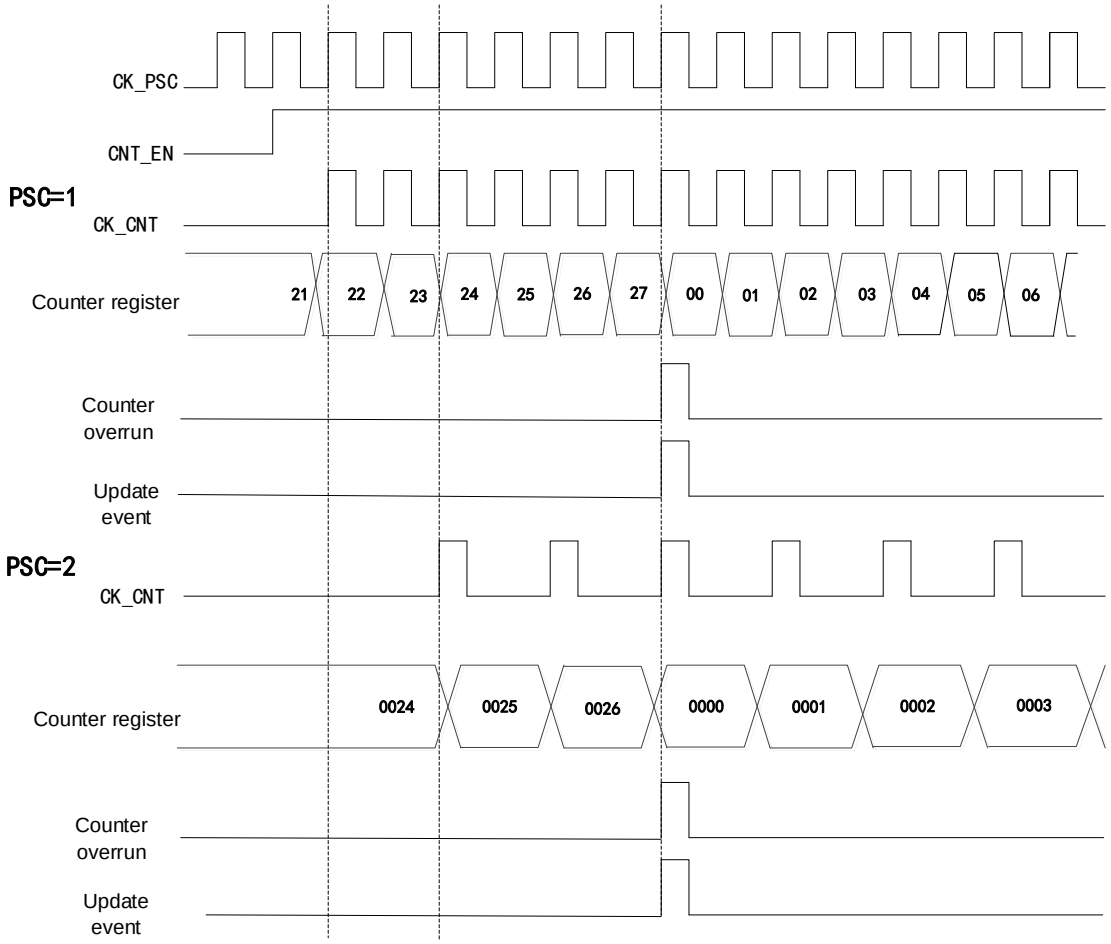
Set to the count-up mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx_CNT) is equal to the value of the auto reload (TMRx_AUTORLD), the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMRx_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by UD bit of configuration control register TMRx_CTRL1.

The figure below is Timing Diagram when Division Factor is 1 or 2 in Count-up Mode

Figure 22 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



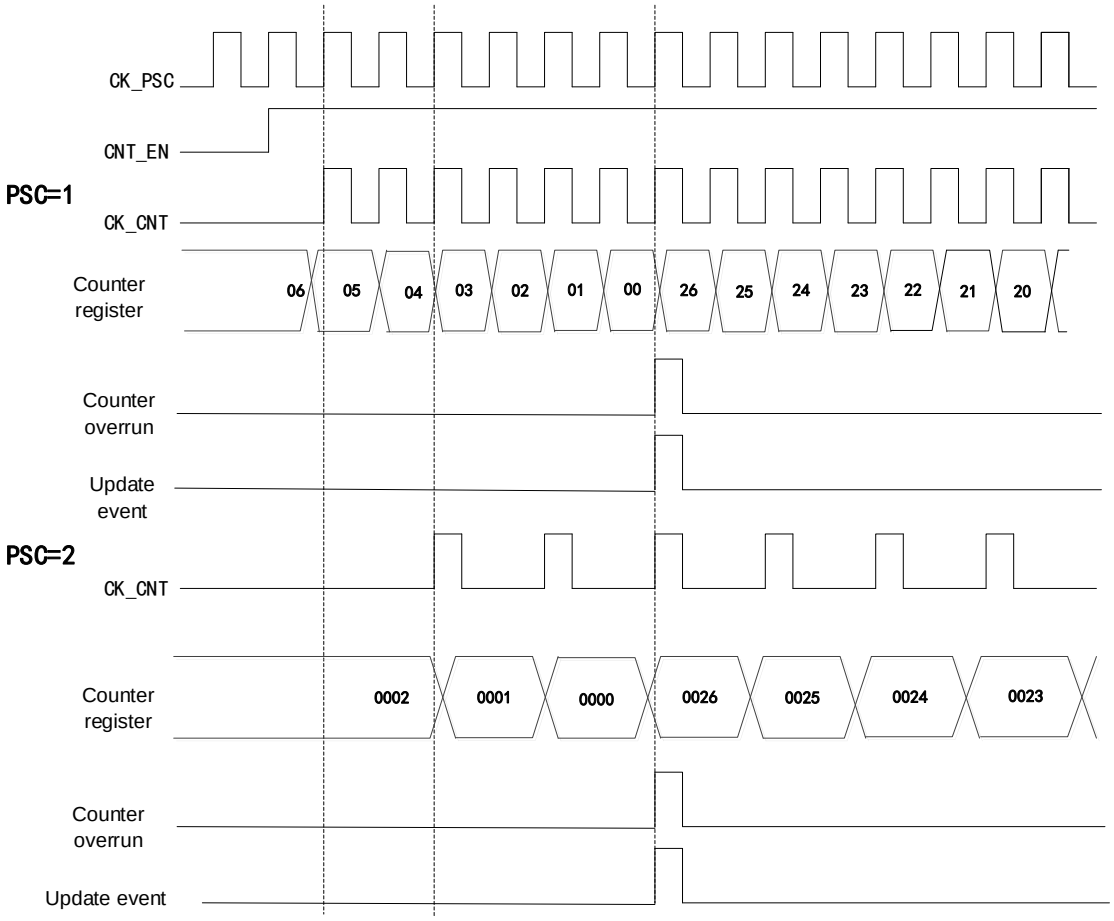
Count-down mode

Set to the count-down mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in count-down mode, the counter will start to count down from the value of the auto reload (TMRx_AUTORLD); every time a pulse is generated, the counter will decrease by 1 and when it becomes 0, the counter will start to count again from (TMRx_AUTORLD), meanwhile, a count-down overrun event will be generated, and the value of the auto reload (TMRx_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by configuring the UD bit of the TMRx_CTRL1 register.

Figure 23 Timing Diagram when Division Factor is 1 or 2 in Count-down Mode

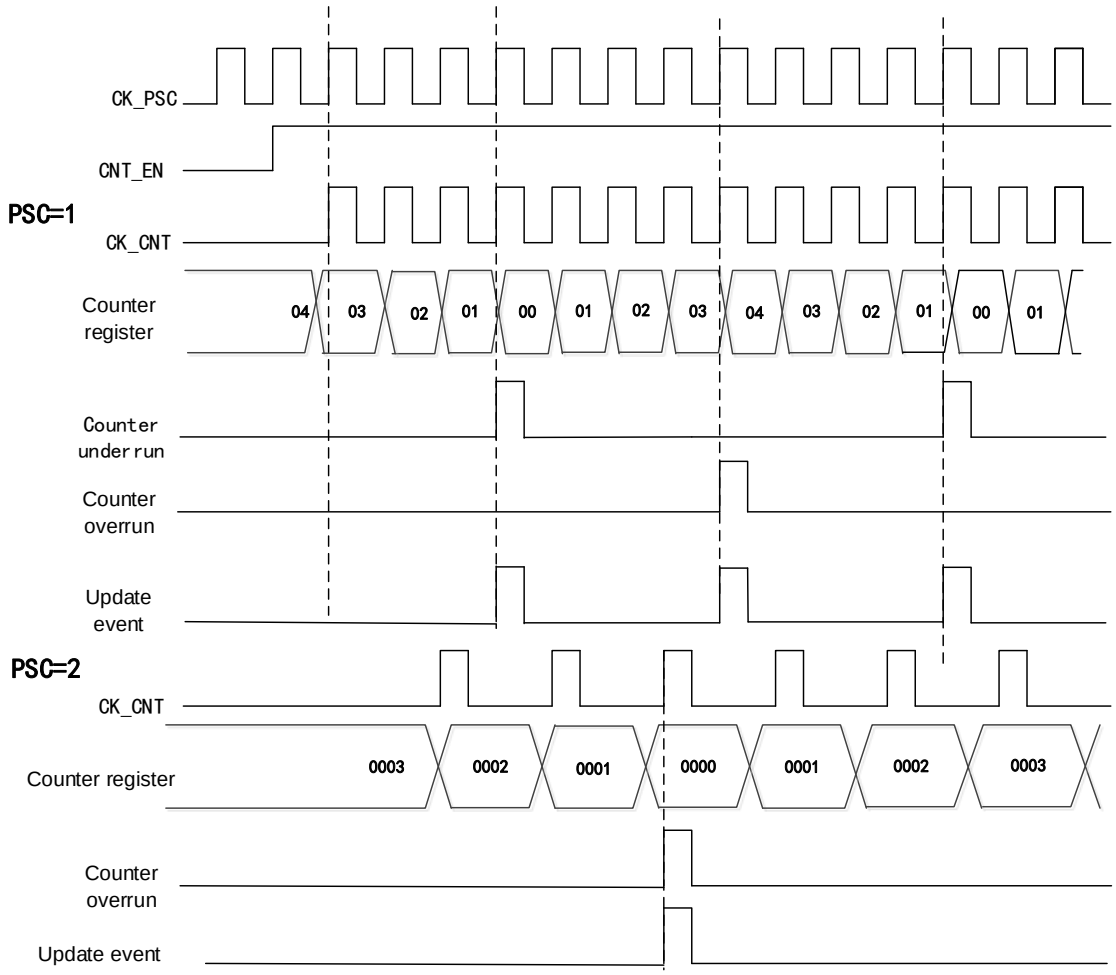


Center-aligned mode

Set to the Center-aligned mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in Center-aligned mode, the counter counts up from 0 to the value of auto reload (TMRx_AUTORLD), then counts down to 0 from the value of the auto reload (TMRx_AUTORLD), which will repeat; in counting up, when the counter value is (AUTORLD-1), a counter overrun event will be generated; in counting down, when the counter value is 1, a counter underrun event will be generated.

Figure 24 Timing Diagram when Division Factor is 1 or 2 in Center-aligned Mode



Repeat counter REPCNT

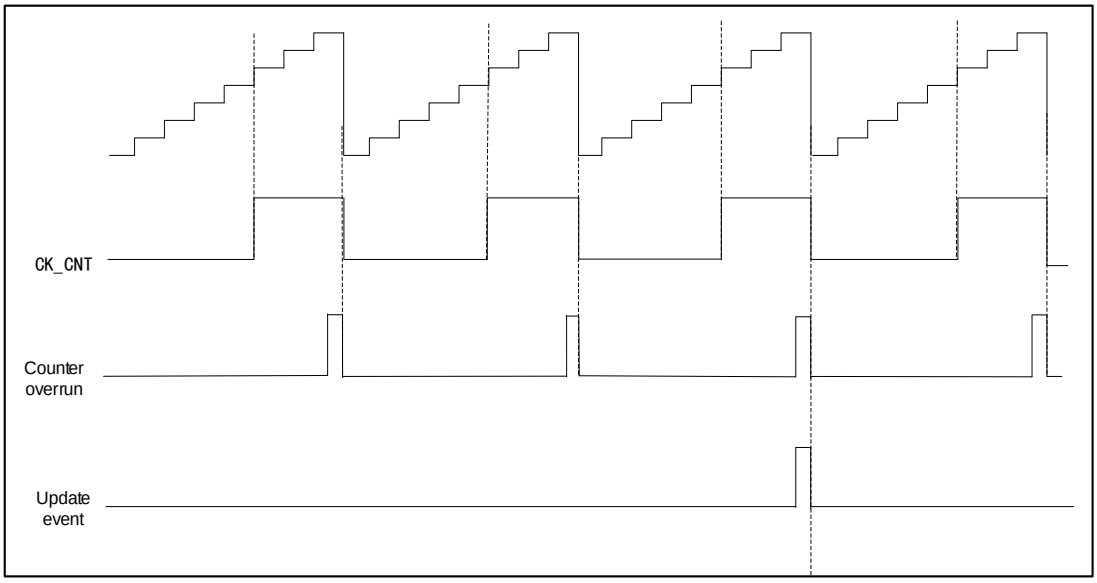
There is no repeat counter REPCNT in the basic/general-purpose timer, which means that when the overrun event or underrun event occurs in the basic/general-purpose timer, an update event will be generated directly; while in the advanced timer, because of the existence of the repeat counter, when an overrun/underrun event occurs to the advanced timer, the update event will be generated only when the value of the repeat counter is 0.

For example, if the advanced timer needs to generate an update event when an overrun/underrun event occurs, the value of the repeat counter should be set to 0.

If the repeat counter function is used in the count-up mode, every time the counter counts up to AUTORLD, an overrun event will occur. At this time, the value of the repeat counter will be decreased by 1, and an update event will be generated until the value of the repeat counter is 0.

That is, when N+1 (N is the value of repeat counter) overrun/underrun events occur, an update event will be generated.

Figure 25 Timing Diagram when Setting REPCNT=2 in Count-up Mode



Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMRx_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

14.4.3 Input Capture

Input capture channel

The advanced timer has four independent capture/comparison channels, each of which is surrounded by a capture/comparison register.

In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the signal will pass through the prescaler, which is used to set how many events to capture at a time.

Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMRx_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMRx_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, cycle and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be

recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

14.4.4 Output Comparison

There are eight modes of output comparison: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is valid, PWM1 and PWM2 modes, which are configured by OCxMOD bit in TMRx_CCMx register and can control the waveform of output signal in output comparison mode.

Output comparison application

In the output comparison mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/comparison register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMRx_CCMx register and the CCxPOL bit in the output polarity TMRx_CCEN register.

When CCxIFLG=1 in TMRx_STS register, if CCxIEN=1 in TMRx_DIEN register, an interrupt will be generated; if CCDSEL=1 in TMRx_CTRL2 register, DMA request will be generated.

14.4.5 PWM Output Mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the comparison register CCx, and the cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 are divided into count-up, count-down and edge alignment counting; in PWM mode 1, if the value of the counter CNT is less than the value of the comparison register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM1 mode when CCx=5, AUTORLD=7

Figure 26 PWM1 Count-up Mode Timing Diagram

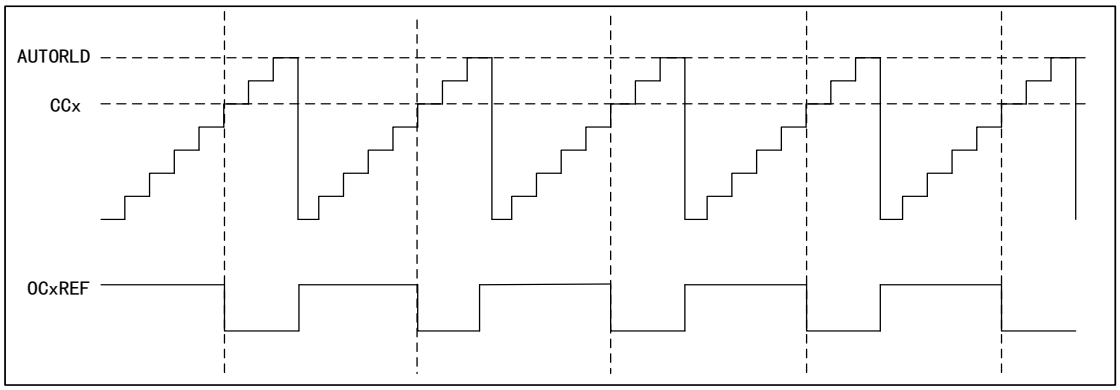


Figure 27 PWM1 Count-down Mode Timing Diagram

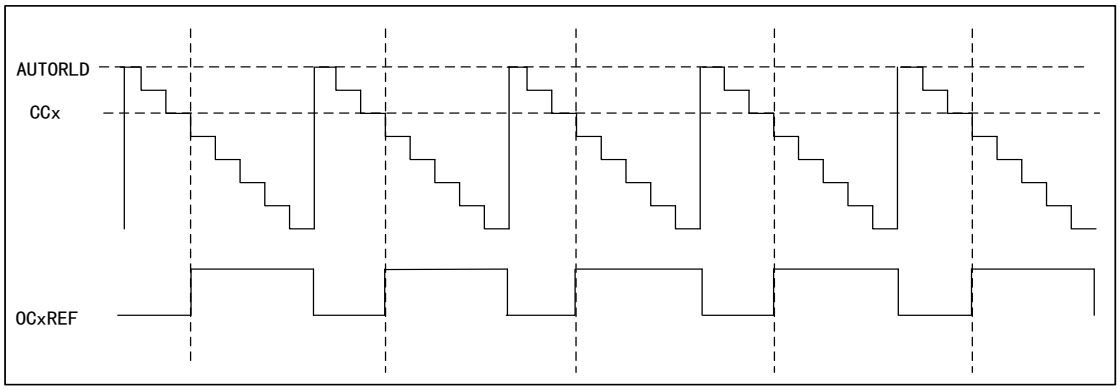
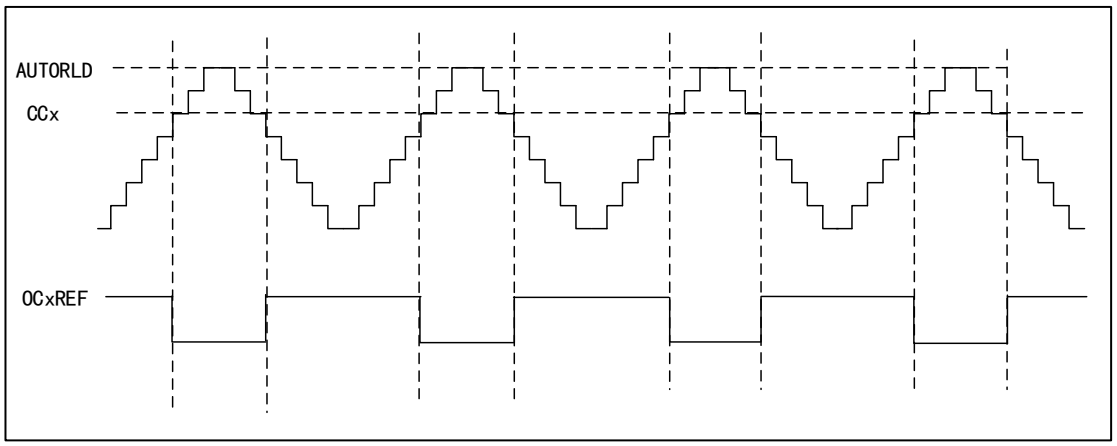


Figure 28 PWM1 Center-aligned Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the comparison register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM2 mode when CCx=5, AUTORLD=7

Figure 29 PWM2 Count-up Mode Timing Diagram

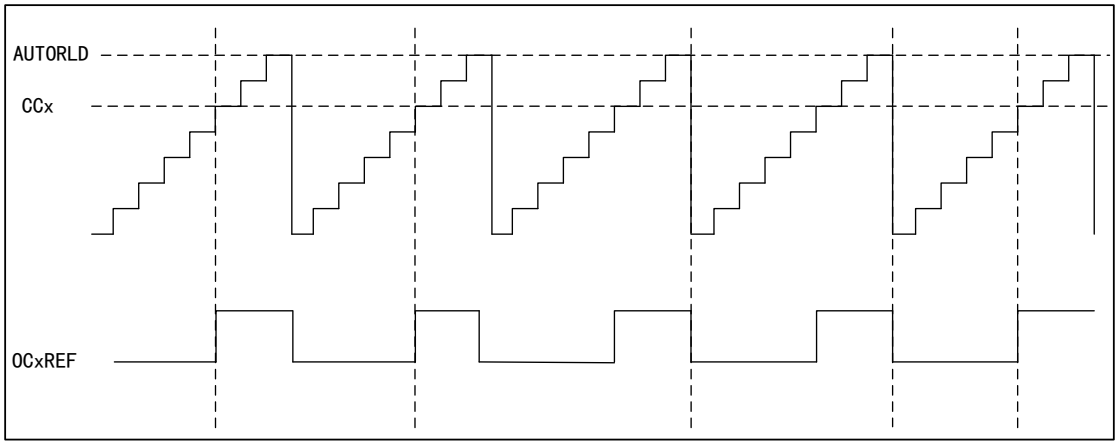


Figure 30 PWM2 Count-down Mode Timing Diagram

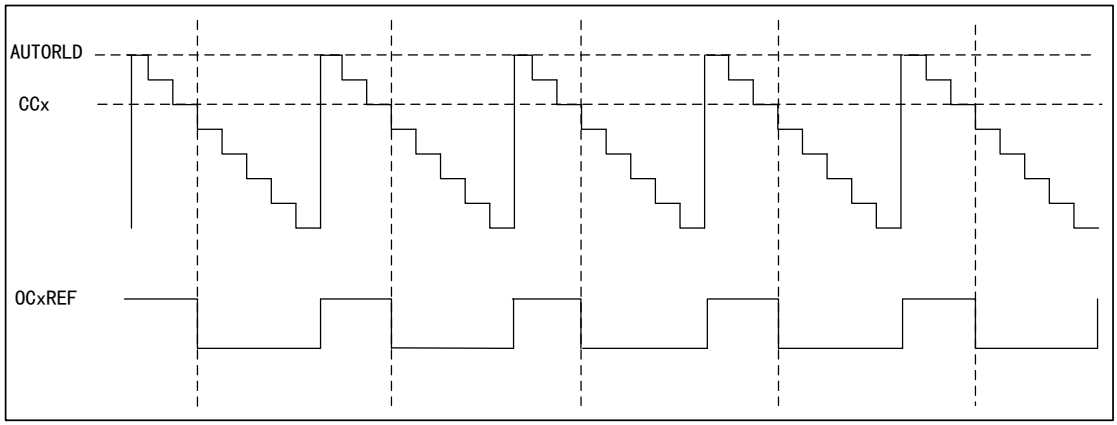
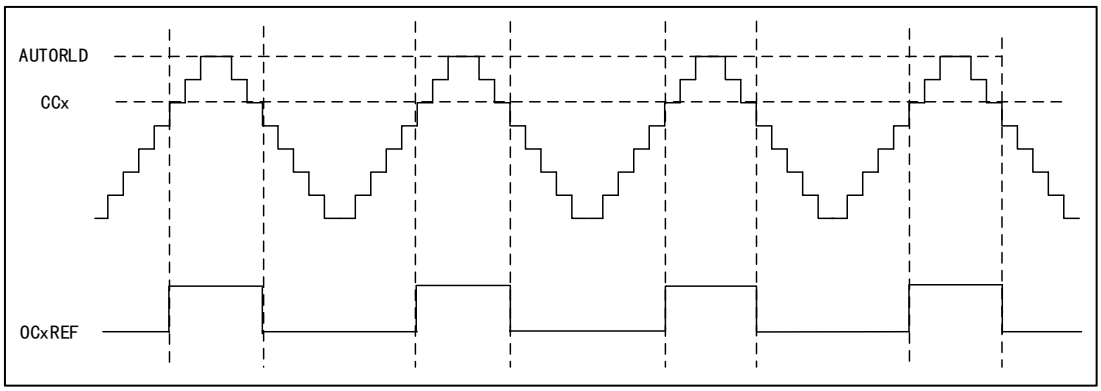


Figure 31 PWM2 Center-aligned Mode Timing Diagram



14.4.6 PWM Input Mode

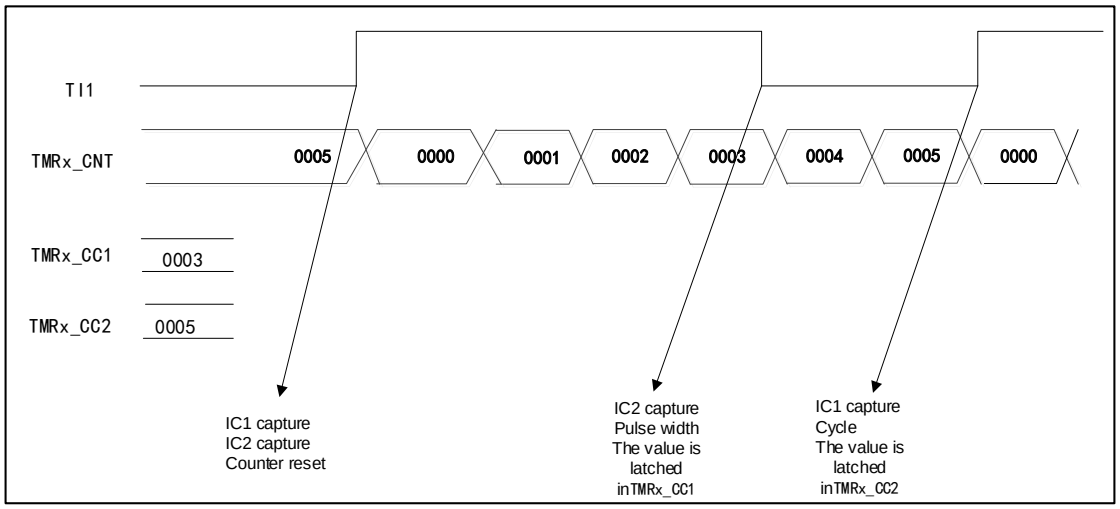
PWM input mode is a particular case of input capture.

In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave mode controller, input can be performed only through the channels TMRx_CH1 and TMRx_CH2, which need to occupy the capure registers of CH1 and CH2.

In the PWM input mode, the PWM signal enters from TMRx_CH1, and the signal will be divided into two channels, one can measure the cycle and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFSEL bit of TMRx_SMCTRL register)

Figure 32 PWM Input Mode Timing Diagram



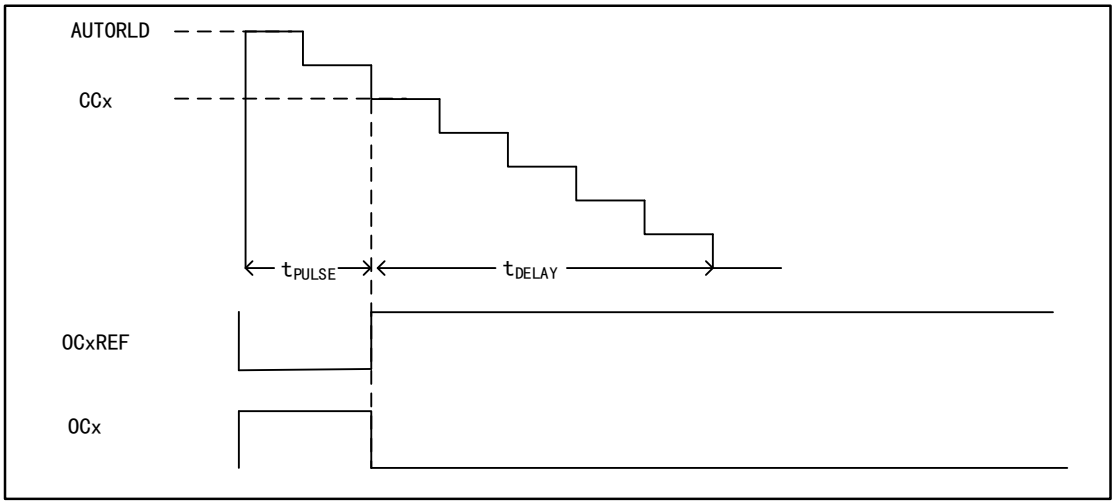
14.4.7 Single-pulse Mode

The single-pulse mode is a special case of timer comparison output, and is also a special case of PWM output mode.

Set SPMEN bit of TMRx_CTRL1 register, and select the single-pulse mode. After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMRx_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 33 Timing Diagram in Single-pulse Mode



14.4.8 Impact of the Register on Output Waveform

The following registers will affect the level of the timer output waveform. For details, please refer to "Register Functional Description".

（1） CCxEN and CCxNEN bits in TMRx_CCEN register
- CCxNEN=0 and CCxEN=0: The output is turned off (output disabled, invalid state)
- CCxNEN=1 and CCxEN=1: The output is turned on (output enabled, normal output)

（2） MOEN bit in TMRx_BDT register
- MOEN=0: Idle mode
- MOEN=1: Run mode

（3） OCxOIS and OCxNOIS bits in TMRx_CTRL2 register
- OCxOIS=0 amd OCxNOIS=0: When idle (MOEN=0), the output level after the dead zone is 0
- OCxOIS=1 amd OCxNOIS=1: When idle (MOEN=0), the output level after the dead zone is 1

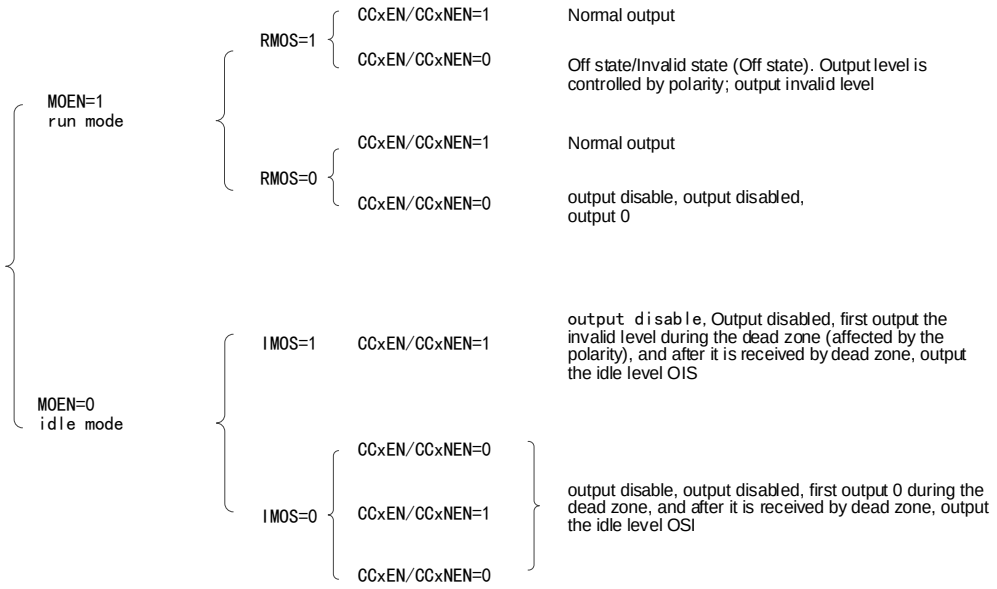
（4） RMOS bit in TMRx_BDT register
- Application environment of RMOS: In corresponding complementary channel and timer are in run mode (MOEN=1), the timer is not working (CCxEN=0, CCxNEN=0) or is working (CCxEN=1, CCxNEN=1)

（5） IMOS bit in TMRx_BDT register
- Application environment of IMOS: In corresponding complementary channel and timer are in idle mode (MOEN=0), the timer is not working (CCxEN=0, CCxNEN=0) or is working (CCxEN=1, CCxNEN=1)

（6） CCxPOL and CCxNPOL bits of TMRx_CCEN register
- CCxPOL=0 and CCxNPOL=0: Output polarity, high level is valid
  CCxPOL=1 and CCxNPOL=1: Output polarity, the low level is valid

The following figure lists the register structure relationships that affect the output waveform

Figure 34 Register Structural Relationship Affecting Output Waveform



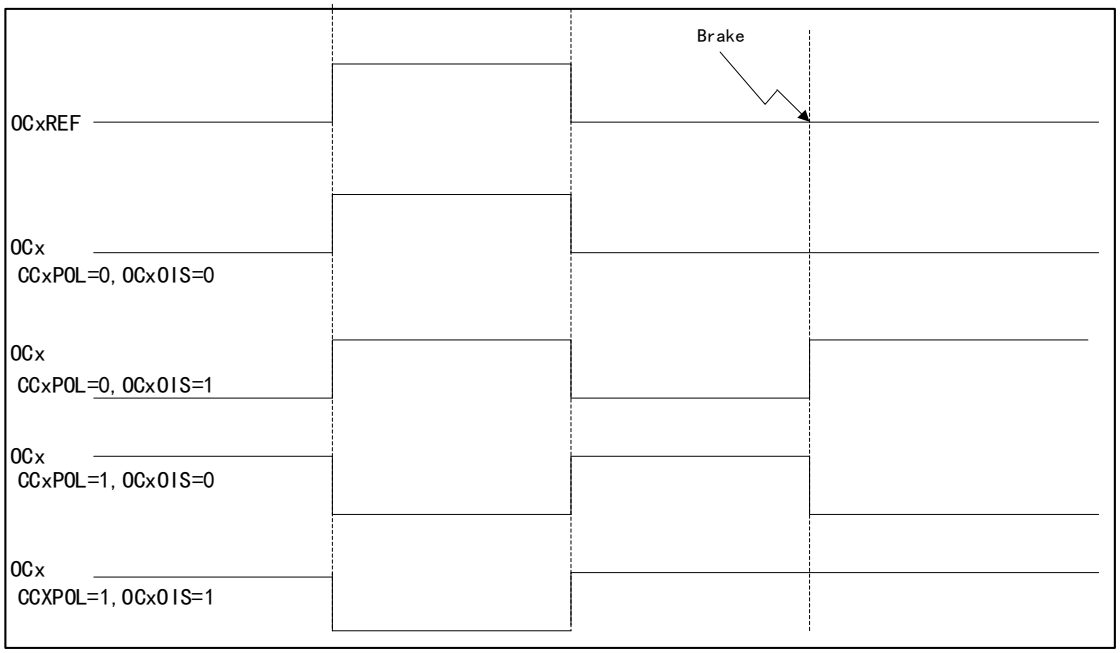
14.4.9 Braking Function

The signal source of braking is clock fault event and external input interface.

Besides, the BRKEN bit in TMRx_BDT register can enable the braking function, and the BRKPOL bit can configure the polarity of braking input signal.

When a braking event occurs, the output pulse signal level can be modified according to the state of the relevant control bit.

Figure 35 Braking Event Timing Diagram

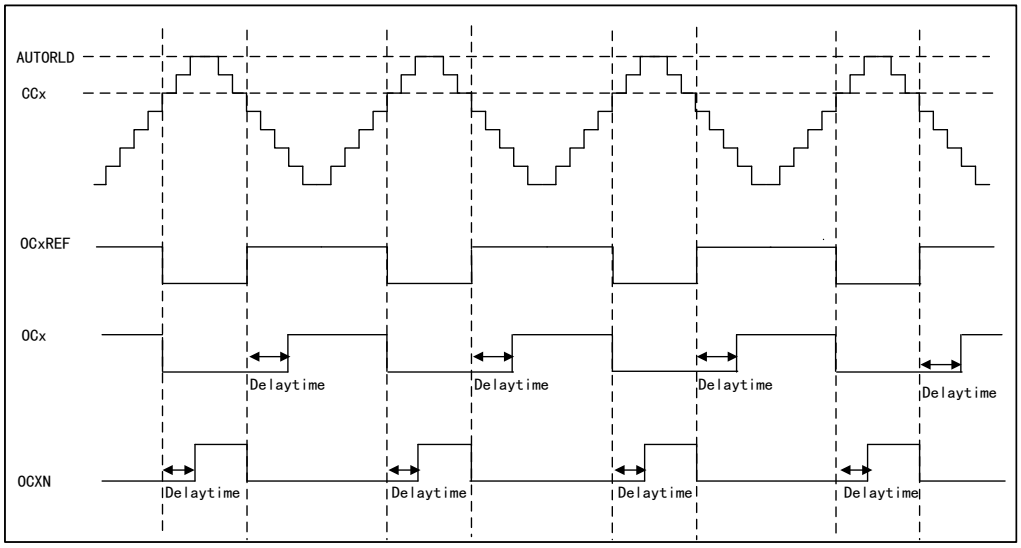


14.4.10 Complementary Output and Dead Zone Insertion

Complementary output is particular output of advanced timer, and the advanced timer has three groups of complementary output channels. The insertion dead time is used to generate complementary output signals to ensure that the two-way complementary signals of channels will not be valid at the same time. The dead time is set according to the output device connected to the timer and its characteristics

The duration of the dead zone can be controlled by configuring DTS bit of TMRx_BDT register

Figure 36 Complementary Output of Insertion with Dead Zone



14.4.11 Forced Output Mode

In the forced output mode, the comparison result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMRx_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMRx_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt and DMA request will still be generated.

14.4.12 Encoder Interface Mode

The encoder interface mode is equivalent to an external clock with direction selection. In the encoder interface mode, the content of the timer can always indicate the position of the encoder.

The selection methods of encoder interface is as follows:

- By setting SMFSEL bit of TMRx_SMCTRL register, set the counter to count on the edge of TI1 channel /TI2 channel, or count on the edge of TI1 and TI2 at the same time.
- Select the polarity of TI1 and TI2 by setting the CC1POL and CC2POL bits of TMRx_CCEN register.
- Select to filter or not by setting the IC1F and IC2F bits of TMRx_CCM1 register.

The two input TI1 and TI2 can be used as the interface of incremental encoder. The counter is driven by the effective jump of the signals TI1FP1 and TI2FP2 after filtering and edge selection in TI1 and TI2.

The count pulse and direction signal are generated according to the input signals of TI1 and TI2

- The counter will count up/down according to the jumping sequence of the input signal.
- Set CNTDIR of control register TMRx_CTRL1 to be read-only (CNTDIR will be re-calculated due to jumping of any input end).

The change mechanism of counter count direction is shown in the figure below

Table 43 Relationship between Count Direction and Encoder

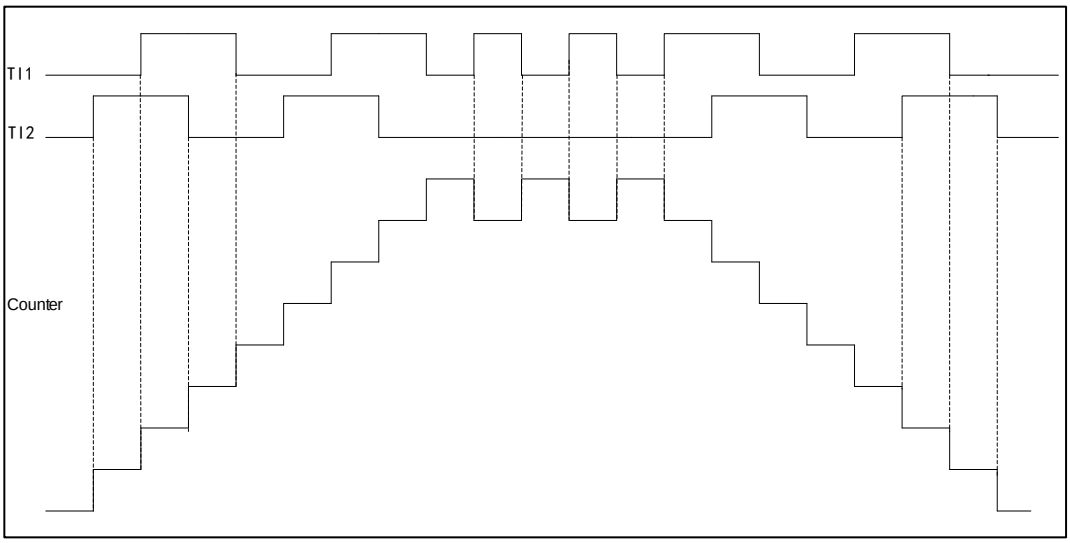
Effective edge		Count only in TI1		Count only in TI2		Count in both TI1 and TI2	
Level of relative signal		High	Low	High	Low	High	Low
TI1FP1	Rising edge	—		Count down	Count up	Count down	Count up
	Falling edge			Count up	Count down	Count up	Count down
TI2FP2	Rising edge	Count up	Count down	—		Count up	Count down
	Falling edge	Count down	Count up			Count down	Count up

The external incremental encoder can be directly connected with MCU, not needing external interface logic, so the comparator is used to convert the differential output of the encoder to digital signal to increase the immunity from noise interference.

Among the following examples:

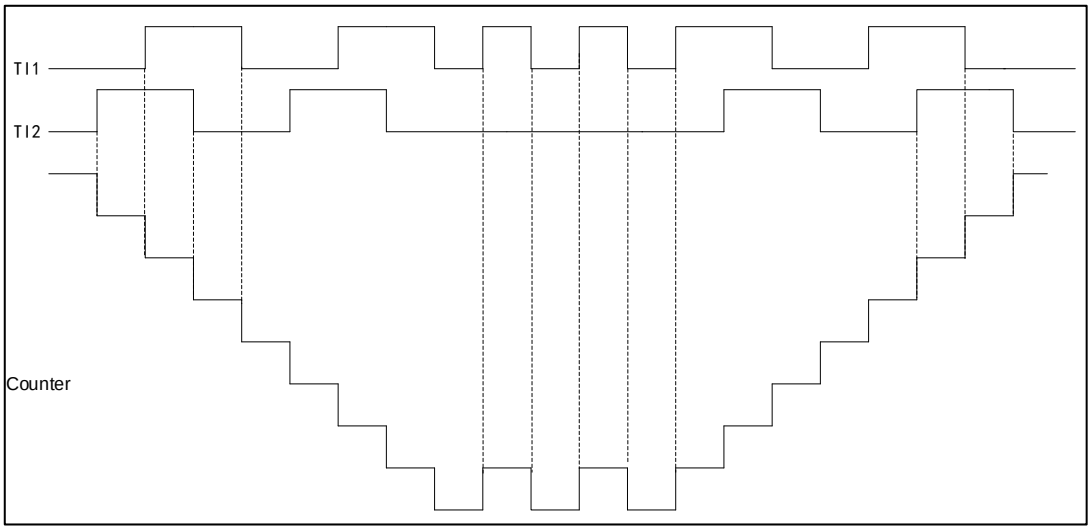
- TI1FP1 is mapped to TI1
- TI2FP2 is mapped to TI2
- Neither TI1FP1 nor TI2FP2 is reverse phase
- The input signal is valid at the rising edge and falling edge
- Enable the counter

Figure 37 Counter Operation Example in Encoder Mode



For example, when TI1 is at low level, and TI2 is in rising edge state, the counter will count up.

Figure 38 Example of Encoder Interface Mode of TI1FP1 Reversed Phase



For example, when TI1 is at low level, and the rising edge of TI2 jumps, the counter will count down.

14.4.13 Slave Mode

TMRx timer can synchronize external trigger

- Reset mode
- Gated mode
- Trigger mode

SMFSEL bit in TMRx_SMCTRL register can be set to select the mode.

SMFSEL=100 set the reset mode, SMFSEL=101 set the gated mode, SMFSEL=110 set the trigger mode.

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

In the gated mode, the enable of the counter depends on the high level of the selected input. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

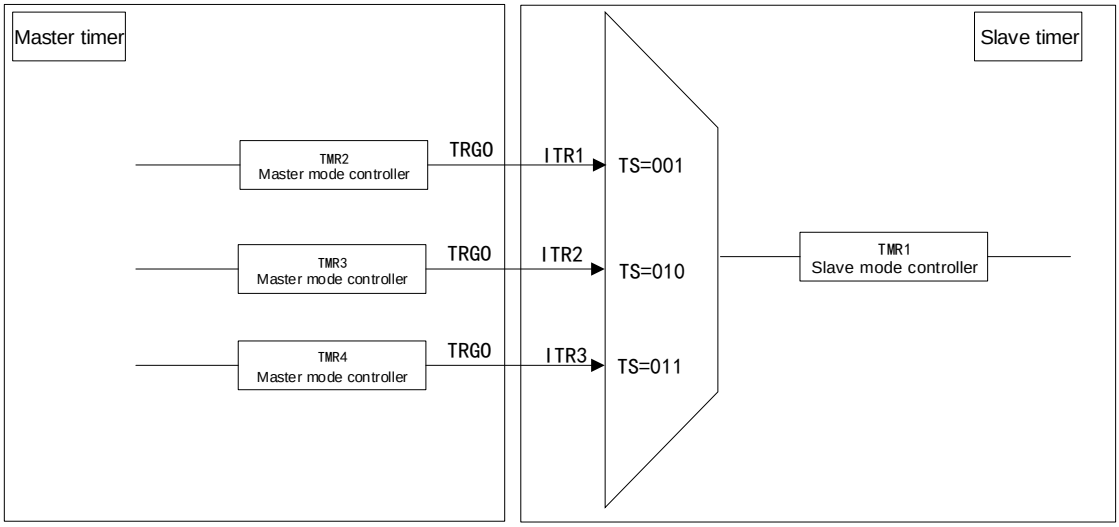
In the trigger mode, the enable of the counter depends on the event on the selected input, the counter is started (but is not reset) at the rising edge of the trigger input, and only the start of the counter is controlled.

14.4.14 Timer Interconnection

Each timer of TMRx can be connected with each other to realize synchronization or cascading between timers. It is required to configure one timer in master mode and the other timer in slave mode.

When the timer is in master mode, it can reset, start, stop and provide clock source for the counter of the slave mode timer.

Figure 39 Timer 1 Master/Slave Mode Example



When the timers are interconnected:

- A timer can be used as the prescaler of other register
- Another register can be started by the enable signal of a timer
- Another register can be started by the update event of a timer
- Another register can be selected by the enable of a timer
- Two timers can be synchronized by an external trigger

14.4.15 Interrupt and DMA Request

The timer can generate an interrupt when an event occurs during operation

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Comparison event
- Braking signal input event

Some internal interrupt events can generate DMA requests, and special interfaces can enable or disable DMA requests.

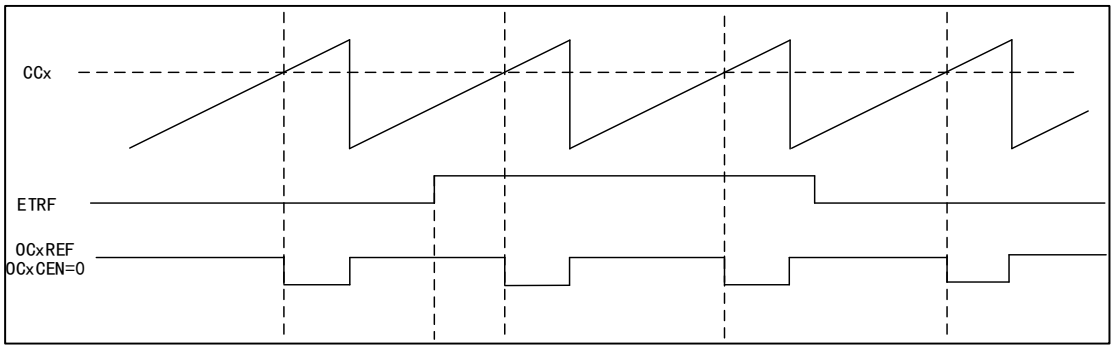
14.4.16 Clear OCxREF Signal when External Events Occur

This function is used for output comparison and PWM mode.

In one channel, the high level of ETRF input port will reduce the signal of OCxREF to low level, and the OCxCEN bit in capture/comparison register TMRx_CCMx is set to 1, and OCxREF signal will remain low until the next update event.

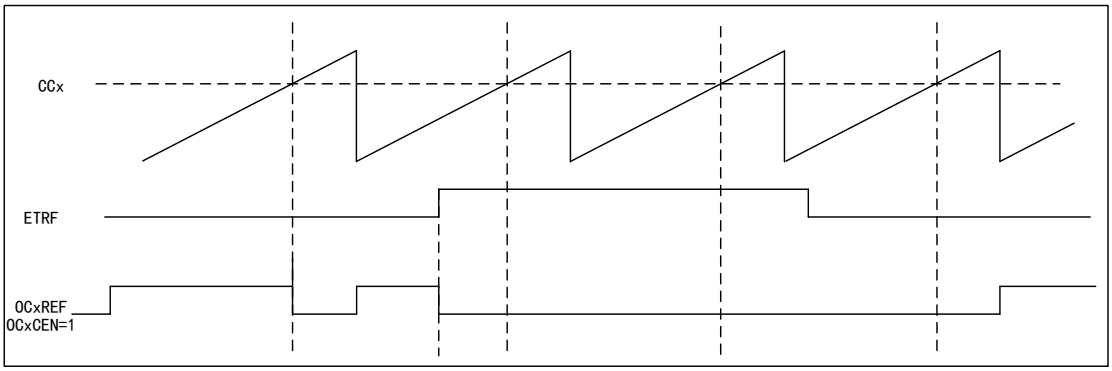
Set TMRx to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=0, and the output OCxREF signal is shown in the figure below.

Figure 40 OCxREF Timing Diagram



Set TMRx to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=1, and the output OCxREF signal is shown in the figure below.

Figure 41 OCxREF Timing Diagram



14.5 Register Address Mapping

In the following table, all registers of the advanced timer are mapped to a 16-bit addressable (address) space.

Table 44 Advanced Timer Register Address Mapping

Register name	Description	Offset address
TMRx_CTRL1	Control register 1	0x00
TMRx_CTRL2	Control register 2	0x04
TMRx_SMCTRL	Slave mode control register	0x08
TMRx_DIEN	DMA/Interrupt enable register	0x0C
TMRx_STS	State register	0x10
TMRx_CEG	Control event generation register	0x14
TMRx_CCM1	Capture/Comparison mode register 1	0x18
TMRx_CCM2	Capture/Comparison mode register 2	0x1C
TMRx_CCEN	Capture/Comparison enable register	0x20
TMRx_CNT	Counter register	0x24
TMRx_PSC	Prescaler register	0x28
TMRx_AUTORLD	Auto reload register	0x2C

Register name	Description	Offset address
TMRx_REPCNT	Repeat count register	0x30
TMRx_CC1	Channel 1 capture/comparison register	0x34
TMRx_CC2	Channel 2 capture/comparison register	0x38
TMRx_CC3	Channel 3 capure/comparison register	0x3C
TMRx_CC4	Channel 4 capture/comparison register	0x40
TMRx_BDT	Braking and dead zone register	0x44
TMRx_DCTRL	DMA control register	0x48
TMRx_DMADDR	DMA address register of continuous mode	0x4C

14.6 Register Functional Description

14.6.1 Control register 1 (TMRx_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit; Update generated by slave mode controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns or underruns Set UEG bit; Update generated by slave mode controller. 1: The counter overruns or underruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed. 0: Disable 1: Enable

Field	Name	R/W	Description
4	CNTDIR	R/W	Counter Direction This bit is read-only when the counter is configured as Center-aligned mode or encoder mode. 0: Count up 1: Count down
6:5	CAMSEL	R/W	Center Aligned Mode Select In the Center-aligned mode, the counter counts up and down alternately; otherwise, it will only count up or down. Different Center-aligned modes affect the timing of setting the output comparison interrupt flag bit of the output channel to 1; when the counter is disabled (CNTEN=0), select the Center-aligned mode. 00: Edge alignment mode 01: Center-aligned mode 1 (the output comparison interrupt flag bit of output channel is set to 1 when counting down) 10: Center-aligned mode 2 (the output comparison interrupt flag bit of output channel is set to 1 when counting up) 11: Center-aligned mode 3 (the output comparison interrupt flag bit of output channel is set to 1 when counting up/down)
7	ARPEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
9:8	CLKDIV	R/W	Clock Division For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit. 00：$t_{DTS}=t_{CK\_INT}$ 01：$t_{DTS}=2\times t_{CK\_INT}$ 10：$t_{DTS}=4\times t_{CK\_INT}$ 11: Reserved
15:10	Reserved		

14.6.2 Control register 2 (TMRx_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
0	CCPEN	R/W	Capture/Compare Preloaded Enable This bit affects the change of CCxEN, CCxNEN and OCxMOD values. When preloading is disabled, the program modification will immediately affect the timer setting; When preloading is enabled, it is only updated after COMG is set, so as to affect the setting of timer; this bit only works on channels with complementary output. 0: Disable 1: Enable
1	Reserved		

Field	Name	R/W	Description
2	CCUSEL	R/W	Capture/compare Control Update Select) only when the capture/comparison preload is enabled (CCPEN=1), and it works only for complementary output channel. 0: It can only be updated by setting COMG bit 1: It can be updated by setting COMG bit or rising edge on TRGI
3	CCDSEL	R/W	Capture/compare DMA Select 0: Send DMA request of CCx when CCx event occurs 1: Send DMA request of CCx when an update event occurs
6:4	MMSEL	R/W	Master Mode Signal Select The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO 011: Comparison pulses; when the master mode timer captures/compares successfully (CCxIFLG=1), a pulse signal is output for TRGO 100: Comparison mode 1; OC1REF is used to trigger TRGO 101: Comparison mode 2; OC2REF is used to trigger TRGO 110: Comparison mode 3; OC3REF is used to trigger TRGO 111: Comparison mode 4; OC4REF is used to trigger TRGO
7	TI1SEL	R/W	Timer Input 1 Selection 0: TMRx_CH1 pin is connected to TI1 input 1: TMRx_CH1, TMRx_CH2 and TMRx_CH3 pins are connected to TI1 input after exclusive
8	OC1OIS	R/W	OC1 Output Idle State Configure Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is realized. 0：OC1=0 1：OC1=1 Note: When LOCKCFG bit in TMRx_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.
9	OC1NOIS	R/W	OC1N Output Idle State Configure Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is realized. 0：OC1N=0 1：OC1N=1 Note: When LOCKCFG bit in TMRx_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.
10	OC2OIS	R/W	Configure OC2 output idle state. Refer to OC1OIS bit
11	OC2NOIS	R/W	Configure OC2N output idle state. Refer to OC1NOIS bit
12	OC3OIS	R/W	Configure OC3 output idle state. Refer to OC1OIS bit
13	OC3NOIS	R/W	Configure OC3N output idle state. Refer to OC1NOIS bit
14	OC4OIS	R/W	Configure OC4 output idle state. Refer to OC1OIS bit

Field	Name	R/W	Description
15	Reserved		

14.6.3 Slave mode control register (TMRx_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

Field	Name	R/W	Description
2:0	SMFSEL	R/W	Slave Mode Function Select 000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock. 001: Encoder mode 1; according to the level of TI1FP1, the counter counts at the edge of TI2FP2. 010: Encoder mode 2; according to the level of TI2FP2, the counter counts at the edge of TI1FP1. 011: Encoder mode 3; according to the input level of another signal, the counter counts at the edge of TI1FP1 and TI2FP2. 100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register. 101: Gated mode; the slave mode timer starts the counter to work after receiving the TRGI high level signal; it stops the counter when receiving TRGI low level; when receiving TRGI high level signal again, the timer will continue to work; the counter is not reset during the whole period. 110: Trigger mode, the slave mode timer starts the counter to work after receiving the rising edge signal of TRGI. 111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.
3	Reserved		
6:4	TRGSEL	R/W	Trigger Input Signal Select In order to avoid false edge detection when changing the bit value, it must be changed when SMFSEL=0. 000: Internal trigger ITR0 001: Internal trigger ITR1 010: Internal trigger ITR2 011: Internal trigger ITR3 100: Channel 1 input edge detector TIF_ED 101: Channel 1 post-filtering timer input TI1FP1 110: Channel 2 post-filtering timer input TI2FP2 111: External trigger input (ETRF)
7	MSMEN	R/W	Master/slave Mode Enable 0: Invalid 1: Enable the master/slave mode
11:8	ETFCFG	R/W	External Trigger Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8

Field	Name	R/W	Description
			0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8 1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, and a jump is generated by every N events.
13:12	ETPCFG	R/W	External Trigger Prescaler Configure The ETR (external trigger input) signal becomes ETRP after frequency division. The signal frequency of ETRP is at most 1/4 of TMRxCLK frequency; when ETR frequency is too high, the ETRP frequency must be reduced through frequency division. 00: The prescaler is disabled; 01: ETR signal 2 divided frequency 10: ETR signal 4 divided frequency 11: ETR signal 8 divided frequency
14	ECEN	R/W	External Clock Enable Mode2 0: Disable 1: Enable Setting ECEN bit has the same function as selecting external clock mode 1 to connect TRGI to ETRF; slave mode (reset, gating, trigger) can be used at the same time with external clock mode 2, but TRGI cannot be connected to ETRF in such case; when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of external clock is ETRF.
15	ETPOL	R/W	External Trigger Polarity Configure This bit decides whether the external trigger ETR is reversed. 0: The external trigger ETR is not reversed, and the high level or rising edge is valid 1: The external trigger ETR is reversed, and the low level or falling edge is valid

Table 45 TMRx Internal Trigger Connection

Slave timer	ITR1 （TS=000）	ITR1 （TS=001）	ITR2 （TS=010）	ITR3 （TS=011）
TMR1	TMR5	TMR2	TMR3	TMR4

14.6.4 DMA/Interrupt enable register (TMRx_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update interrupt Enable 0: Disable 1: Enable

Field	Name	R/W	Description
1	CC1IEN	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
2	CC2IEN	R/W	Capture/Compare Channel2 Interrupt Enable 0: Disable 1: Enable
3	CC3IEN	R/W	Capture/Compare Channel3 Interrupt Enable 0: Disable 1: Enable
4	CC4IEN	R/W	Capture/Compare Channel4 Interrupt Enable 0: Disable 1: Enable
5	COMIEN	R/W	COM Interrupt Enable 0: Disable 1: Enable
6	TRGIEN	R/W	Trigger interrupt Enable 0: Disable 1: Enable
7	BRKIEN	R/W	Break interrupt Enable 0: Disable 1: Enable
8	UDIEN	R/W	Update DMA Request Enable 0: Disable 1: Enable
9	CC1DEN	R/W	Capture/Compare Channel1 DMA Request Enable 0: Disable 1: Enable
10	CC2DEN	R/W	Capture/Compare Channel2 DMA Request Enable 0: Disable 1: Enable
11	CC3DEN	R/W	Capture/Compare Channel3 DMA Request Enable 0: Disable 1: Enable
12	CC4DEN	R/W	Capture/Compare Channel4 DMA Request Enable 0: Disable 1: Enable
13	COMDEN	R/W	COM DMA Request Enable 0: Disable 1: Enable
14	TRGDEN	R/W	Trigger DMA Request Enable 0: Disable 1: Enable
15	Reserved		

14.6.5 State register (TMRx_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMRx_CTRL1 register, and when the value of the repeat counter overruns/underruns, an update event will be generated; (2) URSSEL=0 and UD=0 on TMRx_CTRL1 register, configure UEG=1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software; (3) URSSEL=0 and UD=0 on TMRx_CTRL1 register, generate update event when the counter is initialized by trigger event.
1	CC1IFLG	RC_W0	Capture/Compare Channel1 Interrupt Flag When the capture/comparison channel 1 is configured as output: 0: No matching occurred 1: The value of TMRx_CNT matches the value of TMRx_CC1 When the capture/comparison channel 1 is configured as input: 0: Input capture did not occur 1: Input capture occurred When capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMRx_CC1 register.
2	CC2IFLG	RC_W0	Captuer/Compare Channel2 Interrupt Flag Refer to STS_CC1IFLG
3	CC3IFLG	RC_W0	Capture/Compare Channel3 Interrupt Flag Refer to STS_CC1IFLG
4	CC4IFLG	RC_W0	Captuer/Compare Channel4 Interrupt Flag Refer to STS_CC1IFLG
5	COMIFLG	RC_W0	COM Event Interrupt Generate Flag 0: COM event does not occur 1: COM interrupt waits for response After COM event is generated, this bit is set to 1 by hardware and cleared by software.
6	TRGIFLG	RC_W0	Trigger Event Interrupt Generate Flag 0: Trigger event interrupt did not occur 1: Trigger event interrupt occurred After Trigger event is generated, this bit is set to 1 by hardware and cleared by software.
7	BRKIFLG	RC_W0	Brake Event Interrupt Generate Flag 0: Brake event does not occur 1: Brake event occurs

Field	Name	R/W	Description
			When brake input is valid, this bit is set to 1 by hardware; when brake input is invalid, this bit can be cleared by software.
8	Reserved		
9	CC1RCFLG	RC_W0	Capture/compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs The value of the counter is captured to TMRx_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture.
10	CC2RCFLG	RC_W0	Capture/compare Channel2 Repetition Capture Flag Refer to STS_CC1RCFLG
11	CC3RCFLG	RC_W0	Capture/compare Channel3 Repetition Capture Flag Refer to STS_CC1RCFLG
12	CC4RCFLG	RC_W0	Capture/compare Channel4 Repetition Capture Flag Refer to STS_CC1RCFLG
15:13	Reserved		

14.6.6 Control event generation register (TMRx_CEG)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in Center-aligned mode or count-up mode, the counter will be cleared.
1	CC1EG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Comparison event is generated This bit is set to 1 by software and cleared automatically by hardware. If Channel 1 is in output mode, When CC1IFLG=1, if CC1IEN and CC1DEN bits are set, the corresponding interrupt and DMA request will be generated. If Channel 1 is in input mode The value of the capture counter is stored in TMRx_CC1 register; configure CC1IFLG=1, and if CC1IEN and CC1DEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1.
2	CC2EG	W	Capture/Compare Channel2 Event Generation Refer to CC1EG description
3	CC3EG	W	Capture/Compare Channel3 Event Generation Refer to CC1EG description
4	CC4EG	W	Capture/Compare Channel4 Event Generation

Field	Name	R/W	Description
			Refer to CC1EG description
5	COMG	W	Capture/Compare Control Update Event Generate 0: Invalid 1: Capture/Comparison update event is generated This bit is set to 1 by software and cleared automatically by hardware. Note: COMG bit is valid only in complementary output channel.
6	TEG	W	Trigger Event Generate 0: Invalid 1: Trigger event is generated This bit is set to 1 by software and cleared automatically by hardware.
7	BEG	W	Brake Event Generate 0: Invalid 1: Brake event is generated This bit is set to 1 by software and cleared automatically by hardware.
15:8	Reserved		

14.6.7 Capature/Comparison mode register 1 (TMRx_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (comparison mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCX in the register describes the function of the channel in the output mode, and the ICx in the register describes the function of the channel in the input mode.

Output comparison mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Selection This bit defines the input/output direction and the selected input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC1EN=0).
2	OC1FEN	R/W	Output Compare Channel1 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/comparison output to the trigger input event.
3	OC1PEN	R/W	Output Compare Channel1 Preload Enable 0: Preloading function is disabled; write the value of TMRx_CC1 register through the program and it will work immediately. 1: Preloading function is enabled; write the value of TMRx_CC1 register through the program and it will work after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode

Field	Name	R/W	Description
			(SPMEN=1); otherwise, the following output comparison result is uncertain.
6:4	OC1MOD	R/W	Output Compare Channel1 Mode Configure 000: Freeze The output comparison has no effect on OC1REF 001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture comparison register, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture comparison register, OC1REF will be forced to be at low level 011: Output flaps when matching. When the value of the counter matches the value of the capture comparison register, flap the level of OC1REF 100: The output is forced to be ow Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output comparison value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output comparison value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the comparison result changes or when the output comparison mode changes from freeze mode to PWM mode.
7	OC1CEN	R/W	Output Compare Channel1 Clear Enable 0: OC1REF is unaffected by ETRF input. 1: When high level of ETRF input is detected, OC1REF=0
9:8	CC2SEL	R/W	Capture/Compare Channel2 Select This bit defines the input/output direction and the selected input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC2EN=0).
10	OC2FEN	R/W	Output Compare Channel2 Preload Enable
11	OC2PEN	R/W	Output Compare Channel2 Buffer Enable
14:12	OC2MOD	R/W	Output Compare Channel1 Mode
15	OC2CEN	R/W	Output Compare Channel2 Clear Enable

Input capture mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC1EN=0).

Field	Name	R/W	Description
3:2	IC1PSC	R/W	Input Capture Channel 1 Perscaler Configure 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8 PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC1F	R/W	Input Capture Channel 1 Filter Configuration 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8 0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8 1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
9:8	CC2SEL	R/W	Capture/Compare Channel 2 Select 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI1 10: CC2 channel is input, and IC2 is mapped on TI2 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC2EN=0).
11:10	IC2PSC	R/W	Input Capture Channel 2 Perscaler Configuration
15:12	IC2F	R/W	Input Capture Channel 2 Filter Configuration

14.6.8 Capture/Comparison mode register 2 (TMRx_CCM2)

Offset address: 0x1C
Reset value: 0x0000
Refer to the description of the above CCM1 register.

Output comparison mode:

Field	Name	R/W	Description
1:0	CC3SEL	R/W	Capture/Compare Channel 1 Selection This bit defines the input/output direction and the selected input pin. 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4

Field	Name	R/W	Description
			11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC3EN=0).
2	OC3FEN	R/W	Output Compare Channel3 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/comparison output to the trigger input event.
3	OC3PEN	R/W	Output Compare Channel3 Preload Enable
6:4	OC3MOD	R/W	Output Compare Channel3 Mode Configure
7	OC3CEN	R/W	Output Compare Channel3 Clear Enable 0: OC3REF is unaffected by ETRF input. 1: When high level of ETRF input is detected, OC1REF=0
9:8	CC4SEL	R/W	Capture/Compare Channel 4 Selection This bit defines the input/output direction and the selected input pin. 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI4 10: CC4 channel is input, and IC4 is mapped on TI3 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC4EN=0).
10	OC4FEN	R/W	Output Compare Channel4 Preload Enable
11	OC4PEN	R/W	Output Compare Channel4 Buffer Enable
14:12	OC4MOD	R/W	Output Compare Channel4 Mode Configure
15	OC4CEN	R/W	Output Compare Channel4 Clear Enable

Input capture mode:

Field	Name	R/W	Description
1:0	CC3SEL	R/W	Capture/Compare Channel 3 Select 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4 11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC3EN=0).
3:2	IC3PSC	R/W	Input Capture Channel 3 Perscaler Configuration 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8 PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC3F	R/W	Input Capture Channel 3 Filter Configuration

Field	Name	R/W	Description
9:8	CC4SEL	R/W	Capture/Compare Channel 4 Select 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI4 10: CC4 channel is input, and IC4 is mapped on TI3 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC4EN=0).
11:10	IC4PSC	R/W	Input Capture Channel 4 Perscaler Configuration
15:12	IC4F	R/W	Input Capture Channel 4 Filter Configuration

14.6.9 Capture/Comparison enable register (TMRx_CCEN)

Offset address: 0x20

Reset value: 0x0000

Field	Name	R/W	Description
0	CC1EN	R/W	Capture/Compare Channel1 Output Enable When the capture/comparison channel 1 is configured as output: 0: Output is disabled 1: Output is enabled When the capture/comparison channel 1 is configured as input: This bit determines whether the value CNT of the counter can be captured and enter TMRx_CC1 register 0: Capture is disabled 1: Capture is enabled
1	CC1POL	R/W	Capture/Compare Channel1 Output Polarity Configure When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid When CC1 channel is configured as input: 0: Phase not reversed: select IC1 signal as th trigger or capture signal 1: Phase revered, select reverse signal of IC1 as the trigger or capture signal Note: When the protection level is 2 or 3, this bit cannot be modified
2	CC1NEN	R/W	Capture/Compare Channel1 Complementary Output Enable 0: Disable 1: Enable
3	CC1NPOL	R/W	Capture/Compare Channel1 Complementary Output Polarity 0: OC1N high level is valid 1: OC1N low level is valid Note: When the protection level is 2 or 3, this bit cannot be modified
4	CC2EN	R/W	Capture/Compare Channel2 Output Enable Refer to CCEN_CC1EN
5	CC2POL	R/W	Capture/Compare Channel2 Output Polarity Configure Refer to CCEN_CC1POL
6	CC2NEN	R/W	Capture/Compare Channel1 Complementary Output Enable Refer to CCEN_CC1NEN

Field	Name	R/W	Description
7	CC2NPOL	R/W	Capture/Compare Channel2 Complementary Output Polarity Configure Refer to CCEN_CC1NPOL
8	CC3EN	R/W	Capture/Compare Channel3 Output Enable Refer to CCEN_CC1EN
9	CC3POL	R/W	Capture/Compare Channel3 Output Polarity Configure Refer to CCEN_CC1POL
10	CC3NEN	R/W	Capture/Compare Channel3 Complementary Output Enable Refer to CCEN_CC1NEN
11	CC3NPOL	R/W	Capture/Compare Channel3 Complementary Output Polarity Configure Refer to CCEN_CC1NPOL
12	CC4EN	R/W	Capture/Compare Channel4 Output Enable Refer to CCEN_CC1EN
13	CC4POL	R/W	Capture/Compare Channel4 Output Polarity Refer to CCEN_CC1POL
15:14	Reserved		

14.6.10 Counter register (TMRx_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

14.6.11 Prescaler register (TMRx_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)＝f_{CK_PSC}/(PSC+1)

14.6.12 Auto reload register (TMRx_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

14.6.13 Repeat count register (TMRx_REPCNT)

Offset address: 0x30

Reset value: 0x0000

Field	Name	R/W	Description
7:0	REPCNT	R/W	Repetition Counter Value When the count value of the repeat counter is reduced to 0, an update event will be generated, and the counter will start counting again from the REPCNT value; the new value newly written to this register is valid only when an update event occurs in next cycle.
15:8	Reserved		

14.6.14 Channel 1 capture/comparison register (TMRx_CC1)

Offset address: 0x34

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC1	R/W	Capture/Compare Channel 1 Value When the capture/comparison channel 1 is configured as input mode: CC1 contains the counter value transmitted by the last input capture channel 1 event. When the capture/comparison channel 1 is configured as output mode: CC1 contains the current load capture/comparison register value Compare the value CC1 of the capture and comparison channel 1 with the value CNT of the counter to generate the output signal on OC1. When the output comparison preload is disabled (OC1PEN=0 for TMRx_CCM1 register), the written value will immediately affect the output comparison results; If the output comparison preload is enabled (OC1PEN=1 for TMRx_CCM1 register), the written value will affect the output comparison result when an update event is generated.

14.6.15 Channel 2 capture/comparison register (TMRx_CC2)

Offset address: 0x38

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC2	R/W	Capture/Compare Channel 2 Value Refer to TMRx_CC1

14.6.16 Channel 3 capture/comparison register (TMRx_CC3)

Offset address: 0x3C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC3	R/W	Capture/Compare Channel 3 Value Refer to TMRx_CC1

14.6.17 Channel 4 capture/comparison register (TMRx_CC4)

Offset address: 0x40

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC4	R/W	Capture/Compare Channel 4 Value Refer to TMRx_CC1

14.6.18 Brake and dead zone register (TMRx_BDT)

Offset address: 0x44

Reset value: 0x0000

Note: According to the lock setting, AOEN, BRKPOL, BRKEN, IMOS, RMOS and DTS[7:0] bits all can be write-protected, and it is necessary to configure them when writing to TMRx_BDT register for the first time.

Field	Name	R/W	Description
7:0	DTS	R/W	Dead Time Setup DT is the dead duration, and the relationship between DT and register DTS is as follows: DTS[7:5]=0xx=>DT=DTS[7:0]×T_{DTS}，T_{DTS}=TDTS；

Field	Name	R/W	Description
			DTS[7:5]=10x=>DT=（64+DTS[5:0]）×T_{DTS}，T_{DTS}=2×T_{DTS}； DTS[7:5]=110=>DT=（32+DTS[4:0]）×T_{DTS}，T_{DTS}=8×T_{DTS}； DTS[7:5]=111=>DT=（32+DTS[4:0]）×T_{DTS}，T_{DTS}=16×T_{DTS}； For example: assuming T_{DTS}=125ns (8MHZ), the dead time setting is as follows: If the step time is 125ns, the dead time can be set from 0 to 15875ns; If the step time is 250ns, the dead time can be set from 16us to 31750ns; If the step time is 1us, the dead time can be set from 32us to 63us; If the step time is 2us, the dead time can be set from 64us to 126us. Note: Once LOCK level (LOCKCFG bit in TMRx_BDT register) is set to 1, 2 or 3, these bits cannot be modified.
9:8	LOCKCFG	R/W	Lock Write Protection Mode Configuration 00: Without Lock write protection level; the register can be written directly 01: Lock write protection level 1 It cannot be written to DTS, BRKEN, BRKPOL and AOEN bits of TMRx_BDT, and OCxOIS and OCxNOIS bits of TMRx_CTRL2 register. 02: Lock write protection level 2 It is not allowed to write to all bits with protection level 1 and write to the CCxPOL and OCxNPOL bits in TMRx_CCEN register and the RMOS and IMOS bits in TMRx_BDT register. 11: Lock write protection level 3 It is not allowed to write to all bits with protection level 2, and write to the OCxMOD and OCxPEN bits of TMRx_CCMx register. Note: After system reset, the lock write protect bit can only be written once.
10	IMOS	R/W	Idle Mode Off-state Configure Idle mode means MOEN=0; closed means CcxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=0 and CCxEN changes from 0 to 1. 0: OCx/OCxN output is disabled 1: If CCxEN=1, the invalid level is output during the dead time (the specific level value is affected by the polarity configuration), and the idle level is output after the dead time
11	RMOS	R/W	Run Mode Off-state Configure Run mode means MOEN=1; closed means CCxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=1 and CCxEN changes from 0 to 1. 0: OCx/OCxN output is disabled 1: OCx/OCxN first outptus invalid level (the specific level value is affected by the polarity configuration)
12	BRKEN	R/W	Brake Function Enable 0: Disable 1: Enable Note: When the protection level is 1, this bit cannot be modified.
13	BRKPOL	R/W	Brake Polarity Configure 0: The brake input BRK is valid at low level 1: The brake input BRK is valid at high level

Field	Name	R/W	Description
			Note: When the protection level is 1, this bit cannot be modified. Writing to this bit requires an APB clock delay before it can be used.
14	AOEN	R/W	Automatic Output Enable 0: MOEN can only be set to 1 by software 1: MOEN can be set to 1 by software or be automatically set to 1 in next update event (braking input is ineffective) Note: When the protection level is 1, this bit cannot be modified.
15	MOEN	R/W	PWM Main Output Enable 0: Disable the output of OCx and OCxN or force the output of idle state 1: When CCxEN and CCxNEN bits of the TMRx_CCEN register are set, turn on OCx and OCxN output When the brake input is valid, it is cleared by hardware asynchronously. Note: Setting to 1 by software or setting to 1 automatically depends on AOEN bit of the TMRx_BDT register.

14.6.19 DMA control register (TMRx_DCTRL)

Offset address: 0x48

Reset value: 0x0000

Field	Name	R/W	Description
4:0	DBADDR	R/W	DMA Base Address Setup These bits define the base address of DMA in continuous mode (when reading or writing TMRx_DMADDR register), and DBADDR is defined as the offset from the address of TMRx_CTRL1 register: 00000：TMRx_CTRL1 00001：TMRx_CTRL2 00010：TMRx_SMCTRL …….
7:5	Reserved		
12:8	DBLEN	R/W	DMA Burst Transfer Length Setup These bits define the transfer length and transfer times of DMA in continuous mode. The data transferred can be 16 bits and 8 bits. When reading/writing TMRx_DMADDR register, the timer will conduct a continuous transmission; 00000: Transmission once 00001: Transmission twice 00010: Transmission for three times …… 10001: Transmission for 18 times The transmission address formula is as follows: Transmission address=TMRx_CTRL1 address (slave address) +DBADDR+DMA index; DMA index=DBLEN For example: DBLEN=7, DBADDR=TMR1_CTRL1 (slave address) means the address of the data to be transmitted, while the address +DBADDR+7 of TMRx_CTRL1 means the address of the data to be written/read, Data transmission will occur to: TMRx_CTRL1 address + seven registers starting from DBADDR. The data transmission will change according to different DMA data length:

Field	Name	R/W	Description
			When the transmission data is set to 16 bits, the data will be transmitted to seven registers When the transmission data is set to 8 bits, the data of the first register is the MSB bit of the first data, the data of the second register is the LSB bit of the first data, and the data will still be transmitted to seven registers.
15:13	Reserved		

14.6.20 DMA address register of continuous mode (TMRx_DMADDR)

Offset address: 0x4C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	DMADDR	R/W	DMA Register for Burst Transfer Read or write operation access of TMRx_DMADDR register may lead to access operation of the register in the following address: TMRx_CTRL1 address + (DBADDR+DMA index) ×4 Wherein: "TMRx_CTRL1 address" is the address of control register 1 (TMRx_CTRL1); "DBADDR" is the base address defined in TMRx_DCTRL register; "DMA index" is the offset automatically controlled by DMA, and it depends on DBLEN defined in TMRx_DCTRL register.

15 General-purpose Timer (TMR2/3/4/5)

15.1 Introduction

The general-purpose timer takes the time base unit as the core, and has the functions of input capture and output compare, and can be used to measure the pulse width, frequency and duty cycle, and generate the output waveform. It includes a 16-bit auto reload counter (realize count-up, count-down and center-aligned count).

The timer and timer are independent of each other, and they can achieve synchronization and cascading.

15.2 Main Characteristics

（1） Timebase unit
- Counter: 16-bit counter, count-up, count-down and center-aligned count.
- Prescaler: 16-bit programmable prescaler
- Auto reloading function

（2） Clock source selection
- Internal clock
- External input
- External trigger
- Internal trigger

（3） Input capture function
- Counting function
- PWM input
- Encoder interface mode

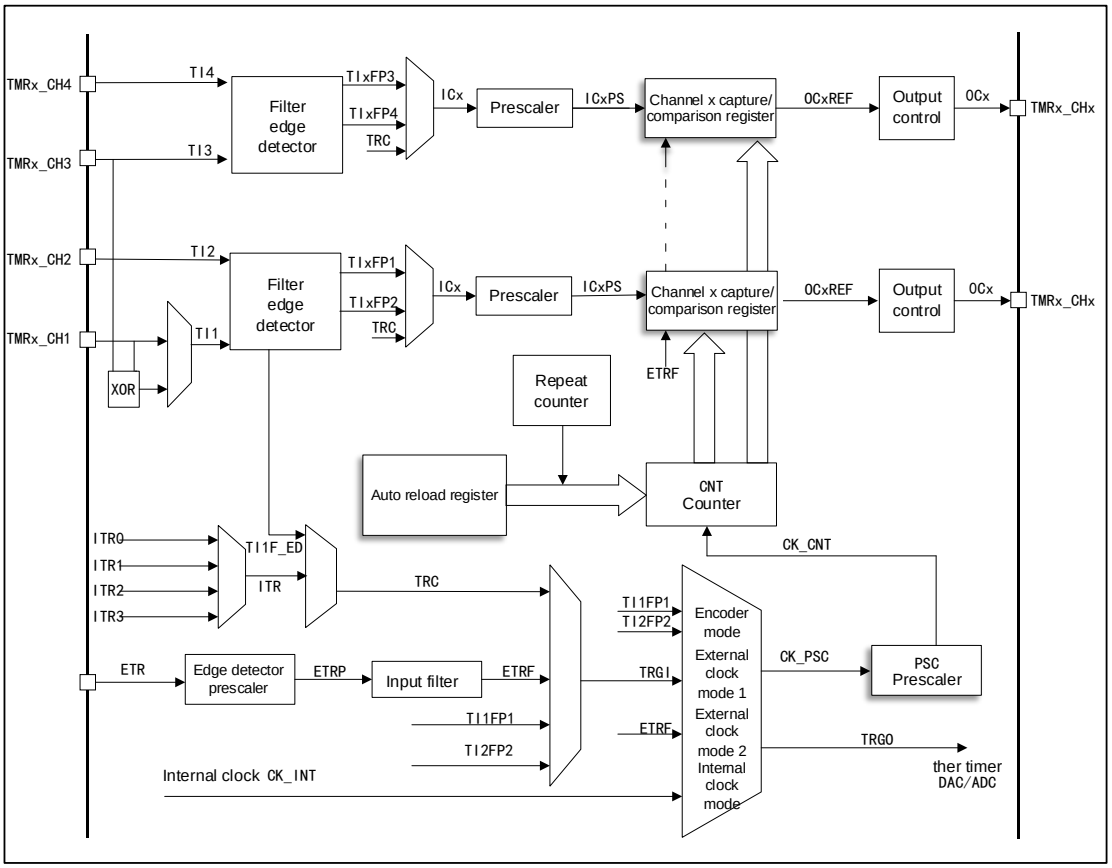
（4） Output compare function
- PWM output mode
- Forced output mode
- Single-pulse mode

（5） Master/Slave mode controller of timer
- Timers can be synchronized and cascaded
- Support multiple slave modes and synchronization signals

（6） Interrupt and DMA request event
- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Input capture
- Output compare

15.3 Structure Block Diagram

Figure 42 General-purpose Timer Structure Block Diagram



15.4 Functional Description

15.4.1 Clock Source Selection

The general-purpose timer has four clock sources

Internal clock

It is TMRx_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

External clock mode 1

The trigger signal generated from the input channel TI1/2/3/4 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of Channel 1 after double-edge detection of the rising edge and the falling edge is logically equal or the future signal is TI1F_ED signal, namely double-edge signal of TIF_ED. Specially the PWM input can only be input by TI1/2.

External clock mode 2

After polarity selection, frequency division and filtering, the signal from external trigger interface (ETR) is connected to slave mode controller through trigger input selector to control the work of counter.

Internal trigger input

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

15.4.2 Timebase Unit

The time base unit in the general-purpose timer contains three registers

- Counter register (CNT) 16 bits
- Auto reload register (AUTORLD) 16 bits
- Prescaler (PSC) 16 bits

Counter CNT

There are three counting modes for the counter in the general-purpose timer

- Count-up mode
- Count-down mode
- Center-aligned mode

Count-up mode

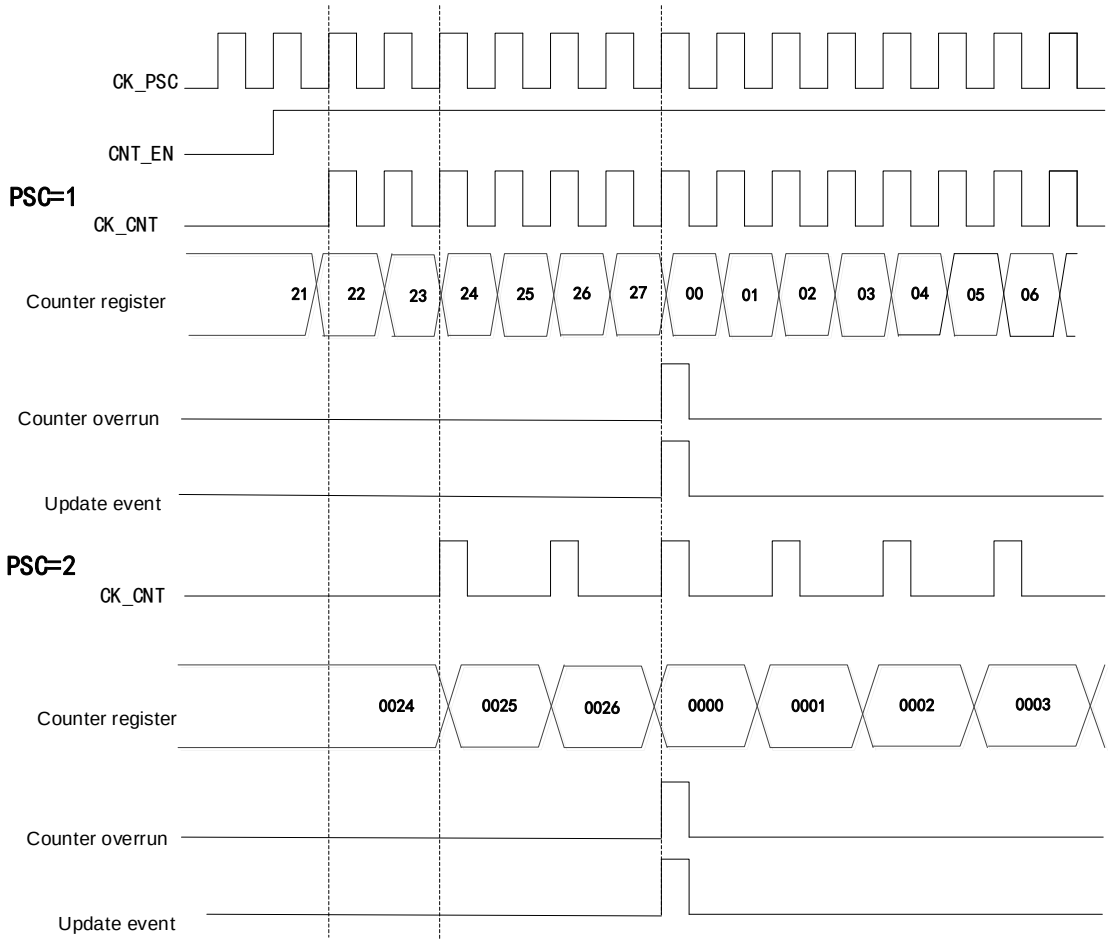
Set to the count-up mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx_CNT) is equal to the value of the auto reload (TMRx_AUTORLD), the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMRx_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by UD bit of configuration control register TMRx_CTRL1.

The figure below is Timing Diagram when Division Factor is 1 or 2 in Count-up Mode

Figure 43 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



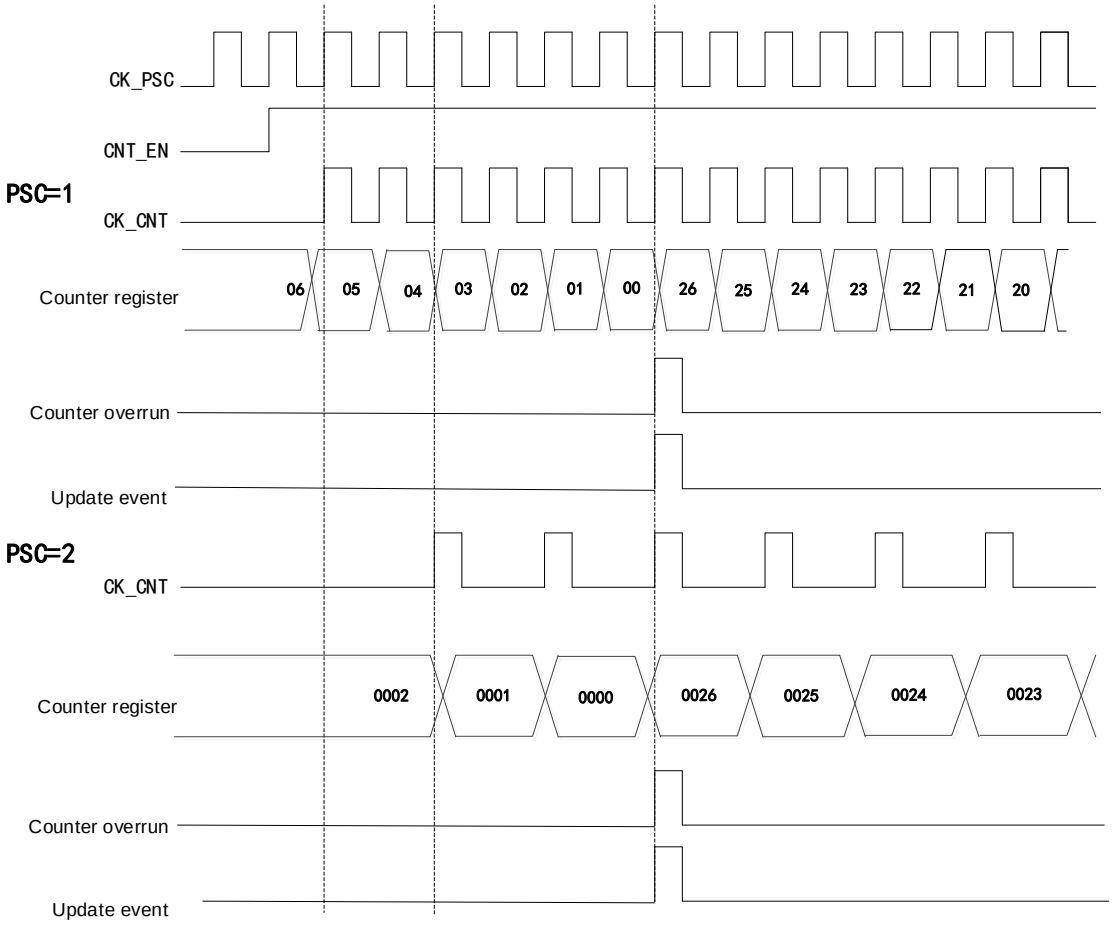
Count-down mode

Set to the count-down mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in count-down mode, the counter will start to count down from the value of the auto reload (TMRx_AUTORLD); every time a pulse is generated, the counter will decrease by 1 and when it becomes 0, the counter will start to count again from (TMRx_AUTORLD), meanwhile, a count-down overrun event will be generated, and the value of the auto reload (TMRx_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by configuring the UD bit of the TMRx_CTRL1 register.

Figure 44 Timing Diagram when Division Factor is 1 or 2 in Count-down Mode

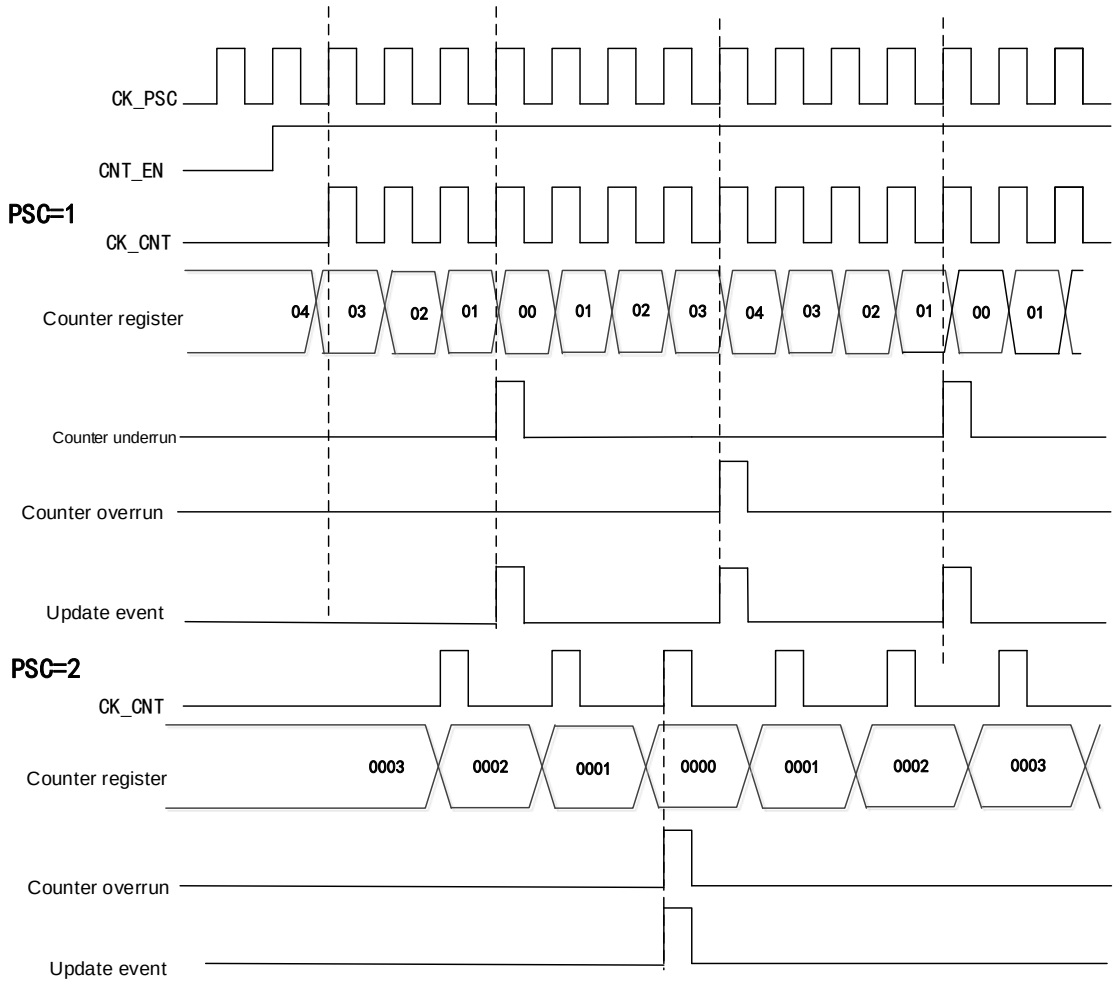


Center-aligned mode

Set to the center-aligned mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in center-aligned mode, the counter counts up from 0 to the value of auto reload (TMRx_AUTORLD), then counts down to 0 from the value of the auto reload (TMRx_AUTORLD), which will repeat; in counting up, when the counter value is (AUTORLD-1), a counter overrun event will be generated; in counting down, when the counter value is 1, a counter underrun event will be generated.

Figure 45 Timing Diagram when Division Factor is 1 or 2 in Center-aligned Mode



Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMRx_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

15.4.3 Input Capture

Input capture channel

The general-purpose timer has four independent capture/comparison channels, each of which is surrounded by a capture/comparison register.

In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the

signal will pass through the prescaler, which is used to set how many events to capture at a time.

Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMRx_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMRx_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

15.4.4 Output Compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is valid, PWM1 and PWM2 modes, which are configured by OCxMOD bit in TMRx_CCMx register and can control the waveform of output signal in output compare mode.

Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/comparison register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMRx_CCMx register and the CCxPOL bit in the output polarity TMRx_CCEN register.

When CCxIFLG=1 in TMRx_STS register, if CCxIEN=1 in TMRx_DIEN register, an interrupt will be generated; if CCDSEL=1 in TMRx_CTRL2 register, DMA request will be generated.

15.4.5 PWM Output Mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the comparison register CCx, and the

cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 are divided into count-up, count-down and edge alignment counting; in PWM mode 1, if the value of the counter CNT is less than the value of the comparison register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM1 mode when CCx=5, AUTORLD=7

Figure 46 PWM1 Count-up Mode Timing Diagram

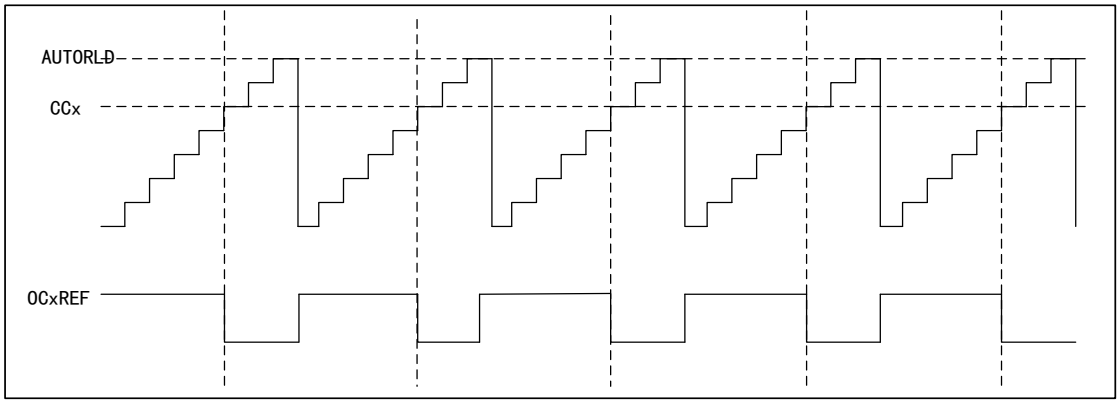


Figure 47 PWM1 Count-down Mode Timing Diagram

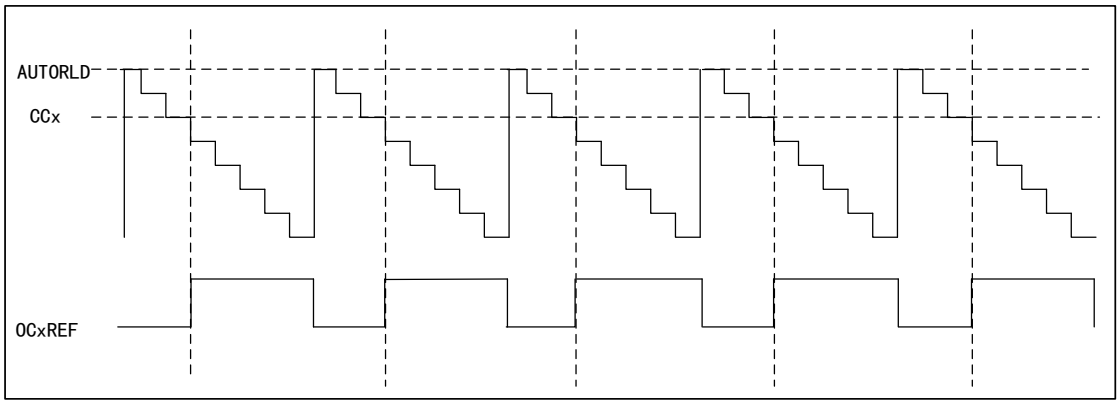
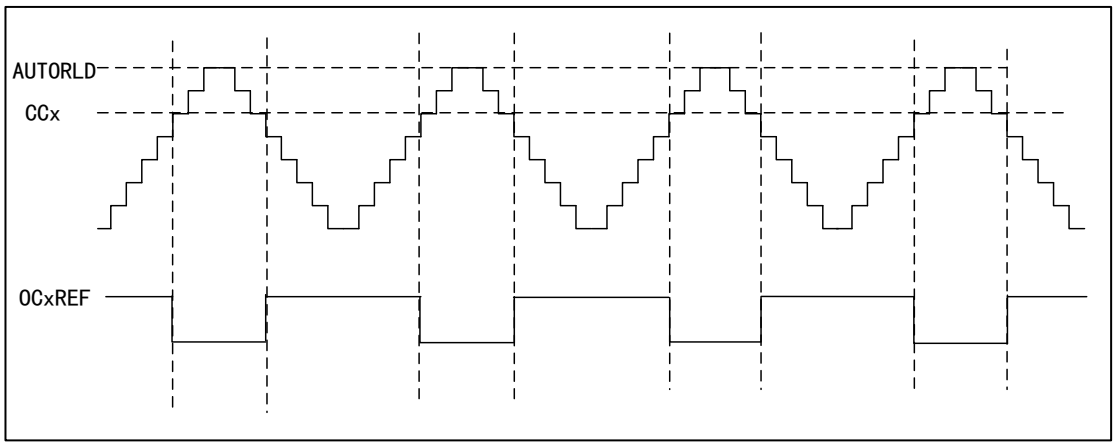


Figure 48 PWM1 Center-aligned Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the comparison register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM2 mode when CCx=5, AUTORLD=7

Figure 49 PWM2 Count-up Mode Timing Diagram

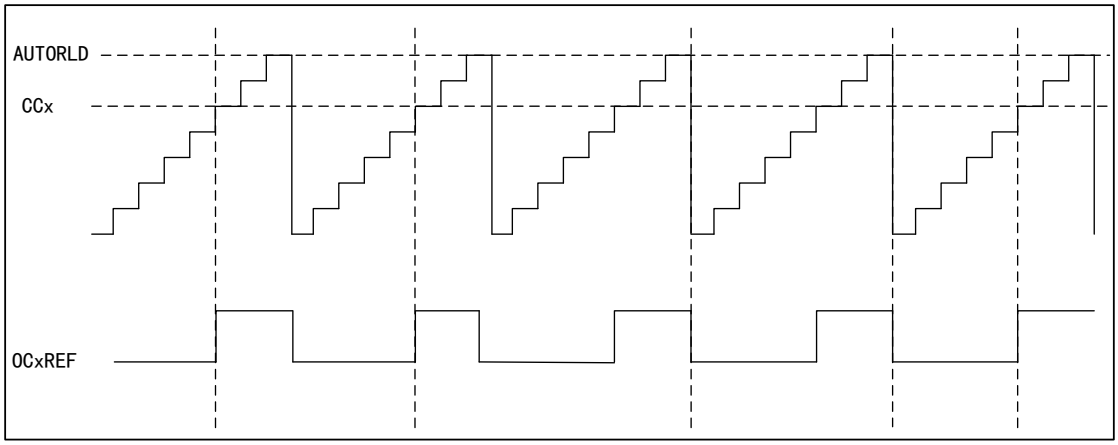


Figure 50 PWM2 Count-down Mode Timing Diagram

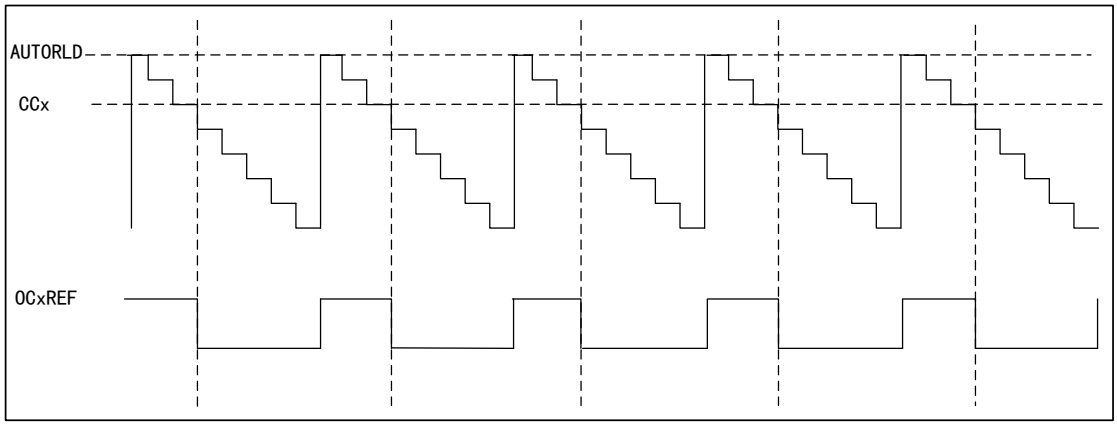
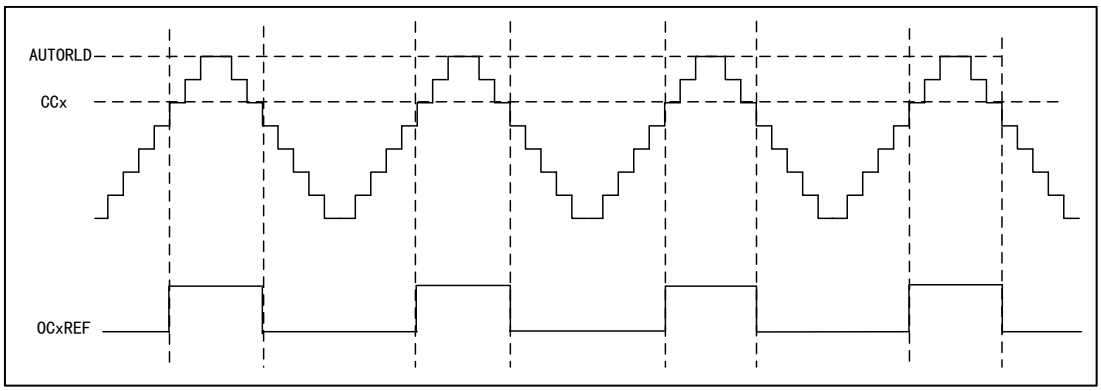


Figure 51 PWM2 Center-aligned Mode Timing Diagram



15.4.6 PWM Input Mode

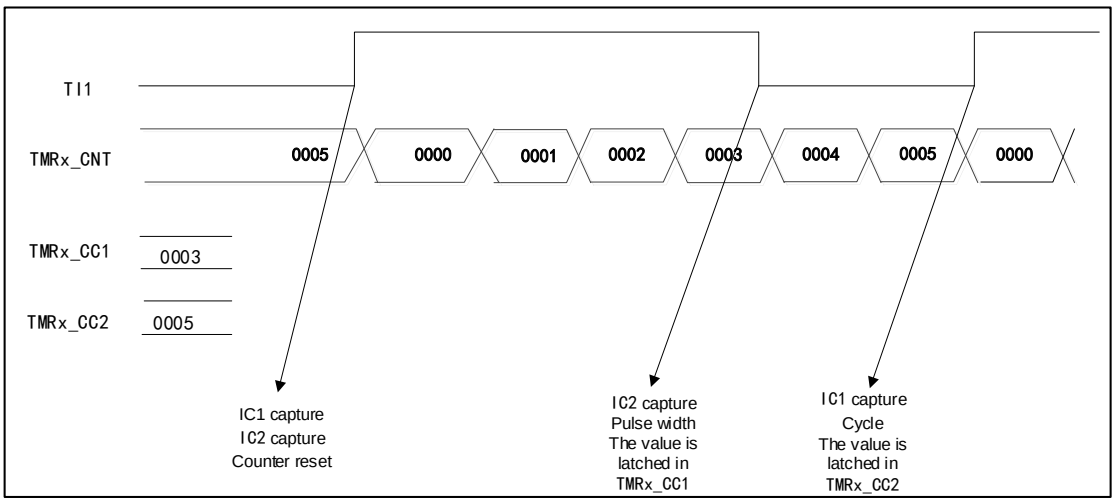
PWM input mode is a particular case of input capture.

In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave mode controller, input can be performed only through the channels TMRx_CH1 and TMRx_CH2, which need to occupy the capure registers of CH1 and CH2.

In the PWM input mode, the PWM signal enters from TMRx_CH1, and the signal will be divided into two channels, one can measure the cycle and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFSEL bit of TMRx_SMCTRL register)

Figure52 PWM Input Mode Timing Diagram



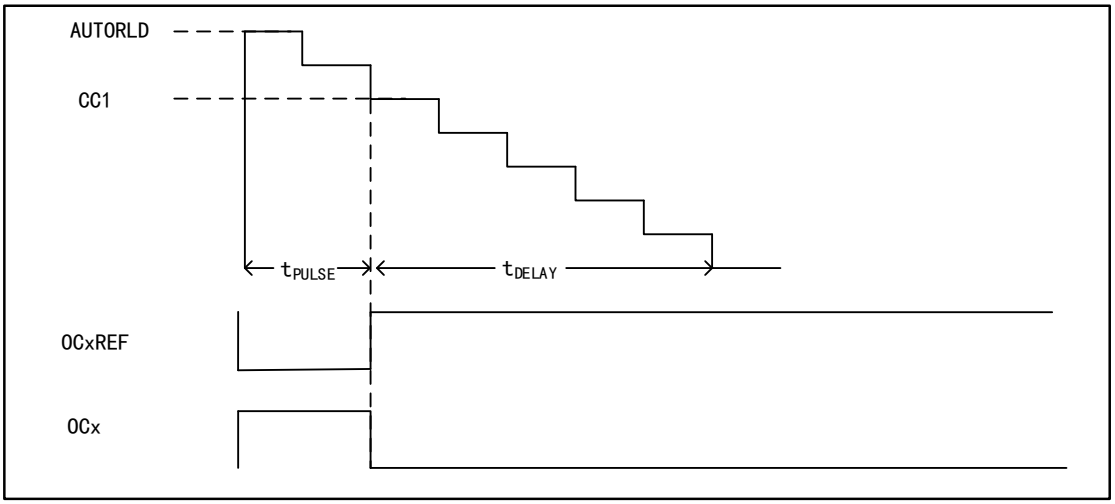
15.4.7 Single-pulse Mode

The single-pulse mode is a special case of timer comparison output, and is also a special case of PWM output mode.

Set SPMEN bit of TMRx_CTRL1 register, and select the single-pulse mode. After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMRx_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 53 Timing Diagram in Single-pulse Mode



15.4.8 Forced Output Mode

In the forced output mode, the comparison result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMRx_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMRx_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt and DMA request will still be generated.

15.4.9 Encoder Interface Mode

The encoder interface mode is equivalent to an external clock with direction selection. In the encoder interface mode, the content of the timer can always indicate the position of the encoder.

The selection methods of encoder interface are as follows:

- By setting SMFSEL bit of TMRx_SMCTRL register, set the counter to count on the edge of TI1 channel /TI2 channel, or count on the edge of TI1 and TI2 at the same time.
- Select the polarity of TI1 and TI2 by setting the CC1POL and CC2POL bits of TMRx_CCEN register.
- Select to filter or not by setting the IC1F and IC2F bits of TMRx_CCM1 register.

The two input TI1 and TI2 can be used as the interface of incremental encoder. The counter is driven by the effective jump of the signals TI1FP1 and TI2FP2 after filtering and edge selection in TI1 and TI2.

The count pulse and direction signal are generated according to the input signals of TI1 and TI2

- The counter will count up/down according to the jumping sequence of the input signal

- Set CNTDIR of control register TMRx_CTRL1 to be read-only (CNTDIR will be re-calculated due to jumping of any input end)

The change mechanism of counter count direction is shown in the figure below

Table 46 Relationship between Count Direction and Encoder

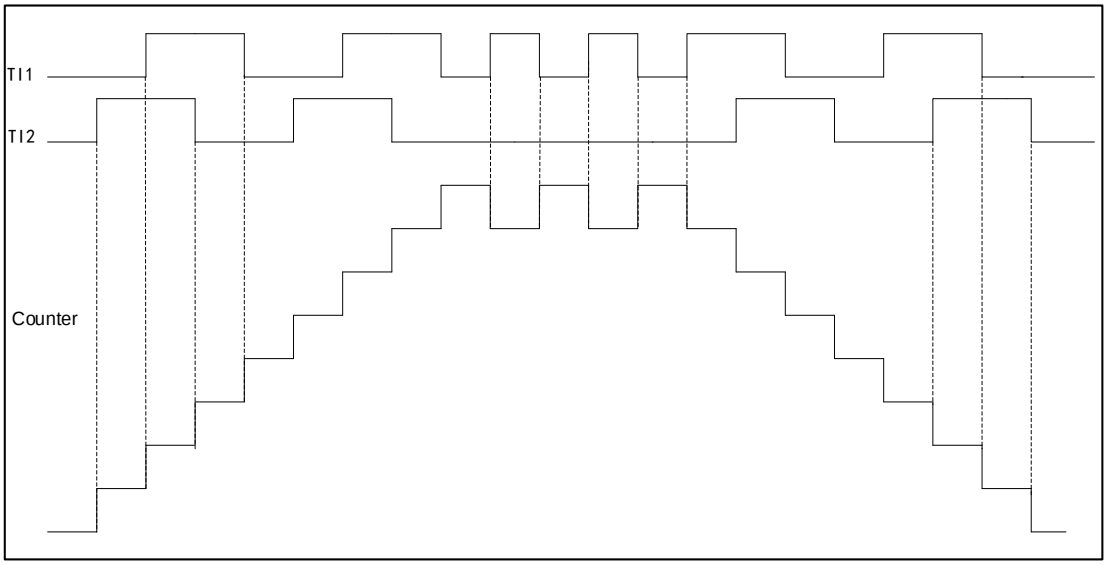
Effective edge		**Count only in TI1**		**Count only in TI2**		**Count in both TI1 and TI2**	
Level of relative signal		High	Low	High	Low	High	Low
TI1FP1	Rising edge	—		Count down	Count up	Count down	Count up
	Falling edge			Count up	Count down	Count up	Count down
TI2FP2	Rising edge	Count up	Count down	—		Count up	Count down
	Falling edge	Count down	Count up			Count down	Count up

The external incremental encoder can be directly connected with MCU, not needing external interface logic, so the comparator is used to convert the differential output of the encoder to digital signal to increase the immunity from noise interference.

Among the following examples,

- TI1FP1 is mapped to TI1
- TI2FP2 is mapped to TI2
- Neither TI1FP1 nor TI2FP2 is reverse phase
- The input signal is valid at the rising edge and falling edge
- Enable the counter

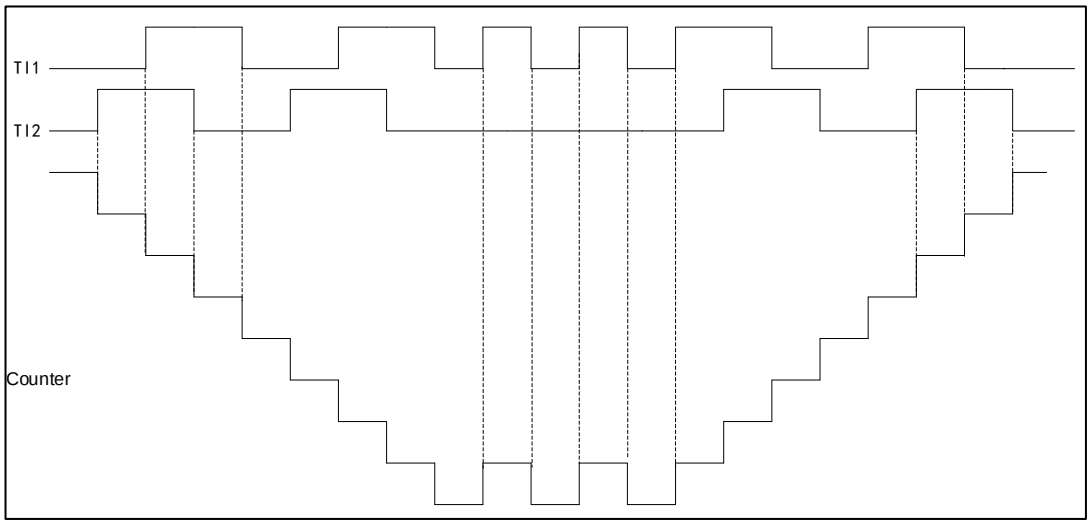
Figure 54 Counter Operation Example in Encoder Mode



For example, when TI1 is at low level, and TI2 is in rising edge state, the

counter will count up.

Figure 55 Example of Encoder Interface Mode of TI1FP1 Reversed Phase



For example, when TI1 is at low level, and the rising edge of TI2 jumps, the counter will count down.

15.4.10 Slave Mode

TMRx timer can synchronize external trigger

- Reset mode
- Gated mode
- Trigger mode

SMFSEL bit in TMRx_SMCTRL register can be set to select the mode

SMFSEL=100 set the reset mode, SMFSEL=101 set the gated mode, SMFSEL=110 set the trigger mode.

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

In the gated mode, the enable of the counter depends on the high level of the selected input. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

In the trigger mode, the enable of the counter depends on the event on the selected input, the counter is started (but is not reset) at the rising edge of the trigger input, and only the start of the counter is controlled.

15.4.11 Timer Interconnection

For details, see 14.4.14 Timer Interconnection

15.4.12 Interrupt and DMA Request

An interrupt occurs when the timer generates an event while it is working

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Comparison event

Some internal interrupt events can generate DMA requests, and special interfaces can enable or disable DMA requests.

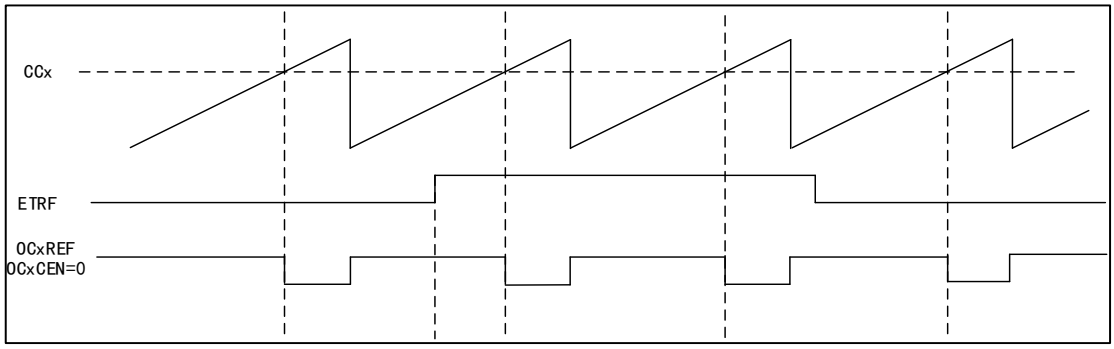
15.4.13 Clear OCxREF Signal when External Events Occur

This function is used for output compare and PWM mode.

In one channel, the high level of ETRF input port will reduce the signal of OCxREF to low level, and the OCxCEN bit in capture/comparison register TMRx_CCMx is set to 1, and OCxREF signal will remain low until the next update event.

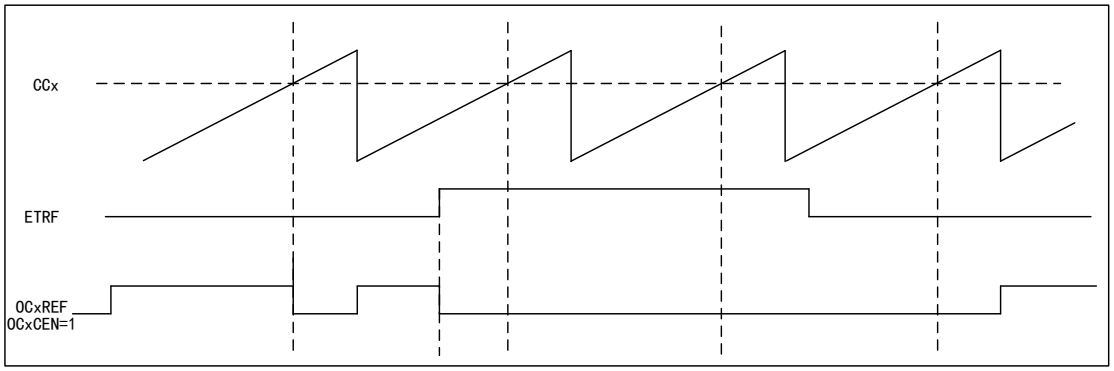
Set TMRx to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=0, and the output OCxREF signal is shown in the figure below.

Figure 56 OCxREF Timing Diagram



Set TMRx to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=1, and the output OCxREF signal is shown in the figure below.

Figure 57 OCxREF Timing Diagram



15.5 Register Address Mapping

In the following table, all registers of the general-purpose timer are mapped to a 16-bit addressable (address) space.

Table 47 General-purpose Timer Register Address Mapping

Register name	Description	Offset address
TMRx_CTRL1	Control register 1	0x00
TMRx_CTRL2	Control register 2	0x04
TMRx_SMCTRL	Slave mode control register	0x08
TMRx_DIEN	DMA/Interrupt enable register	0x0C
TMRx_STS	State register	0x10
TMRx_CEG	Control event generation register	0x14
TMRx_CCM1	Capture/Comparison mode register 1	0x18
TMRx_CCM2	Capture/Comparison mode register 2	0x1C
TMRx_CCEN	Capture/Comparison enable register	0x20
TMRx_CNT	Counter register	0x24
TMRx_PSC	Prescaler register	0x28
TMRx_AUTORLD	Auto reload register	0x2C
TMRx_CC1	Channel 1 capture/comparison register	0x34
TMRx_CC2	Channel 2 capture/comparison register	0x38
TMRx_CC3	Channel 3 capure/comparison register	0x3C
TMRx_CC4	Channel 4 capture/comparison register	0x40
TMRx_DCTRL	DMA control register	0x48
TMRx_DMADDR	DMA address register of continuous mode	0x4C

15.6 Register Functional Description

15.6.1 Control register 1 (TMRx_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work;

Field	Name	R/W	Description
			when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit; Update generated by slave mode controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns or underruns Set UEG bit Update generated by slave mode controller 1: The counter overruns or underruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed. 0: Disable 1: Enable
4	CNTDIR	R/W	Counter Direction When the counter is configured in central alignment mode or encoder mode, the bit is read-only. 0: Count up 1: Count down
6:5	CAMSEL	R/W	Center Aligned Mode Select In the center-aligned mode, the counter counts up and down alternately; otherwise, it will only count up or down. Different center-aligned modes affect the timing of setting the output compare interrupt flag bit of the output channel to 1; when the counter is disabled (CNTEN=0), select the center-aligned mode. 00: Edge alignment mode 01: Center-aligned mode 1 (the output compare interrupt flag bit of output channel is set to 1 when counting down) 10: Center-aligned mode 2 (the output compare interrupt flag bit of output channel is set to 1 when counting up) 11: Center-aligned mode 3 (the output compare interrupt flag bit of output channel is set to 1 when counting up/down)
7	ARPEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable

Field	Name	R/W	Description
			1: Enable
9:8	CLKDIV	R/W	Clock Division For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit. 00: $t_{DTS}=t_{CK\_INT}$ 01: $t_{DTS}=2\times t_{CK\_INT}$ 10: $t_{DTS}=4\times t_{CK\_INT}$ 11: Reserved
15:10	Reserved		

15.6.2 Control register 2 (TMRx_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
2:0	Reserved		
3	CCDSEL	R/W	Capture/compare DMA Select 0: Send DMA request of CCx when CCx event occurs 1: Send DMA request of CCx when an update event occurs
6:4	MMSEL	R/W	Master Mode Signal Select The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO 011: Comparison pulses; when the master mode timer captures/compares successfully (CCxIFLG=1), a pulse signal is output for TRGO 100: Comparison mode 1; OC1REF is used to trigger TRGO 101: Comparison mode 2; OC2REF is used to trigger TRGO 110: Comparison mode 3; OC3REF is used to trigger TRGO 111: Comparison mode 4; OC4REF is used to trigger TRGO
7	TI1SEL	R/W	Timer Input 1 Selection 0: TMRx_CH1 pin is connected to TI1 input 1: TMRx_CH1, TMRx_CH2 and TMRx_CH3 pins are connected to TI1 input after exclusive
15:8	Reserved		

15.6.3 Slave mode control register (TMRx_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

Field	Name	R/W	Description
2:0	SMFSEL	R/W	Slave Mode Function Select 000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock. 001: Encoder mode 1; according to the level of TI1FP1, the counter counts at the edge of TI2FP2. 010: Encoder mode 2; according to the level of TI2FP2, the counter counts at the edge of TI1FP1. 011: Encoder mode 3; according to the input level of another signal, the counter counts at the edge of TI1FP1 and TI2FP2. 100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register. 101: Gated mode; the slave mode timer starts the counter to work after receiving the TRGI high level signal; it stops the counter when receiving TRGI low level; when receiving TRGI high level signal again, the timer will continue to work; the counter is not reset during the whole period. 110: Trigger mode, the slave mode timer starts the counter to work after receiving the rising edge signal of TRGI. 111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.
3	Reserved		
6:4	TRGSEL	R/W	Trigger Input Signal Select In order to avoid false edge detection when changing the bit value, it must be changed when SMFSEL=0. 000: Internal trigger ITR0 001: Internal trigger ITR1 010: Internal trigger ITR2 011: Internal trigger ITR3 100: Channel 1 input edge detector TIF_ED 101: Channel 1 post-filtering timer input TI1FP1 110: Channel 2 post-filtering timer input TI2FP2 111: External trigger input (ETRF)
7	MSMEN	R/W	Master/slave Mode Enable 0: Invalid 1: Enable the master/slave mode
11:8	ETFCFG	R/W	External Trigger Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001: DIV=1, N=2 0010: DIV=1, N=4 0011: DIV=1, N=8 0100: DIV=2, N=6 0101: DIV=2, N=8 0110: DIV=4, N=6 0111: DIV=4, N=8 1000: DIV=8, N=6 1001: DIV=8, N=8

Field	Name	R/W	Description
			1010: DIV=16, N=5 1011: DIV=16, N=6 1100: DIV=16, N=8 1101: DIV=32, N=5 1110: DIV=32, N=6 1111: DIV=32, N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, and a jump is generated by every N events.
13:12	ETPCFG	R/W	External Trigger Prescaler Configure The ETR (external trigger input) signal becomes ETRP after frequency division. The signal frequency of ETRP is at most 1/4 of TMRxCLK frequency; when ETR frequency is too high, the ETRP frequency must be reduced through frequency division. 00: The prescaler is disabled; 01: ETR signal 2 divided frequency 10: ETR signal 4 divided frequency 11: ETR signal 8 divided frequency
14	ECEN	R/W	External Clock Mode2 Enable 0: Disable 1: Enable Setting ECEN bit has the same function as selecting external clock mode 1 to connect TRG1 to ETRF; slave mode (reset, gating, trigger) can be used at the same time with external clock mode 2, but TRGI cannot be connected to ETRF in such case; when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of external clock is ETRF.
15	ETPOL	R/W	External Trigger Polarity Configure This bit decides whether the external trigger ETR is reversed. 0: The external trigger ETR is not reversed, and the high level or rising edge is valid 1: The external trigger ETR is reversed, and the low level or falling edge is valid

Table 48 TMRx Internal Trigger Connection

Slave timer	ITR0 (TS=000)	ITR1 (TS=001)	ITR2 (TS=010)	ITR3 (TS=011)
TMR2	TMR1	-	TMR3	TMR4
TMR3	TMR1	TMR2	TMR5	TMR4
TMR4	TMR1	TMR2	TMR3	-
TMR5	TMR2	TMR3	TMR4	-

15.6.4 DMA/Interrupt enable register (TMRx_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update Interrupt Enable 0: Disable

Field	Name	R/W	Description
			1: Enable
1	CC1IEN	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
2	CC2IEN	R/W	Capture/Compare Channel2 Interrupt Enable 0: Disable 1: Enable
3	CC3IEN	R/W	Capture/Compare Channel3 Interrupt Enable 0: Disable 1: Enable
4	CC4IEN	R/W	Capture/Compare Channel4 Interrupt Enable 0: Disable 1: Enable
5	Reserved		
6	TRGIEN	R/W	Trigger Interrupt Enable 0: Disable 1: Enable
7	Reserved		
8	UDIEN	R/W	Update DMA Request Enable 0: Disable 1: Enable
9	CC1DEN	R/W	Capture/Compare Channel1 DMA Request Enable 0: Disable 1: Enable
10	CC2DEN	R/W	Capture/Compare Channel2 DMA Request Enable 0: Disable 1: Enable
11	CC3DEN	R/W	Capture/Compare Channel3 DMA Request Enable 0: Disable 1: Enable
12	CC4DEN	R/W	Capture/Compare Channel4 DMA Request Enable 0: Disable 1: Enable
13	Reserved		
14	TRGDEN	R/W	Trigger DMA Request Enable 0: Disable 1: Enable
15	Reserved		

15.6.5 State register (TMRx_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMRx_CTRL1 register, and when the value of the repeat counter overruns/underruns, an update event will be generated; (2) URSEL=0 and UD=0 on TMRx_CTRL1 register, configure UG = 1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software; (3) URSEL=0 and UD=0 on TMRx_CTRL1 register, generate update event when the counter is initialized by trigger event.
1	CC1IFLG	RC_W0	Capture/Compare Channel1 Interrupt Flag When the capture/comparison channel 1 is configured as output: 0: No matching occurred 1: The value of TMRx_CNT matches the value of TMRx_CC1 When the capture/comparison channel 1 is configured as input: 0: Input capture did not occur 1: Input capture occurred When capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMRx_CC1 register.
2	CC2IFLG	RC_W0	Capture/Compare Channel2 new Interrupt Flag Refer to STS_CC1IFLG
3	CC3IFLG	RC_W0	Capture/Compare Channel3 Interrupt Flag Refer to STS_CC1IFLG
4	CC4IFLG	RC_W0	Captuer/Compare Channel4 Interrupt Flag Refer to STS_CC1IFLG
5	Reserved		
6	TRGIFLG	RC_W0	Trigger Event Interrupt Generate Flag 0: Trigger event interrupt did not occur 1: Trigger event interrupt occurred When trigger event occurs, this bit is set to 1 by hardware and cleared by software.
8:7	Reserved		
9	CC1RCFLG	RC_W0	Capture/compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs The value of the counter is captured to TMRx_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture.
10	CC2RCFLG	RC_W0	Capture/compare Channel2 Repetition Capture Flag Refer to STS_CC1RCFLG

Field	Name	R/W	Description
11	CC3RCFLG	RC_W0	Capture/compare Channel3 Repetition Capture Flag Refer to STS_CC1RCFLG
12	CC4RCFLG	RC_W0	Capture/compare Channel4 Repetition Capture Flag Refer to STS_CC1RCFLG
15:13	Reserved		

15.6.6 Control event generation register (TMRx_CEG)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared.
1	CC1EG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Comparison event is generated This bit is set to 1 by software and cleared automatically by hardware. If Channel 1 is in output mode When CC1IFLG=1, if CC1IEN and CC1DEN bits are set, the corresponding interrupt and DMA request will be generated. If Channel 1 is in input mode The value of the capture counter is stored in TMRx_CC1 register; configure CC1IFLG=1, and if CC1IEN and CC1DEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1.
2	CC2EG	W	Capture/Compare Channel2 Event Generation Refer to CC1EG description
3	CC3EG	W	Capture/Compare Channel3 Event Generation Refer to CC1EG description
4	CC4EG	W	Capture/Compare Channel4 Event Generation Refer to CC1EG description
5	Reserved		
6	TEG	W	Trigger Event Generate 0: Invalid 1: Trigger event is generated This bit is set to 1 by software and cleared automatically by hardware.
15:7	Reserved		

15.6.7 Capature/Comparison mode register 1 (TMRx_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (comparison mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCX in the register describes the function of the channel in the output mode, and the ICx in the register describes the function of the channel in the input mode.

Output compare mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Selection This bit defines the input/output direction and the selected input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC1EN=0).
2	OC1FEN	R/W	Output Compare Channel1 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/comparison output to the trigger input event.
3	OC1PEN	R/W	Output Compare Channel1 Preload Enable 0: Preloading function is disabled; write the value of TMRx_CC1 register through the program and it will work immediately. 1: Preloading function is enabled; write the value of TMRx_CC1 register through the program and it will work after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.

Field	Name	R/W	Description
6:4	OC1MOD	R/W	Output Compare Channel1 Mode Configure 000: Freeze. The output compare has no effect on OC1REF 001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compare register, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture/compare register, OC1REF will be forced to be at low level 011: Output flaps when matching. When the value of the counter matches the value of the capture/compare register, flap the level of OC1REF 100: The output is forced to be ow Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output compare value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output compare value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the comparison result changes or when the output compare mode changes from freeze mode to PWM mode.
7	OC1CEN	R/W	Output Compare Channel1 Clear Enable 0: OC1REF is unaffected by ETRF input. 1: When high level of ETRF input is detected, OC1REF=0
9:8	CC2SEL	R/W	Capture/Compare Channel2 Select This bit defines the input/output direction and the selected input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC2EN=0).
10	OC2FEN	R/W	Output Compare Channel2 Preload Enable
11	OC2PEN	R/W	Output Compare Channel2 Buffer Enable
14:12	OC2MOD	R/W	Output Compare Channel2 Mode
15	OC2CEN	R/W	Output Compare Channel2 Clear Enable

Input capture mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC1EN=0).

Field	Name	R/W	Description
3:2	IC1PSC	R/W	Input Capture Channel 1 Perscaler Configure 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8 PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC1F	R/W	Input Capture Channel 1 Filter Configuration 0000: Filter disabled, sampling by f_{DTS} 0001: DIV=1, N=2 0010: DIV=1, N=4 0011: DIV=1, N=8 0100: DIV=2, N=6 0101: DIV=2, N=8 0110: DIV=4, N=6 0111: DIV=4, N=8 1000: DIV=8, N=6 1001: DIV=8, N=8 1010: DIV=16, N=5 1011: DIV=16, N=6 1100: DIV=16, N=8 1101: DIV=32, N=5 1110: DIV=32, N=6 1111: DIV=32, N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
9:8	CC2SEL	R/W	Capture/Compare Channel 2 Select 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI1 10: CC2 channel is input, and IC2 is mapped on TI2 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC2EN=0).
11:10	IC2PSC	R/W	Input Capture Channel 2 Perscaler Configuration
15:12	IC2F	R/W	Input Capture Channel 2 Filter Configuration

15.6.8 Capture/Compare mode register 2 (TMRx_CCM2)

Offset address: 0x1C

Reset value: 0x0000

Refer to the description of the above CCM1 register.

Output compare mode:

Field	Name	R/W	Description
1:0	CC3SEL	R/W	Capture/Compare Channel 3 Selection This bit defines the input/output direction and the selected input pin. 00: CC3 channel is output

Field	Name	R/W	Description
			01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4 11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC3EN=0).
2	OC3FEN	R/W	Output Compare Channel3 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/compare output to the trigger input event.
3	OC3PEN	R/W	Output Compare Channel3 Preload Enable
6:4	OC3MOD	R/W	Output Compare Channel3 Mode Configure
7	OC3CEN	R/W	Output Compare Channel3 Clear Enable 0: OC3REF is unaffected by ETRF input. 1: When high level of ETRF input is detected, OC1REF=0
9:8	CC4SEL	R/W	Capture/Compare Channel 4 Selection This bit defines the input/output direction and the selected input pin. 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI4 10: CC4 channel is input, and IC4 is mapped on TI3 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC4EN=0).
10	OC4FEN	R/W	Output Compare Channel4 Preload Enable
11	OC4PEN	R/W	Output Compare Channel4 Buffer Enable
14:12	OC4MOD	R/W	Output Compare Channel4 Mode Configure
15	OC4CEN	R/W	Output Compare Channel4 Clear Enable

Input capture mode:

Field	Name	R/W	Description
1:0	CC3SEL	R/W	Capture/Compare Channel 3 Select 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4 11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC3EN=0).
3:2	IC3PSC	R/W	Input Capture Channel 3 Perscaler Configuration 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8

Field	Name	R/W	Description
			PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC3F	R/W	Input Capture Channel 3 Filter Configuration
9:8	CC4SEL	R/W	Capture/Compare Channel 4 Select 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI4 10: CC4 channel is input, and IC4 is mapped on TI3 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC4EN=0).
11:10	IC4PSC	R/W	Input Capture Channel 4 Perscaler Configuration
15:12	IC4F	R/W	Input Capture Channel 4 Filter Configuration

15.6.9 Enable capture/compare channel register (TMRx_CCEN)

Offset address: 0x20

Reset value: 0x0000

Field	Name	R/W	Description
0	CC1EN	R/W	Capture/Compare Channel1 Output Enable When the capture/compare channel 1 is configured as output: 0: Output is disabled 1: Output is enabled When the capture/compare channel 1 is configured as input: This bit determines whether the value CNT of the counter can be captured and enter TMRx_CC1 register 0: Capture is disabled 1: Capture is enabled
1	CC1POL	R/W	Capture/Compare Channel1 Output Polarity Configure When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid When CC1 channel is configured as input: 0: Phase not reversed: capture at the rising edge of IC1; phase not reversed when IC1 is used as external trigger. 1: Phase reversed, capature at the falling edge of ICC1; phase reversed when IC1 is used as external trigger. Note: When the protection level is 2 or 3, this bit cannot be modified
3:2	Reserved		
4	CC2EN	R/W	Capture/Compare Channel2 Output Enable Refer to CCEN_CC1EN
5	CC2POL	R/W	Capture/Compare Channel2 Output Polarity Configure Refer to CCEN_CC1POL
7:6	Reserved		
8	CC3EN	R/W	Capture/Compare Channel3 Output Enable Refer to CCEN_CC1EN

Field	Name	R/W	Description
9	CC3POL	R/W	Capture/Compare Channel3 Output Polarity Configure Refer to CCEN_CC1POL
11:10	Reserved		
12	CC4EN	R/W	Capture/Compare Channel4 Output Enable Refer to CCEN_CC1EN
13	CC4POL	R/W	Capture/Compare Channel4 Output Polarity Refer to CCEN_CC1POL
15:14	Reserved		

Table 49Output Control Bit of Standard OCx Channel

CCxEN bit	OCx output state
0	Output is disabled (OCx=0, OCx_EN=0)
1	OCx=OCxREF+polarity, OCx_EN=1

Note: The state of external I/O pin connected to the standard OCx channel depends on the state of the OCx channel and the GPIO and AFIO registers.

15.6.10 Counter register (TMRx_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

15.6.11 Prescaler register (TMRx_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)=f_{CK_PSC}/(PSC+1)

15.6.12 Auto reload register (TMRx_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

15.6.13 Channel 1 capture/compare register (TMRx_CC1)

Offset address: 0x34

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC1	R/W	Capture/Compare Channel 1 Value When the capture/compare channel 1 is configured as input mode: CC1 contains the counter value transmitted by the last input capture channel 1 event. When the capture/compare channel 1 is configured as output mode: CC1 contains the current load capture/compare register value Compare the value CC1 of the capture/compare channel 1 with the value CNT of the counter to generate the output signal on OC1. When the output compare preload is disabled (OC1PEN=0 for TMRx_CCM1 register), the written value will immediately affect the output compare results; If the output compare preload is enabled (OC1PEN=1 for TMRx_CCM1 register), the written value will affect the output compare result when an update event is generated.

15.6.14 Channel 2 capture/compare register (TMRx_CC2)

Offset address: 0x38

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC2	R/W	Capture/Compare Channel 2 Value Refer to TMRx_CC1

15.6.15 Channel 3 capture/compare register (TMRx_CC3)

Offset address: 0x3C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC3	R/W	Capture/Compare Channel 3 Value Refer to TMRx_CC1

15.6.16 Channel 4 capture/compare register (TMRx_CC4)

Offset address: 0x40

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC4	R/W	Capture/Compare Channel 4 Value Refer to TMRx_CC1

15.6.17 DMA control software (TMRx_DCTRL)

Offset address: 0x48

Reset value: 0x0000

Field	Name	R/W	Description
4:0	DBADDR	R/W	DMA Base Address Setup These bits define the base address of DMA in continuous mode (when reading or writing TMRx_DMADDR register), and DBADDR is defined as the offset from the address of TMRx_CTRL1 register: 00000: TMRx_CTRL1 00001: TMRx_CTRL2 00010: TMRx_SMCTRL …….
7:5	Reserved		
12:8	DBLEN	R/W	DMA Burst Transfer Length Setup These bits define the transfer length and transfer times of DMA in continuous mode. The data transferred can be 16 bits and 8 bits. When reading/writing TMRx_DMADDR register, the timer will conduct a continuous transmission; 00000: Transmission once 00001: Transmission twice 00010: Transmission for three times …… 10001: Transmission for 18 times The transmission address formula is as follows: Transmission address=TMRx_CTRL1 address (slave address) +DBADDR+DMA index; DMA index=DBLEN For example: DBLEN=7, DBADDR=TMR1_CTRL1 (slave address) means the address of the data to be transmitted, while the address of TMRx_CTRL1+DBADDR+7 means the address of the data to be written/read, Data transmission will occur to: TMRx_CTRL1 address + seven registers starting from DBADDR. The data transmission will change according to different DMA data length: When the transmission data is set to 16 bits, the data will be transmitted to seven registers When the transmission data is set to 8 bits, the data of the first register is the MSB bit of the first data, the data of the second register is the LSB bit of the first data, and the data will still be transmitted to seven registers.
15:13	Reserved		

15.6.18 DMA address register of continuous mode (TMRx_DMADDR)

Offset address: 0x4C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	DMADDR	R/W	DMA Register for Burst Transfer Read or write operation access of TMRx_DMADDR register may lead to access operation of the register in the following address: TMRx_CTRL1 address + (DBADDR+DMA index) ×4 Wherein: "TMRx_CTRL1 address" is the address of control register 1 (TMRx_CTRL1); "DBADDR" is the base address defined in TMRx_DCTRL register;

Field	Name	R/W	Description
			"DMA index" is the offset automatically controlled by DMA, and it depends on DBLEN defined in TMRx_DCTRL register.

16 Basic Timer (TMR6/7)

16.1 Introduction

The basic timers TMR6 and TMR7 have an unsigned 16-bit counter, auto reload register, prescaler and trigger controller.

The basic timer provides time reference for general-purpose timer and provides clock for DAC. DMA request can be generated by configuration.

16.2 Main Characteristics

（1） Counter: 16-bit counter, which can only count up

（2） Prescaler: 16-bit programmable prescaler

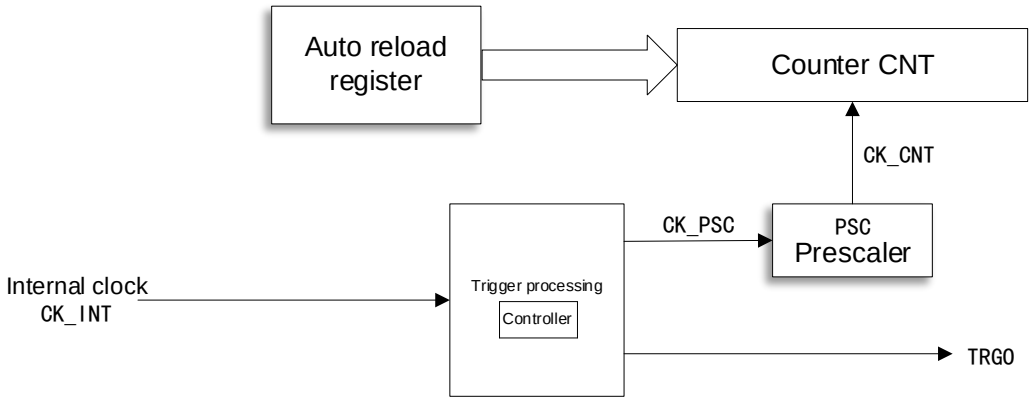
（3） Clock source: There is only internal clock

（4） Single-pulse mode

（5） Provide clock for DAC

16.3 Structure Block Diagram

Figure 58 Basic Timer Structure Block Diagram



16.4 Functional Description

16.4.1 Clock Source Selection

The basic timer is driven by internal clock source TMRx_CLK

Configure the CNTEN bit of TMRx_CTRL1 register to enable the counter; when CNTEN bit is set, the internal clock CK_INT can generate CK_INT to drive the counter through the controller and prescaler.

16.4.2 Timebase Unit

The time base unit in the basic timer contains three registers:

- Counter register (CNT) 16 bits
- Auto reload register (AUTORLD) 16 bits
- Prescaler (PSC) 16 bits

Counter CNT

The basic timer only has one count mode: count-up

Count-up mode

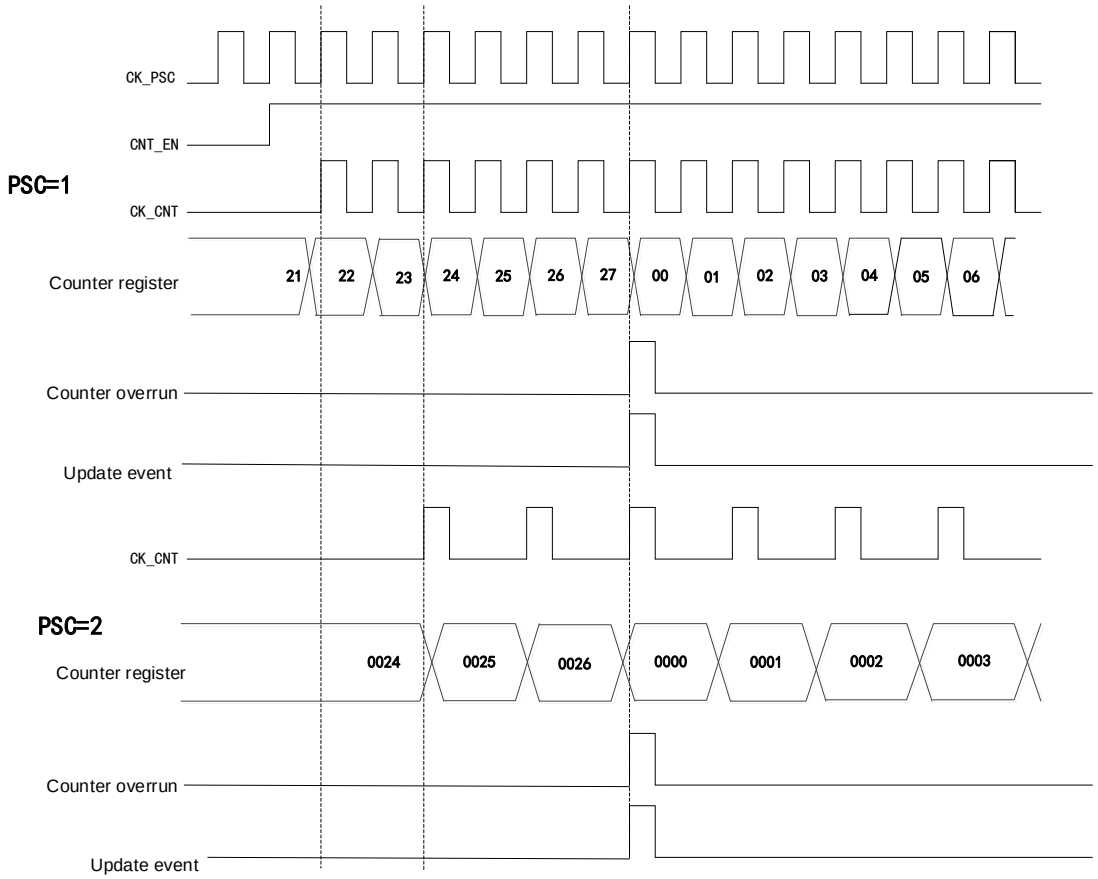
When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx_CNT) is equal to the value of the auto reload (TMRx_AUTORLD), then the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMRx_AUTORLD) is written in advance.

Disable the update event and set UD bit of TMRx_CTRL1 register to 1.

Generate the update interrupt or DMA request and set URSSEL bit in TMRx_CTRL1 register.

When an update event occurs, both the auto reload register and the prescaler register will be updated.

Figure 59 Timer Timing Diagram, the internal clock division factor is 1 or 2



Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMRx_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

16.5 Register Address Mapping

In the following table, all registers of the basic timer are mapped to a 16-bit addressable (address) space.

Table 60 Basic Timer Register Mapping

Register name	Description	Offset address
TMRx_CTRL1	Control register 1	0x00
TMRx_CTRL2	Control register 2	0x04
TMRx_DIEN	DMA/Interrupt enable register	0x0C
TMRx_STS	State register	0x10

Register name	Description	Offset address
TMRx_CEG	Control event generation register	0x14
TMRx_CNT	Counter register	0x24
TMRx_PSC	Prescaler register	0x28
TMRx_AUTORLD	Auto reload register	0x2C

16.6 Register Functional Description

16.6.1 Control register 1 (TMRx_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit; Update generated by slave mode controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns or underruns Set UEG bit Update generated by slave mode controller 1: The counter overruns or underruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed. 0: Disable 1: Enable
6:4	Reserved		

Field	Name	R/W	Description
7	ARPEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
15:8	Reserved		

16.6.2 Control register 2 (TMRx_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
2:0	Reserved		
3	CCDSEL	R/W	Capture/compare DMA Select 0: Send DMA request of CCx when CCx event occurs 1: Send DMA request of CCx when an update event occurs
6:4	MMSEL	R/W	Master Mode Signal Select The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO 011: Compare pulses; when the master mode timer captures/compares successfully (CCxIFLG=1), a pulse signal is output for TRGO 100: Compare mode 1; OC1REF is used to trigger TRGO 101: Compare mode 2; OC2REF is used to trigger TRGO 110: Compare mode 3; OC3REF is used to trigger TRGO 111: Compare mode 4; OC4REF is used to trigger TRGO
15:7	Reserved		

16.6.3 DMA/Interrupt enable register (TMRx_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update Interrupt Enable 0: Disable 1: Enable
7:1	Reserved		
8	UDIEN	R/W	Update DMA Request Enable 0: Disable 1: Enable
15:9	Reserved		

16.6.4 State register (TMRx_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMRx_CTRL1 register, and when the value of the repeat counter overruns/underruns, an update event will be generated; (2) URSEL=0 and UD=0 on TMRx_CTRL1 register, configure UG = 1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software; (3) URSEL=0 and UD=0 on TMRx_CTRL1 register, generate update event when the counter is initialized by trigger event.
15:1	Reserved		

16.6.5 Control event generation register (TMRx_CEG)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared.
15:1	Reserved		

Note: The state of external I/O pin connected to the standard OCx channel depends on the state of the OCx channel and the GPIO and AFIO registers.

16.6.6 Counter register (TMRx_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

16.6.7 Prescaler register (TMRx_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)＝f_{CK_PSC}/(PSC+1)

16.6.8 Auto reload register (TMRx_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

17 Watchdog Timer (WDT)

17.1 Introduction

The watchdog is used to monitor system failures caused by software errors. There are two watchdog devices on the chip: independent watchdog and window watchdog, which improve the security, and make the time more accurate and the use more flexible.

The independent watchdog will reset only when the counter is reduced to 0, and the value of refresh counter will not be reset until it is not reduced to 0.

The window watchdog will reset when the counter decreases to 0x3F. When the count value of the counter is before the window value of the configuration register, the refresh counter will also be reset.

17.2 Independent Watchdog Timer (IWDT)

17.2.1 Introduction

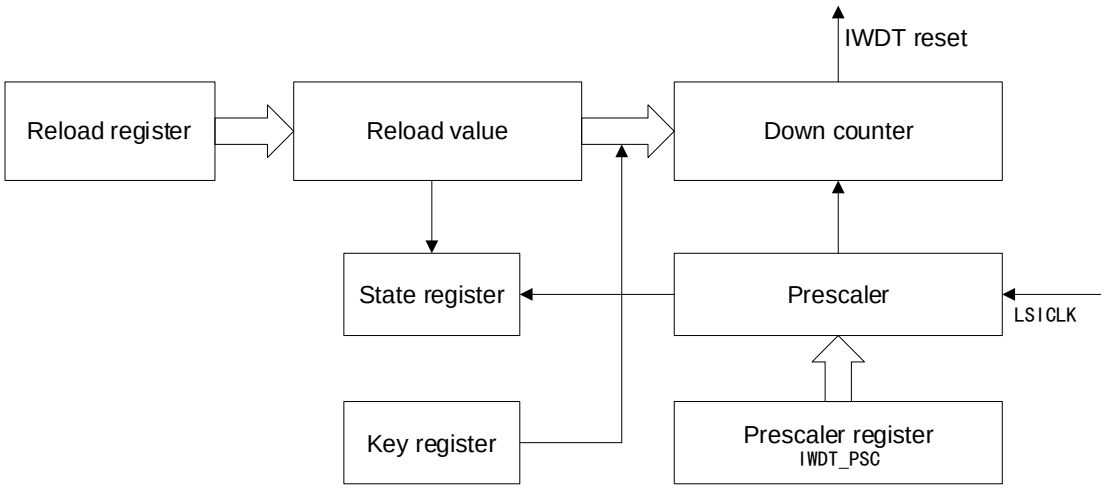
The independent watchdog consists of an 8-bit prescaler IWDT_PSC, 12-bit count-down counter, 12-bit reload register IWDT_CNTRLD, key register IWDT_KEY and state register IWDT_STS.

The independent watchdog has an independent clock source, and even if the master clock fails, it is still valid.

The independent watchdog is applicable to the situations where an independent environment is required but the accuracy requirement is not high.

17.2.2 Structure Block Diagram

Figure 60 Independent Watchdog Structure Block Diagram



Note: The watchdog function is in the V_{DD} power supply area and can work normally in the shutdown or standby mode.

17.2.3 Functional Description

17.2.3.1 Key register

Write 0xCCCC in the key register to enable the independent watchdog, then the counter starts to count down, and when the counter counts to 0x000, a reset will be generated.

Write 0xAAAA in the key register, and the value of the reload register will be reloaded to the counter to prevent the watchdog from resetting.

Write 0X5555 in the key register to rewrite the value of the prescaler register and the reload register.

17.2.3.2 Regiser access protection

The prescaler register and reload register have the function of write protection. If you want to rewrite these two registers, you need to write 0X5555 in the key register. If you write other value in the key register, the protection of the register will be started again.

Write 0xAAAA to the key register and the write protection function will also be enabled.

17.2.3.3 Hardware watchdog

After the "hardware watchdog" function is enabled, and the system is powered on and reset, the watchdog will run automatically. If 0xAAAA is not written to the key register, reset will be generated after the counter finishes counting.

17.2.3.4 Debug mode

The independent watchdog can be configured in debug mode and choose to stop or continue to work. Depend on DBGMCU_CFG register IWDT_STS bit.

17.3 Window Watchdog Timer (WWDT)

17.3.1 Introduction

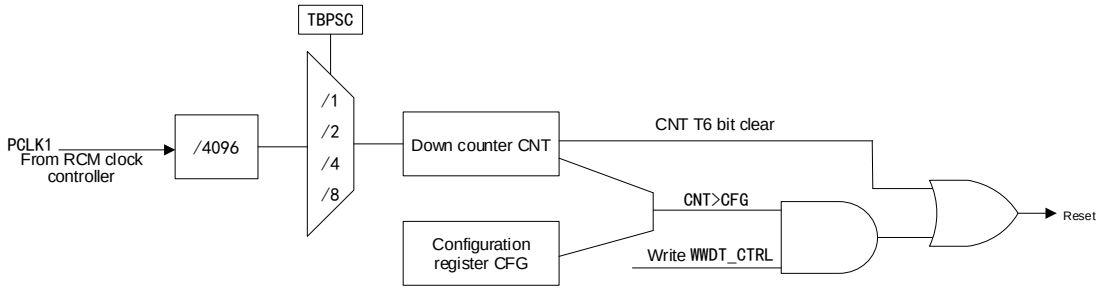
The window watchdog contains a 7-bit free-running down counter, prescaler and control register WWDT_CTRL, configuration register WWDT_CFG and state register WWDT_STS.

The window watchdog clock comes from PCLK1, and the counter clock is obtained from the CK counter clock through frequency division by prescaler (configured by the configuration register).

The window watchdog is applicable when precise timing is needed.

17.3.2 Structure Block Diagram

Figure 61 Window Watchdog Structure Block Diagram



17.3.3 Functional Description

Enable window watchdog timer; the reset conditions are:

- When the counter count is less than 0x40, a reset will be generated.
- The reload counter will be reset before the counter counts to the value of the window register.

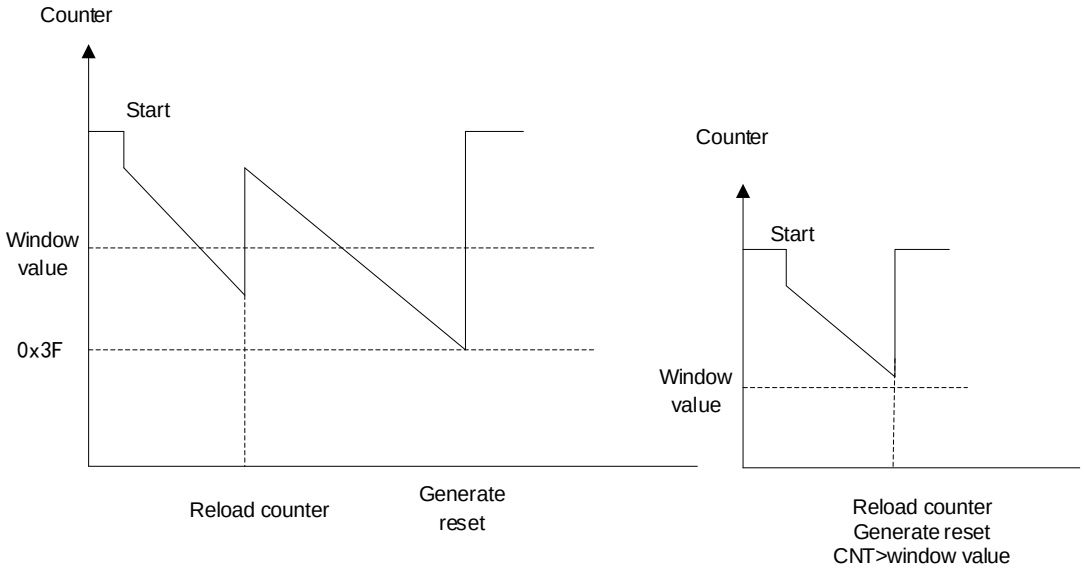
After reset, the watchdog is always closed and the watchdog can be enabled only by setting the WWDTEN bit of WWDT_CTRL control register.

The counter of window watchdog is in free state. When the watchdog is disabled, the counter will continue to count down. The counter must be reloaded between the value of window register and 0x40 to avoid reset.

Setting the EWIEN bit of the configuration register can enable the early wake-up interrupt. When the count reaches 0x40, the interrupt will be generated. Entering the interrupt service program (ISTS) can be used to prevent the window watchdog from resetting. EWIEN interrupt can be cleared by writing 0 in the state register.

The unique window of the window watchdog timer can effectively monitor whether the program is faulty. For example, assuming that the running time of a program segment is T, and the value of the window register is slightly less than (TR-T), if there is no reload register in the window, it means that the program is faulty, and when the counter counts to 0x3F, it will generate reset.

Figure 62 Window Watchdog Timing Diagram



The calculation formula of window watchdog timer timeout is as follows:

$$T_{WWDT}=T_{PCLK1}\times 2^{WTB}\times（T[5:0]+1）$$

Wherein:

- T_{WWDT}: WWDT timeout
- T_{PCLK1}: Clock cycle of APB1 in ms

Minimum/Maximum timeout when PCLK1=48MHZ

WTB	Minimum timeout value	Maximum timeout value
0	84.75μs	5.46ms
1	170.25μs	10.92ms
2	341.25μs	21.84ms
3	682.5μs	43.6875ms

17.4 IWDT Register Address Mapping

Table 50 IWDT Register Mapping

Register name	Description	Offset address
IWDT_KEY	Key register	0x00
IWDT_PSC	Prescaler register	0x04
IWDT_CNTRLD	Counter reload register	0x08
IWDT_STS	State register	0x0C

17.5 IWDT Register Functional Description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

17.5.1 Key register (IWDT_KEY)

Offset address: 0x00

Reset value: 0x0000 0000 (reset in standby mode)

Field	Name	R/W	Description
15:0	KEY	W	Allow Access IWDT Register Key Value Writing 0x5555 means enabled access to IWDT_PSC and IWDT_CNTRLD registers; When the software writes 0xAAAA, it means to execute the reload counter, and a certain interval is required to prevent the watchdog from resetting. Write 0xCCCC and the watchdog will be enabled (the hardware watchdog is unrestricted by this command word); This register is write-only and the read-out vlue is 0x0000.
31:16	Reserved		

17.5.2 Prescaler register (IWDT_PSC)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	PSC	R/W	Prescaler Factor Configure Support write protection function; when writing 0x5555 in the IWDT_KEY register, it is allowed to access the register; in the process of writing this register, only when IWDT_STS register PSCUFLG=0, can the prescaler factor be changed; in the process of reading this register, only when PSCUFLG=0, can the read-out value of PSC register be valid. 000：PSC=4 001：PSC=8 010：PSC=16 011：PSC=32 100: PSC=64 101：PSC=128 110：PSC=256 111：PSC=256
31:3	Reserved		

17.5.3 Counter reload register (IWDT_CNTRLD)

Offset address: 0x08

Reset value: 0x0000 0FFF (reset in standby mode)

Field	Name	R/W	Description
11:0	CNTRLD	R/W	Watchdog Counter Reload Value Setup It supports write protection function and defines the value loaded to the watchdog counter when 0xAAAA is written by IWDT_KEY register; in the process of writing this register, this register can be modified only when CNTUFLG=0. In the process of reading this register, when CNTUFLG=0 in IWDT_STS register, the read value is valid. The watchdog timeout cyclecan be calculated by the reload value and clock prescaled value.
31:12	Reserved		

17.5.4 State register (IWDT_STS)

Offset address: 0x0C

Reset value: 0x0000 0000 (not reset in standby mode)

Field	Name	R/W	Description
0	PSCUFLG	R	Watchdog Prescaler Factor Update Flag When the prescaler factor is updated, it is set to 1 by hardware; after the prescaler factor is updated, the bit is cleared by hardware; the prescaler factor is updated only when the PSCUFLG bit is cleared.
1	CNTUFLG	R	Watchdog Counter Reload Value Update Flag When the counter reload value is updated, it is set to 1 by hardware; after the counter reload value is updated, the bit is cleared by hardware; the counter reload value is updated only when the CNTUFLG bit is cleared.
31:2	Reserved		

17.6 WWDT Register Address Mapping

Table 51 WWDT Register Mapping

Register name	Description	Offset address
WWDT_CTRL	Control register	0x00
WWDT_CFG	Configuration register	0x04
WWDT_STS	State register	0x08

17.7 WWDT Register Functional Description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

17.7.1 Control register (WWDT_CTRL)

Offset address: 0x00

Reset value: 0x0000 007F

Field	Name	R/W	Description
6:0	CNT	R/W	Counter Value Setup This counter is 7 bits, and CNT6 is the most significant bit These bits are used to store the counter value of the watchdog. When the count value decreases from 0x40 to 0x3F, WWDT reset will be generated.
7	WWDTEN	R/S	Window Watchdog Enable This bit is set to 1 by software and can be cleared by hardware only after reset. When WWDTEN=1, WWDT can generate a reset. 0: Disable 1: Enable
31:8	Reserved		

17.7.2 Configuration register (WWDT_CFG)

Offset address: 0x04

Reset value: 0x0000 007F

Field	Name	R/W	Description
6:0	WIN	R/W	Window Value Setup This window value is 7 bits, which is used to compare with the down counter (CNT).
8:7	TBPSC	R/W	Timer Base Prescaler Factor Configure Divide the frequency on the basis of PCLK1/4096 00: No frequency division 01: Two-divided frequency 10: Four-divided frequency 11: Eight-divided frequency
9	EWIEN	R/S	Early Wakeup Interrupt Enable 0: No effect 1: When the counter value reaches 0x40, an interrupt will be generated; this interrupt is cleared by hardware after reset.
31:10	Reserved		

17.7.3 State register (WWDT_STS)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	EWIFLG	RC_W0	Early Wakeup Interrupt Occur Flag 0: Not occur 1: When the counter value reaches 0x40, it is set to 1 by hardware; if the interrupt is not enabled, the bit will also be set to 1; it can be cleared by writing 0 by software.
31:1	Reserved		

18 Real-time Clock (RTC)

18.1 Full Name and Abbreviation Description of Terms

Table 52 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Second	SEC
Alarm	ALR
Overflow	OVR
Prescaler	PSC
Time Basic Clock	TBCLK

18.2 Main Characteristics

Real-time clock (RTC) is a timer that automatically switches to backup power supply after main power failure to maintain the operation.

（1） Timebase unit

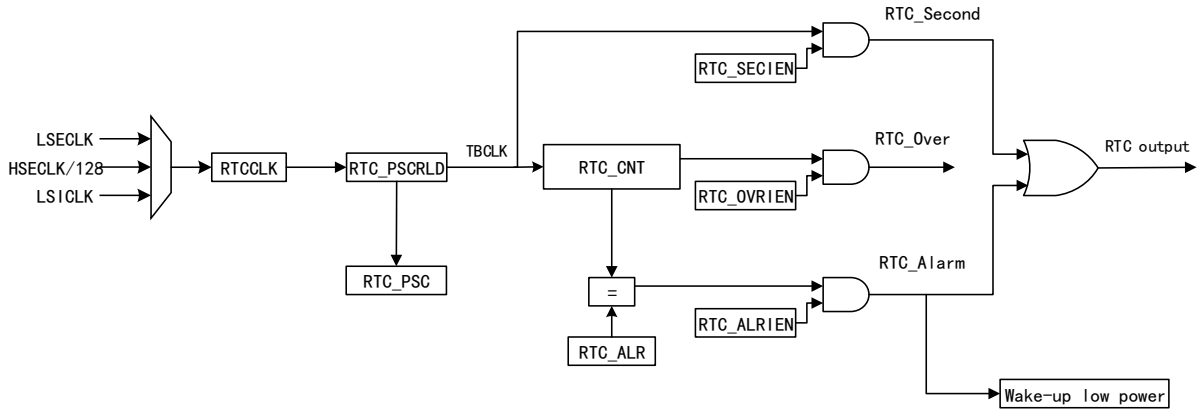
（2） Programmable 32bit counter

（3） Multiple interrupt control

（4） Automatic wakeup of low power

18.3 Structure Block Diagram

Figure 63 RTC Structure Block Diagram



18.4 Functional Description

18.4.1 Timebase Unit

Clock source

RTC has three clock sources RTC_CLK:

- External LSECLK crystal oscillator
- External HSECLK crystal oscillator 128 divided frequency
- Internal LSICLK

Different clock sources are configured through RCM peripheral of clock controller.

Prescaler

The RTC prescaler contains a 20-bit programmable frequency divider, which can be programmed to generate RTC time reference of up to 1 second.

18.4.2 RTC Register Configuration

In order to prevent counting exception caused by accidental write in RTC register, RTC adopts write protection mechanism. Only when the write protection is removed, can the register with write protection function be operated.

When configuring RTC clock, it's required to set BPWEN bit of the power control register (PMU_CTRL) to "1"; configure CFGMFLG bit of RTC_CSTS register to make the RTC enter the configuration mode so that the RTC_PSCRLD, RTC_CNT and RTC_ALR registers can be configured; clear CFGMFLG bit of RTC_CSTS register to exit the configuration mode.

The write operation to any register of RTC can be performed only after the previous write operation is finished (judge by querying RTC_CSTS OCFLG).

18.4.3 Programmable Alarm

As a real-time clock, RTC integrates the alarm function internally, and it runs mainly through alarm register and counter, and configures the alarm time through register RTC_ ALR; after the alarm function is enabled, when the counter value is equal to the alarm value, it will be triggered and the alarm flag will be set. If the alarm interrupt is enabled, the interrupt processing will be triggered, and through the configuration of external line 17 interrupt, RTC alarm can be used to wake up low power consumption.

18.4.4 RTC Output

RTC can output the internal RTC second pulse, alarm signal and calibration clock to the outside through PC13 pin, and select the output pulse by

configuring BAKPR_CLKCAL register.

18.4.5 Interrupt

RTC can generate second interrupt, alarm interrupt and overrun interrupt. When 20-bit prescaler overrun, alarm event and 32-bit counter overrun are generated, the corresponding state flag bit will be pending and the corresponding interrupt can be generated by configuring RTC_CTRL register.

18.5 Register Address Mapping

Table 53 RTC Register Address Mapping

Register name	Description	Offset address
RTC_CTRL	RTC control register	0x00
RTC_CSTS	RTC control/state register	0x04
RTC_PSCRLDH	RTC prescaler reload register high bit	0x08
RTC_PSCRLDL	RTC prescaler reload register low bit	0x0C
RTC_PSCH	RTC prescaler register high bit	0x10
RTC_PSCL	RTC prescaler register low bit	0x14
RTC_CNTH	RTC counter register high bit	0x18
RTC_CNTL	RTC counter register low bit	0x1C
RTC_ALRH	RTC alarm value register high bit	0x20
RTC_ALRL	RTC alarm value register low bit	0x24

18.6 Register Functional Description

18.6.1 RTC control register (RTC_CTRL)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	SECIEN	R/W	Second Interrupt Enable 0: Disable 1: Enable
1	ALRIEN	R/W	Alarm Interrupt Enable 0: Disable 1: Enable
2	OVRIEN	R/W	Overflow Interrupt Enable 0: Disable 1: Enable
15:3	Reserved		

18.6.2 RTC control/state register (RTC_CSTS)

Offset address: 0x04

Reset value: 0x0020

Field	Name	R/W	Description
0	SECFLG	RC_W0	Second Signal Condition Met Flag This flag can provide a periodic signal (usually 1 second) for the RTC counter. When the 32-bit programmable prescaler overruns, it is set to 1 by hardware and the RTC counter will add by 1; it can be only cleared by writing 0 by software. 0: No second flag 1: Second flag
1	ALRFLG	RC_W0	Alarm Occur Flag When the counter reaches RTC_ALR value, it is set to 1 by hardware; it can be only cleared by writing 0 by software. 0: No alarm 1: Alarm
2	OVRFLG	RC_W0	Overflow Occur Flag When the counter overruns, it is set to 1 by hardware; it can be only cleared by writing 0 by software. 0: No overrun 1: 32-bit programmable counter overrun
3	RSYNCFLG	RC_W0	Registers Synchronized Flag When RTC_CNT, RTC_PSCRLD and RTC_ALR registers have been synchronized, it is set to 1 by hardware; it can be cleared by writing 0 by software. After the APB1 clock is reset or stopped, this bit must be cleared by software, and the user program can correctly read out the values of RTC_CNT, RTC_PSCRLD and RTC_ALR only when it is set to 1 by hardware. 0: Not synchronized 1: Synchronized
4	CFGMFLG	R/W	Configure Mode Enable Flag Write operation can be performed for RTC_CNT, RTC_ALR or RTC_PSCRLD registers only after writing 1 by software and entering the configuration mode; exit the configuration mode after writing 0 by software. 0: Exit configuration mode (start to update RTC register) 1: Enable configuration mode
5	OCFLG	R	RTC Operation Complete Flag Indicate the state of last write of RTC register. 0: Uncompleted; next write operation cannot be executed 1: Completed; next write operation can be executed
15:6	Reserved		

18.6.3 RTC prescaler reload register (RTC_PSCRLD)

This register saves the cycle count value of RTC prescaler, and only when the OCFLG value is 1, can the write operation be performed.

RTC prescaler reload register high bit (RTC_PSCRLDH)

Offset address: 0x08

Reset value: 0x0000

Field	Name	R/W	Description
3:0	PSCRLDH[19:16]	W	RTC Prescaler Reload Value High Setup These bits can be used to define the frequency of time base clock according to the following formula: f_{TBCLK}=f_{RTCCLK}/(RLD [19:0]+1)
15:4	Reserved		

RTC prescaler reload register low bit (RTC_PSCRLDL)

Offset address: 0x0C

Reset value: 0x8000

Field	Name	R/W	Description
15:0	PSCRLDL[15:0]	W	RTC Prescaler Reload Value Low Setup These bits can be used to define the frequency of time base clock according to the following formula: f_{TBCLK}=f_{RTCCLK}/(RLD[19:0]+1)

Note: If the input clock frequency is 32.768kHz (f_{RTCCLK}), write 7FFFh in this register to obtain a signal with a cycle of 1 second.

18.6.4 RTC prescaer register (RTC_PSC)

This register saves the value of RTC_PSCRLD, which is read-only, and can be reloaded by hardware when RTC_PSCRLD or RTC_CNT register changes.

RTC prescaler register high bit (RTC_PSCH)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
3:0	PSCH[19:16]	R	RTC Clock Prescaler High Setup
15:4	Reserved		

RTC prescaler register low bit (RTC_PSCL)

Offset address: 0x14

Reset value: 0x8000

Field	Name	R/W	Description
15:0	PSCL[15:0]	R	RTC Clock Prescaler Low Setup

18.6.5 RTC counter register (RTC_CNT)

When the OCFLG value is 1, write operation is allowed; when read operation is performed, the count value (system time) in the counter will be returned directly.

RTC counter register high bit (RTC_CNTH)

Offset address: 0x18

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNTH[31:16]	R/W	RTC Counter High Setup

RTC counter register low bit (RTC_CNTL)

Offset address: 0x1C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNTL[15:0]	R/W	RTC Counter Low Setup

18.6.6 RTC alarm value register (RTC_ALR)

Write operation can be performed when OCFLG value is 1.

RTC alarm value register high bit (RTC_ALRH)

Offset address: 0x20

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	ALRH[31:16]	W	RTC Alarm Value High Setup

RTC alarm value register low bit (RTC_ALRL)

Offset address: 0x24

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	ALRL[15:0]	W	RTC Alarm Value Low Setup

19 Universal Synchronous/Asynchronous Transceiver (USART)

19.1 Full Name and Abbreviation Description of Terms

Table 65 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Clear to Send	CTS
Request to Send	RTS
Most Significant Bit	MSB
Least Significant Bit	LSB
Guard	GRD
Overrun	OVR

19.2 Introduction

USART (universal synchronous/asynchronous transceiver) is a serial communication device that can flexibly exchange full-duplex and half-duplex data with external devices, and meets the requirements of external devices for industry standard NRZ asynchronous serial data format. USART also provides a wide range of baud rate for selection and supports multiprocessor communication.

USART not only supports standard asynchronous transceiver mode, but also supports some other serial data exchange modes, such as LIN protocol, smart card protocol, IrDA SIR ENDEC specification and hardware flow control mode.

USART also supports DMA function to realize high-speed data communication.

19.3 Main Characteristics

（1） Full duplex asynchronous communication

（2） Single-line half-duplex communication

（3） NRZ standard format

（4） Characteristics of programmable serial port:

- Data bit: 8 or 9 bits
- Check bits: Even parity check, odd parity check, no check
- Support 0.5, 1, 1.5 and 2 stop bits

（5） Check control

- Transmit the check bit
- Check the received data

（6） Independent transmitter and receiver enable bit

（7） programmable baud rate generator, with baud rate of up to 4.5Mbits/s

（8） Multiprocessor communication:
- If the address does not match, it will enter the mute mode
- Wake up from mute mode through idle bus detection or address flag detection

（9） Synchronous transmission mode

（10） Generation and detection of LIN break frame

（11） Support the smart card interface of ISO7816-3 standard

（12） Support IrDA protocol

（13） Support hardware flow control

（14） DMA can be used for continuous communication

（15） State flag bit:
- Transmission detection flag: The transmit register is empty, the receive register is not empty, and transmission is completed
- Error detection flag: Overrun error, noise error, parity error, frame error

（16） Multiple interrupt sources:
- The transmit register is empty
- Transmission is completed
- CTS changed
- The receive register cannot be empty
- Overload error
- Bus idle
- Parity error
- LIN disconnection detection
- Noise error
- Overrun error
- Frame error

19.4 Functional Description

Table 54 USART Pin Description

Pin	Type	Description
USART_RX	Input	Data receiving

Pin	Type	Description
USART_TX	Output I/O (single-line mode/smart card mode)	Data transmission When the transmitter is enabled and does not transmit data, the default is high
USART_CK	Output	Clock output
USART_nRTS	Input	Request to send in hardware flow control mode
USART_nCTS	Output	Clear to send in hardware flow control mode
IrDA_RDI	Input	Data input in IrDA mode
IrDA_TDO	Output	Data output in IrDA mode

19.4.1 Single-line Half-duplex Communication

HDEN bit of USART_CTRL3 register determines whether to enter the single-line half-duplex mode.

When USART enters single-line half-duplex mode:

- The CLKEN and LINMEN bit of USART_CTRL2 register, and IREN and SCEN bits of USART_CTRL3 register must be cleared.
- RX pin is disabled.
- TX pin should be configured as open-drain output and connected with RX pin inside the chip.
- Sending data and receiving data can not be carried out at the same time. The data cannot be received before they are transmitted. If needing to receive data, enabling receiving can be turned on only after TXCFLG bit of USART_STS register is set to 1.
- If there is data conflict on the bus, software management is needed to allocate the communication process.

19.4.2 Frame Format

The frame format of data frame is controlled by USART_CTRL1 register

- DBLCFG bit controls the character length, which can be set to 8 or 9 bits.
- PCEN bit controls to enable the check bit or not.
- PCFG bit controls the parity bit to be odd or even.

Table 55 Frame Format

DBLCFG bit	PCEN bit	USART data frame
0	0	Start bit+8-bit data+stop bit
0	1	Start bit+7-bit data+odd-even parity check bit+stop bit
1	0	Start bit+9-bit data+stop bit
1	1	Start bit+8-bit data+odd-even parity check bit+stop bit

Configurable stop bit

Four different stop bits can be configured through STOPCFG bit of USART_CTRL2 register.

- 1 stop bit: Default stop bit.
- 0.5 stop bit: Used when receiving data in smart card mode.
- 2 stop bits: Used in normal mode, single-line mode and hardware flow control mode.
- 1.5 stop bits: Used when sending and receiving data in smart card mode.

Check bit

PCFG bit of USART_CTRL1 determines the parity check bit; when PCFG=0, it is even parity check, on the contrary, it is odd parity check.

- Even check: When the number of frame data and check bit 1 is even, the even check bit is 0; otherwise it is 1.
- Odd check: When the number of frame data and check bit 1 is even, the odd check bit is 1; otherwise it is 0.

19.4.3 Transmitter

When TXEN bit of the register USART_CTRL1 is set, the transmit shift register will output data through TX pin and the corresponding clock pulses will be output through CK pin.

19.4.3.1 Character Transmit

DuringTransmitting period of USART, the least significant bit of the data will be moved out by TX pin first. In this mode, USART_ DATA register has a buffer between the internal bus and the transmitter shift register.

A data frame is composed of the start bit, character and stop bit, so there is a low-level start bit in front of each character; then there is a high-level stop bits the number of which is configurable.

Transmission configuration steps

- Set UEN bit of USART_CTRL1 register to enable USART.
- Decide the word length by setting DBLCFG bit of USART_CTRL1 register.
- Decide the number of stop bits by setting STOPCFG bit of USART_CTRL2 register.
- If multi-buffer communication is selected, DMA should be enabled in USART_CTRL3 register.
- Set the baud rate of communication in USART_BR register.
- Enable TXEN bit in USART_CTRL1 register, and Transmit an idle frame.
- Wait for TXBEFLG bit of USART_STS register to be set to 1.

- Write data to USART_DATA register (if DMA is not enabled, repeat steps 7-8 for each byte to be transmitted).
- Wait for TXCFLG bit of USART_STS register to be set to 1, indicating transmission completion.

Note: TXEN bit cannot be reset during data transmission; otherwise, the data on TX pin will be destroyed, which is because if the baud rate generator stops counting, the data being transmitted will be lost.

19.4.3.2 Single-byte communication

TXBEFLG bit can be cleared by writing USART_DATA register. When the TXBEFLG bit is set by hardware, the shift register will receive the data transferred from the data transmit register, then the data will be transmitted, and the data transmit register will be cleared. The next data can be written in the data register without covering the previous data.

（1） If TXBEIEN in USART_CTRL1 register is set to 1, an interrupt will be generated.

（2） If USART is in the state of transmitting data, write to the data register to save the data to the DATA register, and transfer the data to the shift register at the end of the current data transmission.

（3） If USART is in idle state, write to the data register, put the data into the shift register, start Transmitting data, and set TXBEFLG bit to 1.

（4） When a data transmission is completed and TXBEFLG bit is set, TXCFLG bit will be set to 1; at this time if TXCIEN bit in USART_CTRL1 register is set to 1, an interrupt will be generated.

（5） After the last data is written in the USART_DATA register, before entering the low-power mode or before closing the USART module, wait to set TXCFLG to 1.

19.4.3.3 Break frame

The break frames are considered to receive 0 in a frame period. Setting TXBF bit of USART_CTRL1 register can Transmit a break frame, and the length of the break frame is determined by DBLCFG bit of USART_CTRL1 register. If the TXBF bit is set, after completion of transmission of current data, the TX line will Transmit a break frame, and after completion of transmission of break frame, the TXBF bit will be reset. At the end of the break frame, the transmitter inserts one or two stop bits to respond to the start bit.

Note: If the TXBF bit is reset before transmission of the break frame starts, the break frame will not be transmitted. To transmit two consecutive break frames, the TXBF bit should be set after the stop bit of the previous disconnection symbol.

19.4.3.4 Idle frame

The idle frame is regarded as a complete data frame composed entirely of 1,

followed by the start bit of the next frame containing the data. Set TXEN bit of USART_CTRL1 register to 1 and one idle frame can be set before the first data frame.

19.4.4 Receiver

19.4.4.1 Character receiving

During receiving period of USART, RX pin will first introduce the least significant bit of the data. In this mode, USART_ DATA register has a buffer between the internal bus and the receiver shift register. The data is transmitted to the buffer bit by bit. When fully receiving the data, the corresponding receiver register is not empty, then the user can read USART_ DATA.

Receiving configuration steps

- Set UEN bit of USART_CTRL1 register to enable USART.
- Decide the word length by setting DBLCFG bit of USART_CTRL1 register.
- Decide the number of stop bits by setting STOPCFG bit of USART_CTRL2 register.
- If multi-buffer communication is selected, DMA should be enabled in USART_CTRL3 register.
- Set the baud rate of communication in USART_BR register.
- Set RXEN bit of USART_CTRL1 to enable receiving.

Note:

(1) RXEN bit cannot be reset during data receiving period; otherwise, the bytes being received will be lost.

(2) In the process when the receiver is receiving a data frame, if overrun error, noise error or frame error is detected, the error flag will be set to 1.

(3) When data is transferred from the shift register to USART_DATA register, the RXBNEFLG bit of USART_STS will be set by hardware.

(4) An interrupt will be generated if RXBNEIEN bit is set.

(5) In single buffer mode, the RXBNEFLG bit can be cleared by reading USART_DATA register by software or by writing 0.

(6) In multi-buffer mode, after each byte is received, RXBNEFLG bit of USART_STS register will be set to 1, and DMA will read the data register to clear it.

19.4.4.2 Break frame

When the receiver receives a break frame, USART will handle it as receiving a frame error.

19.4.4.3 Idle frame

When the receiver receives an idle frame, USART will handle it as receiving an

ordinary data frame; if IDLEIEN bit of USART_CTRL1 is set, an interrupt will be generated.

19.4.4.4 Overrun error

When RXBNEFLG bit of USART_STS register is set to 1 and a new character is received at the same time, an overrun error will be caused. Only after RXEN is reset, can the data be transferred from the shift register to DATA register. RXBNEFLG bit will be set to 1 after receiving the byte. This bit needs to be reset before receiving the next data or serving the previous DMA request; otherwise, an overrun error will be caused.

When an overrun error occurs

- USART_STS OVREFLG bit set to 1.
- The data in DATA register will not be lost.
- The data in the shift register received before will be overwritten, but the data received later will not be saved.
- If RXBNEIEN bit of USART_CTRL1 is set to 1, an interrupt will be generated.
- When OVREFLG bit is set to 1, it means that the data has been lost. There are two possibilities:
  - When RXBNEFLG=1, the previous valid data is still on DATA register, and can be read.
  - When RXBNEFLG=0, there is no valid data in DATA register.
- The OVREFLG bit can be reset through read operation for USART_STS and USART_DATA registers.

19.4.4.5 Noise error

When noise is detected in receiving process of the receiver:

- Set NE flag on the rising edge of RXBNEFLG bit of USART_STS register.
- Invalid data is transmitted from the shift register to USART_DATA register.

19.4.4.6 Frame error

If the stop bit is not received and recognized at the expected receiving time due to excessive noise or lack of synchronization, a frame error will be detected.

When a frame error is detected in receiving process of the receiver:

（1） Set the FEFLG bit of USART_STS register.

（2） Invalid data is transmitted from the shift register to USART_DATA register.

（3） In single byte communication, there is no interrupt, but in multi-buffer communication, an interrupt will be generated by setting the ERRIEN bit of USART_CTRL3 register.

19.4.5 Baud Rate Generator

The baud rate division factor (USARTDIV) is a 16-digit number consisting of 12-digit integer part and 4-digit decimal part. Its relationship with the system clock:

Baud rate=PCLK/16×(USARTDIV)

The system clock of USART2/3 is PCLK1, and that of USART1 is PCLK2. USART can be enabled only after the clock control unit enables the system clock.

19.4.6 Multi-processor Communication

In multi-processor communication, multiple USARTs are connected to form a network. In this network, two devices communicate with each other, and the mute mode can be enabled for other devices not participating in the communication in order to reduce the burden of USART. In mute mode, no receive state bit will be set and all receive interrupts are disabled.

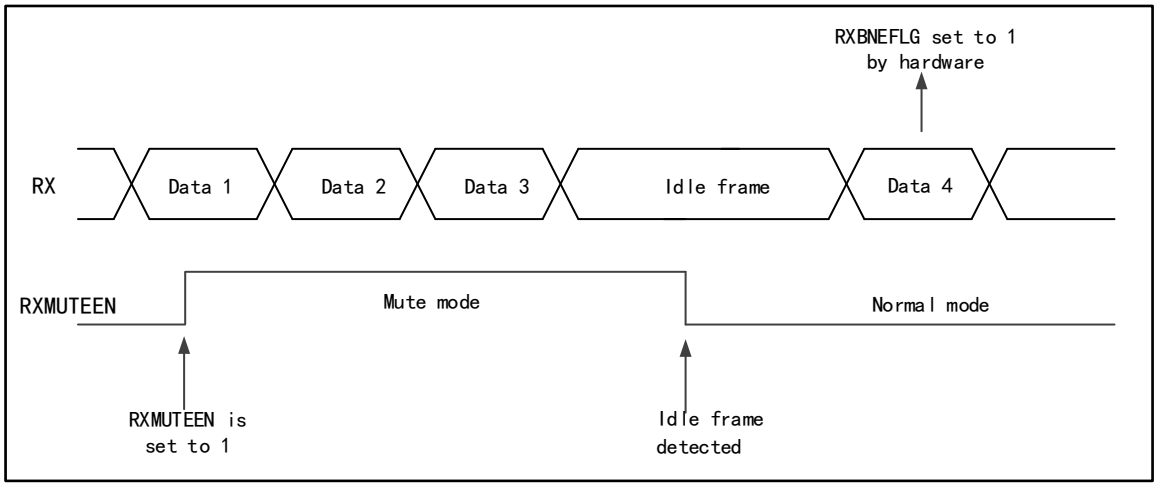
When mute mode is enabled, there are two ways to exit the mute mode:

- WUPMCFG bit is cleared and the bus is idle to exit the mute mode.
- WUPMCFG bit is set and after receiving the address flag, it can exit the mute mode.

Idle bus detection (WUPMCFG=0)

When RXMUTEEN is set to 1, USART enters the mute mode, and it can be waken up from the mute mode when an idle frame is detected, meanwhile, the RXMUTEEN bit will be cleared by the hardware. RXMUTEEN can also be cleared by software.

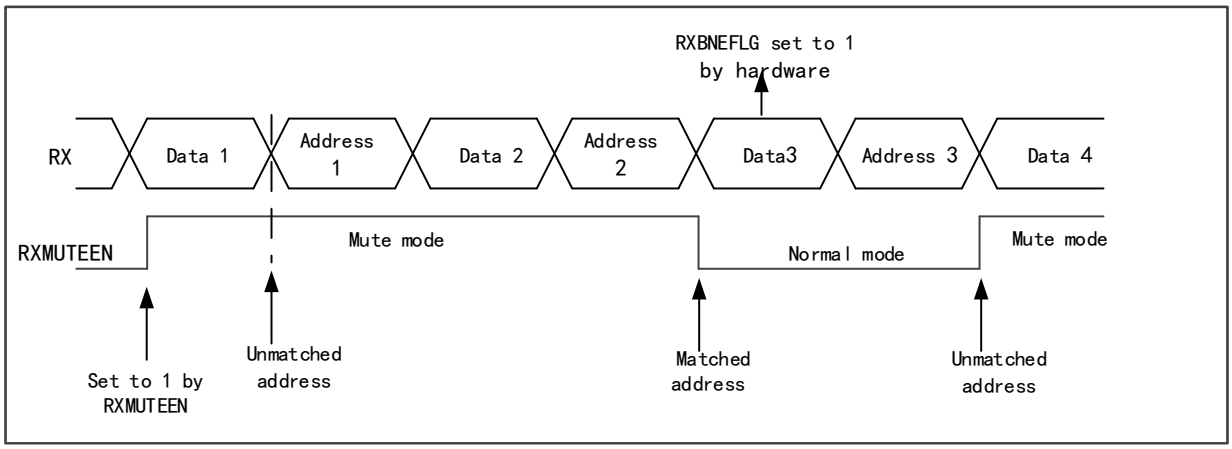
Figure 64 Idle Bus Exit Mute Mode



Address flag detection (WUPMCFG=1)

If the address flag bit is 1, this byte is regarded as the address. The storage address of lower four bits of the address bytes will first be compared with its own address when the receiver receives the address byte. If the addresses do not match, the receiver will enter the mute mode. If the addresses match, the receiver will wake up from the mute mode and be ready to receive the next byte. If the address byte is received again after exiting the mute mode, but the address does not match its own address, the receiver will enter the mute mode again.

Figure 65 Address Flag Exit Mute Mode



19.4.7 Synchronous Mode

The synchronous mode supports full duplex synchronous serial communication in master mode, and has one more signal line USART_CK which can output synchronous clock than the asynchronous mode.

CLKEN bit of USART_CTRL2 register decides whether to enter the synchronous mode.

When USART enters the synchronous mode:

- The LINMEN bit of USART_CTRL2 register, and IREN, HDEN and SCEN bits of USART_CTRL3 register must be cleared.
- The start bit and stop bit of data frame have no clock output.
- Whether the last data bit of data frame generates USART_CK clock is decided by the LBCPOEN bit of USART_CTRL2 register.
- The clock polarity of USART_CK is decided by CPOL bit of USART_CTRL2 register.
- The phase of USART_CK is decided by the CPHA bit of USART_CTRL2.
- The external CK clock cannot be activated when the bus is idle or the frame is disconnected.

Figure 66 USART Synchronous Transmission Example

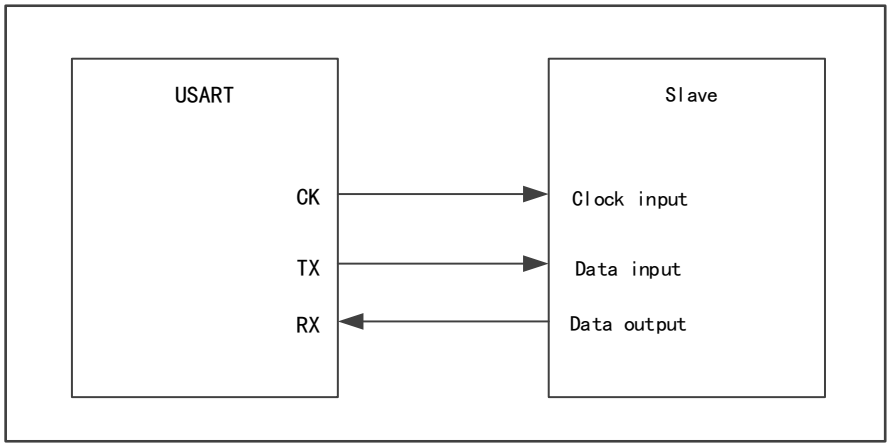


Figure 67 USART Synchronous Transmission Timing Diagram (DBLCFG=0)

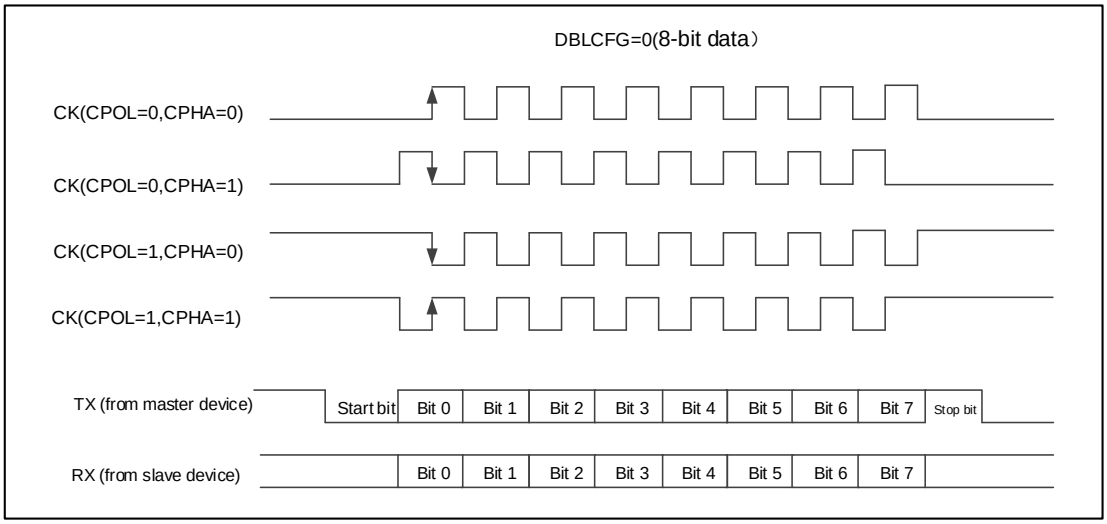
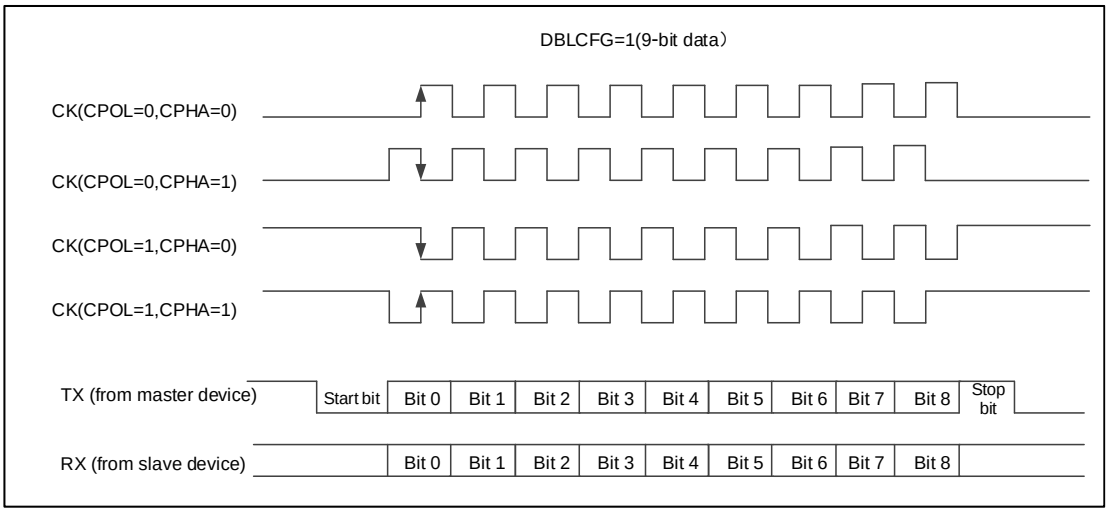


Figure 68 USART Synchronous Transmission Timing Diagram (DBLCFG=1)



19.4.8 LIN Mode

LINMEN bit of USART_CTRL2 register decides whether to enter LIN mode.

When entering LIN mode:

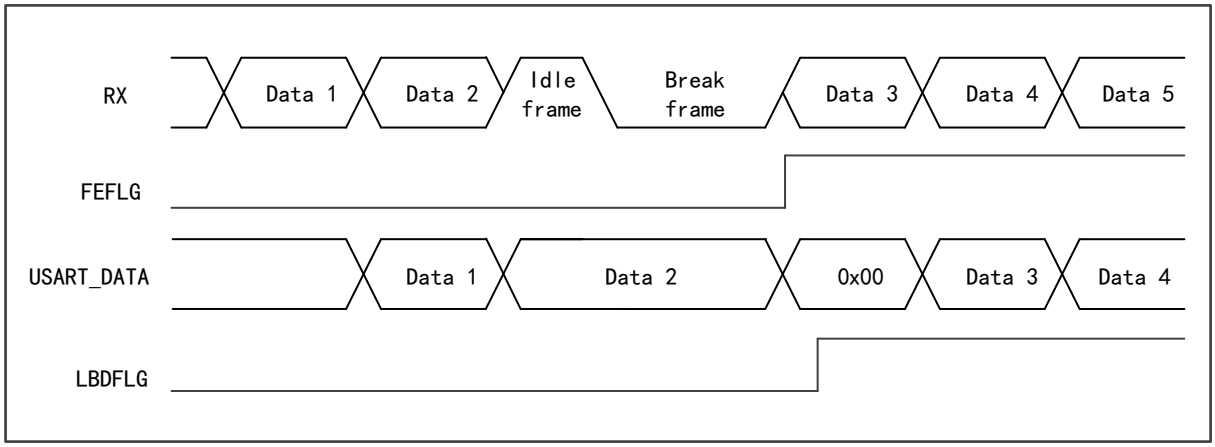
- All data frames are 8 data bits and 1 stop bit.
- The CLKEN bit and STOPCFG bit of USART_CTRL2 register and IREN bit, HDEN bit and SCEN bit of USART_CTRL3 register need to be cleared.

In LIN master mode, USART can generate break frame, and the detection length of break frame can be set to 10 bits and 11 bits through LBDLCFG bit of USART_CTRL2. The break frame detection circuit is independent of USART receiver, and no matter in idle state or in data transmission state, RX pin can detect the break frame, and LBDFLG bit of USART_STS register is set to 1; at this time, if LBDIEN bit of USART_CTRL2 is enabled, an interrupt will be generated.

Detection of break frame in idle state

In idle state, if a break frame is detected on RX pin, the receiver will receive a data frame of 0 and generate FEFLG.

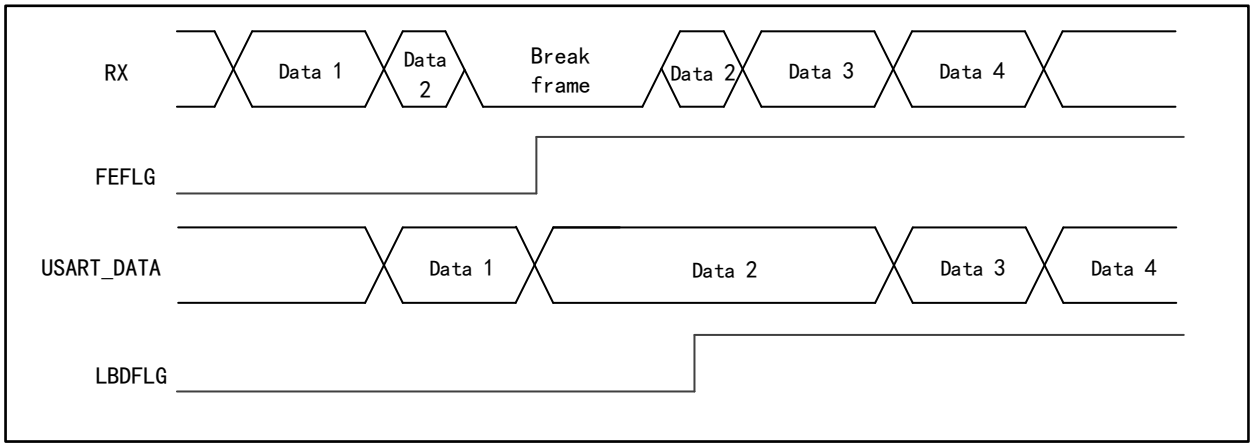
Figure 69 Break Frame Detection in Idle State



Detection of break frame in data transmission state

In the process of data transmission, if the RX pin detects the break frame, the currently transmitted data frame will generate FEFLG.

Figure 70 Break Frame Detection in Data Transmission State



19.4.9 Smart card mode

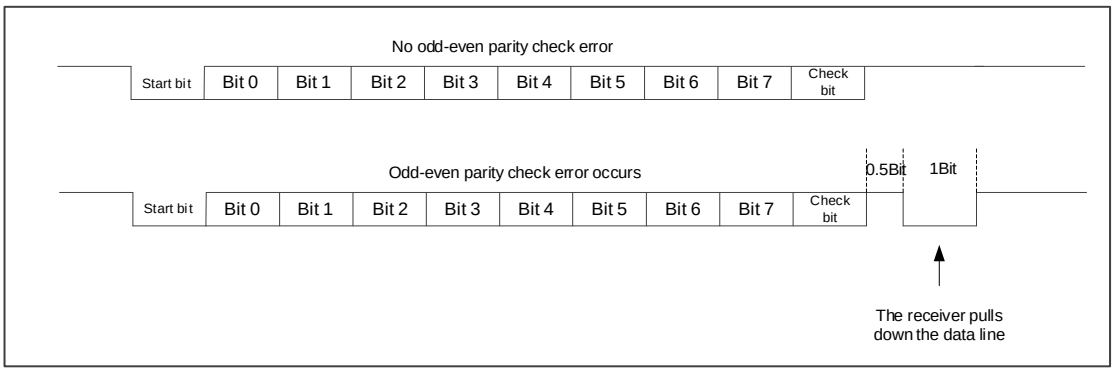
Smart card mode is a single-line half-duplex communication mode. The interface supports ISO7816-3 standard protocol and can control the reading and writing of smart cards that meet the standard protocol.

SCEN bit of USART_CTRL3 register decides whether to enter the smart card mode.

When USART enters the smart card mode:

- The LINMEN bit of USART_CTRL2 register, and IREN and HDEN bits of USART_CTRL3 register must be cleared.
- The data frame format is 8 data bits and 1 check bit, and 0.5 or 1.5 stop bits are used. (To avoid switching between two configurations, it is recommended to use 1.5 stop bits when transmitting and receiving data)
- CLKEN bit of USART_CTRL2 can be set to provide clocks for smart card.
- During the communication, when the receiver detects a parity error, in order to inform the transmitter that the data has not been received successfully, the data line will be pulled down after half a baud rate clock, and keep pulling down for one baud rate clock.
- The break frame has no meaning in smart card mode. A 00h data with frame error will be regarded as a data instead of disconnection symbol.

Figure 71 ISO7816-3 Standard Protocol



19.4.10 Infrared (IrDA SIR) Function Mode

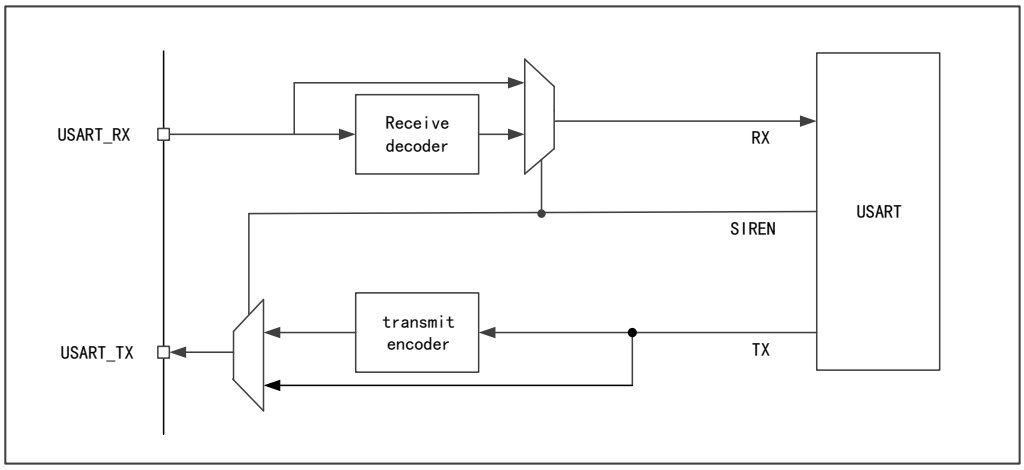
IrDA mode is a half-duplex protocol, transmitting and receiving data can not be carried out at the same time, and the delay between data transmitting and receiving should be more than 10ms.

IREN bit of USART_CTRL3 register decides whether to enter the IrDA mode.

When USART enters the IrDA mode:

- The CLKEN bit, STOPCFG bit and LINMEN bit of USART_CTRL2 register and HDEN bit and SCEN bit of USART_CTRL3 register must be cleared.
- The data frame uses 1 stop bit and the baud rate is less than 115200Hz.
- Using infrared pulse (RZI) indicates logic 0, so in normal mode, its pulse width is 3/16 baud rate cycles. When IrDA is in low power mode, it is recommended that the pulse width be greater than three DIV frequency division clocks so as to ensure that this pulse can be detected by IrDA normally.

Figure 72 IrDA Mode Block Diagram

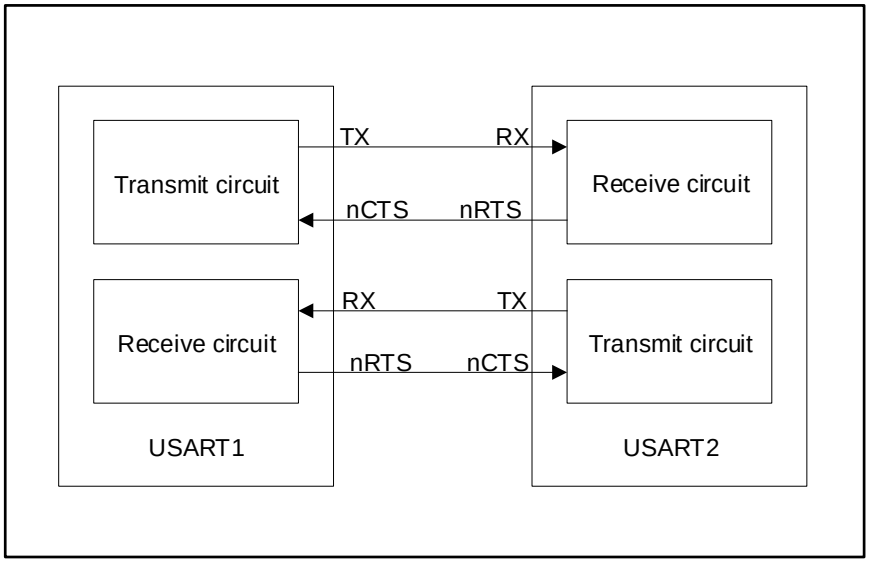


19.4.11 Hardware Flow Control

The function of hardware flow control is to control the serial data flow between

two devices through nCTS pin and nRTS pin.

Figure 73 Hardware Flow Control between Two USARTs



CTS flow control

CTSEN bit of USART_CTRL3 register determines whether CTS flow control is enabled. If CTS flow control is enabled, the transmitter will detect whether the data frame of nCTS pin can be transmitted. If TXBEFLG bit=0 for USART_STS register and nCTS is pulled to low level, the data frame can be transmitted. If nCTS becomes high during transmission, the transmitter will stop transmitting after the current data frame is transmitted.

RTS flow control

RTSEN bit of USART_CTRL3 register determines whether RTS flow control is enabled. If RTS flow control is enabled, when the receiver receives data, nRTS will be pulled to low level. When a data frame is received, nRTS will becomes high to inform the transmitter to stop transmitting data frame.

19.4.12 DMA Multi-buffer Communication

USART can access the data buffer in DMA mode in order to reduce the burden of processors.

Transmission in DMA mode

DMATXEN bit of USART_CTRL3 register determines whether to transmit in DMA mode. When transmitting by DMA, the data in the designated SRAM will be transmitted to the buffer by DMA.

Configuration steps of transmission by DMA:

- Clear the TXCFLG bit of USART_STS register.

- Set the address of SRAM memory storing data as DMA source address.
- Set the address of USART_DATA register as DMA destination address.
- Set the number of data bytes to be transmitted.
- Set channel priority.
- Set interrupt enable.
- Enable DMA channel.
- Wait for TXCFLG bit of USART_STS register to be set to 1, indicating transmission completion.

Receive in DMA mode

DMARXEN bit of USART_CTRL3 register determines whether to receive by DMA. When receiving by DMA, every time one byte is received, the data in the receive buffer will be transmitted to the designated SRAM area by DMA.

Configuration steps of receiving by DMA:

- Set the address of USART_DATA register as DMA source address.
- Set the address of SRAM memory storing data as DMA destination address.
- Set the number of data bytes to be transmitted.
- Set channel priority.
- Set interrupt enable.
- Enable DMA channel.

19.4.13 Interrupt Request

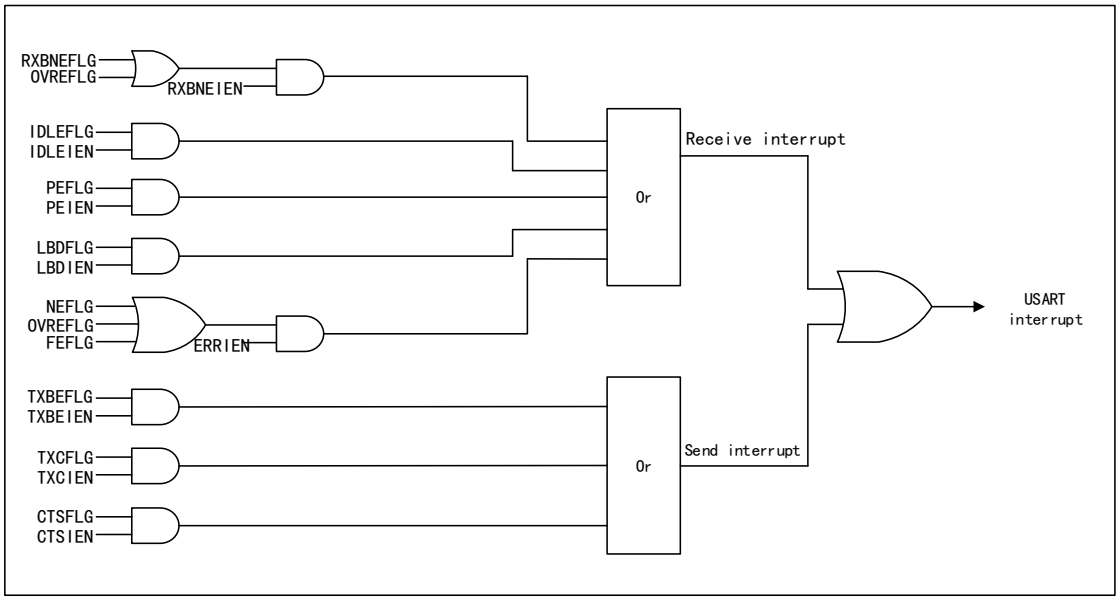
Table 56 USART Interrupt Request

Interrupt event		Event flag bit	Enable bit
The receive register is not empty		RXBNEFLG	RXBNEIEN
Overload error		OVREFLG	
Line idle is detected		IDLEFLG	IDLEIEN
Odd-even parity error		PEFLG	PEIEN
LIN break frame flag		LBDFLG	LBDIEN
Receiving error in DMA mode	Noise error	NEFLG	ERRIEN
	Overrun error	OVREFLG	
	Frame error	FEFLG	
Data transmit register is empty		TXBEFLG	TXBEIEN
Transmission is completed		TXCFLG	TXCIEN
CTS flag		CTSFLG	CTSIEN

All interrupt requests of USART are connected to the same interrupt controller,

and the interrupt requests have logical or relational before they are transmitted to the interrupt controller.

Figure 74 USART Interrupt Mapping



19.4.14 Comparison of USART Supporting Functions

Table 57 Comparison of USART Supporting Functions

USART mode	USART1	USART2	USART3	UART4	UART5
Asynchronous mode	√	√	√	√	√
Hardware flow control	√	√	√	—	—
Multi-buffer communication (DMA)	√	√	√	√	—
Multi-processor communication	√	√	√	√	√
Synchronous	√	√	√	—	—
Smart card	√	√	√	—	—
Half duplex (single-line mode)	√	√	√	√	√
IrDA	√	√	√	√	√
LIN	√	√	√	√	√

Note: "√" means this function is supported, while "—" means that this function is not supported.

19.5 Register Address Mapping

Table 70 USART Register Address Mapping

Register name	Description	Offset address
USART_STS	State register	0x00

Register name	Description	Offset address
USART_DATA	Data register	0x04
USART_BR	Baud rate register	0x08
USART_CTRL1	Control register 1	0x0C
USART_CTRL2	Control register 2	0x10
USART_CTRL3	Control register 3	0x14
USART_GTPSC	Protection time and prescaler register	0x18

19.6 Register Functional Description

19.6.1 State register (USART_STS)

Offset address: 0x00

Reset value: 0x00C0

Field	Name	R/W	Description
0	PEFLG	R	Parity Error Occur Flag 0: No error 1: Parity error occurs In the receiving mode, when a parity error occurs, set to 1 by hardware; This bit can be cleared by software; after setting of RXBNEFLG, first read USART_STS register, and then read USART_DATA register to complete clearing.
1	FEFLG	R	Frame Error Occur Flag 0: No frame error 1: A frame error or disconnection symbol appeared When there is synchronous dislocation, too much noise or disconnection symbol, set to 1 by hardware; This bit can be cleared by software; first read USART_STS register, and then read USART_DATA register to complete clearing.
2	NEFLG	R	Noise Error Occur Flag 0: No noise 1: There is noise error When there is noise error, set to 1 by hardware; This bit can be cleared by software; first read USART_STS register, and then read USART_DATA register to complete clearing.
3	OVREFLG	R	Overrun Error Occur Flag 0: Overrun error 1: Overrun error occurred When the RXBNEFLG bit is set and the data in the shift register is to be transmitted to the receiver register, set to 1 by hardware; This bit can be cleared by software; first read USART_STS register, and then read USART_DATA register to complete clearing.

Field	Name	R/W	Description
4	IDLEFLG	R	IDLE Line Detected Flag 0: Idle bus is not detected 1: Idle bus is detected When idle bus is detected, set to 1 by hardware; This bit can be cleared by software; first read USART_STS register, and then read USART_DATA register to complete clearing.
5	RXBNEFLG	RC_W0	Receive Data Buffer Not Empty Flag 0: The receive data buffer is empty 1: The receive data buffer is not empty When the data register receives the data transmitted by the receiver shift register, set to 1 by hardware; This bit can be cleared by software; read USART_DATA to clear, or write 0 to this bit to clear it.
6	TXCFLG	RC_W0	Transmit Data Complete Flag 0: Sending data is not completed 1: Sending data is completed After the last frame of data is transmitted and the TXBEFLG is set, set to 1 by hardware; This bit can be cleared by software; first read USART_STS register, and then write USART_DATA register to complete clearing; or this bit can be cleared by writing 0 to it.
7	TXBEFLG	R	Transmit Data Buffer Empty Flag 0: The transmit data buffer is not empty 1: The transmit data buffer is empty When the shift register receives the data transmitted by the transmitter data register, set to 1 by hardware; This bit can be cleared by software; write USART_DATA register to complete clearing.
8	LBDFLG	RC_W0	LIN Break Detected Flag 0: LIN disconnection not detected 1: LIN disconnection detected When LIN disconnection is detected, set to 1 by hardware; This bit can be cleared by software; or cleared by writing 0 to this bit.
9	CTSFLG	RC_W0	CTS Change Flag 0: No change on nCTS state line 1: There is change on nCTS state line If the CTSEN bit is set, when switching to the nCTS input, set to 1 by hardware; This bit can be cleared by software; or cleared by writing 0 to this bit.
31:10	Reserved		

19.6.2 Data register (USART_DATA)

Offset address: 0x04

Reset value: 0xXXXX XXXX, X=undefined bit

Field	Name	R/W	Description
8:0	DATA	R/W	Data Value Transmit or receive the data value; read data when receiving data, and write data to the register when transmitting data. When the parity bit is enabled, for 9 data bits, the 8 bit of DATA is parity bit; for 8 data bits, the 7 bit of DATA is parity bit.
31:9	Reserved		

19.6.3 Baud rate register (USART_BR)

Offset address: 0x08

Reset value: 0x0000Reset value: 0x0000

Field	Name	R/W	Description
3:0	FBR[3:0]	R/W	Fraction of USART Baud Rate Divider factor The decimal part of USART baud rate division factor is determined by these four bits.
15:4	IBR[15:4]	R/W	Integer of USART Baud Rate Divider factor The integral part of USART baud rate division factor is determined by these 12 bits.
31:16	Reserved		

19.6.4 Control register 1 (USART_CTRL1)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	TXBF	R/W	Transmit Break Frame 0: Not transmit 1: Will transmit This bit can be set by software and cleared by hardware when the stop bit of the break frame is transmitted.
1	RXMUTEEN	R/W	Receive Mute Mode Enable 0: Normal working mode 1: Mute mode This bit is set or cleared by software, or cleared by hardware when wake-up sequence is detected. USART must receive a data before it is put in the mute mode, so that it can be detected and awakened by idle bus. In the wake-up of address flag detection, if the RXBNEFLG bit is set, the RXMUTEEN bit cannot be modified by software.
2	RXEN	R/W	Receive Enable 0: Disable 1: Enable, and start to detect the start bit on RX pin

Field	Name	R/W	Description
3	TXEN	R/W	Transmit Enable 0: Disable 1: Enable Except in smart card mode, if there is a 0 pulse on this bit at any time of transmitting data, an idle bus will be transmitted after the current data is transmitted. After this bit is set, the data will be transmitted after one-bit time.
4	IDLEIEN	R/W	IDLE Interrupt Enable 0: Disable 1: Generate an interrupt when IDLEFLG is set
5	RXBNEIEN	R/W	Receive Buffer Not Empty Interrupt Enable 0: Disable 1: Generate an interrupt when OVREFLG or RXBNEFLG is set
6	TXCIEN	R/W	Transmit Complete Interrupt Enable 0: Disable 1: Generate an interrupt when TXCFLG is set
7	TXBEIEN	R/W	Transmit Buffer Empty Interrupt Enable 0: Interrupt generation is disabled 1: Generate an interrupt when TXBEFLG is set
8	PEIEN	R/W	Parity Error Interrupt Enable 0: Interrupt generation is disabled 1: Generate an interrupt when PEFLG is set
9	PCFG	R/W	Odd/Even Parity Configure 0: Even parity check 1: Odd parity check The selection will not take effect until the current transmission of bytes is completed.
10	PCEN	R/W	Parity Control Enable 0: Disable 1: Enable If this bit is set, a check bit will be inserted in the most significant bit when transmitting data; when receiving data, check whether the check bit of the received data is correct. The check control will not take effect until the current transmission of bytes is completed.
11	WUPMCFG	R/W	Wakeup Method Configure 0: Idle bus wakeup 1: Address flag wakeup
12	DBLCFG	R/W	Data Bits Length Configure 0: 1 start bit, 8 data bits, n stop bits 1: 1 start bit, 9 data bits, n stop bits This bit cannot be modified during transmission of data.
13	UEN	R/W	USART Enable 0: USART frequency divider and output are disabled 1: USART module is enabled
31:14	Reserved		

19.6.5 Control register 2 (USART_CTRL2)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	ADDR[3:0]	R/W	USART Device Node Address Setup This bit is valid only in the mute mode of multiprocessor communication, and decides to enter the mute mode or wake up according to whether the detected address tags are consistent.
4	Reserved		
5	LBDLCFG	R/W	LIN Break Detection Length Configure 0: 10 bits 1: 11 bits
6	LBDIEN	R/W	LIN Break Detection Interrupt Enable 0: Disable 1: Generate an interrupt when LBDFLG bit is set
7	Reserved		
8	LBCPOEN	R/W	Last Bit Clock Pulse Output Enable 0: Not output from CK 1: Output from CK This bit is valid only in synchronous mode; this bit does not exist on UART4 and UART5.
9	CPHA	R/W	Clock Phase Configure This bit indicates on the edge of which clock sampling is conducted 0: The first 1: The second This bit is valid only in synchronous mode; this bit does not exist on UART4 and UART5.
10	CPOL	R/W	Clock Polarity Configure The state of CK pin when USART is in idle state 0: Low level 1: High level This bit is valid only in synchronous mode; this bit does not exist on UART4 and UART5.
11	CLKEN	R/W	Clock Enable (CK pin) 0: Disable 1: Enable This bit does not exist on UART4 and UART5.
13:12	STOPCFG	R/W	STOP Bit Configure 00: 1 stop bit 01: 0.5 stop bit 10: 2 stop bit 11: 1.5 stop bit This bit does not exist on UART4 and UART5.
14	LINMEN	R/W	LIN Mode Enable 0: Disable 1: Enable

Field	Name	R/W	Description
31:15	Reserved		

Note: These three bits (CPOL, CPHA and LBCPOEN) cannot be changed after transmission is enabled.

19.6.6 Control register 3 (USART_CTRL3)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	ERRIEN	R/W	Error Interrupt Enable 0: Disable 1: Enable; when DMARXEN is set and one among FEFLG, OVREFLG or NEFLG is set, an interrupt will be generated.
1	IREN	R/W	IrDA Function Enable 0: Disable 1: Enable
2	IRLPEN	R/W	IrDA Low-power Mode Enable 0: Normal mode 1: Low-power mode
3	HDEN	R/W	Half-duplex Mode Enable 0: Disable 1: Enable
4	SCNACKEN	R/W	NACK Transmit Enable During Parity Error in Smartcard Function 0: NACK is not transmitted 1: Transmit NACK This bit does not exist on UART4 and UART5.
5	SCEN	R/W	Smartcard Function Enable 0: Disable 1: Enable This bit does not exist on UART4 and UART5.
6	DMARXEN	R/W	DMA Receive Enable 0: Disable 1: Enable This bit does not exist on UART4 and UART5.
7	DMATXEN	R/W	DMA Transmit Enable 0: Disable 1: Enable This bit does not exist on UART4 and UART5.
8	RTSEN	R/W	RTS Hardware Flow Control Function Enable 0: Disable 1: Enable RTS interrupt RTS: Require To Send, which is output signal, indicating it has been ready to receive. Request is made to receive data only when there is space in the receive buffer; when data can be received, RTS output is pulled to low level. This bit does not exist on UART4 and UART5.

Field	Name	R/W	Description
9	CTSEN	R/W	CTS Hardware Flow Control Function Enable 0: Disable 1: Enable CTS: Clear To Send, which is input signal When CTS input signal is at low level, the data can be transmitted; otherwise, the data cannot be transmitted; if CTS signal is pulled to high during data transmission, the data transmission will be stopped after the data transmission is completed; if write operation is performed for the data register when CTS is high, the data will not be transmitted until CTS is valid. This bit does not exist on UART4 and UART5.
10	CTSIEN	R/W	CTS Interrupt Enable 0: Disable 1: Generate an interrupt when CTSFLG is set This bit does not exist on UART4 and UART5.
31:11	Reserved		

19.6.7 Protection time and prescaler register (USART_GTPSC)

Offset address: 0x18

Reset value: 0x0000

Field	Name	R/W	Description
7:0	PSC	R/W	Prescaler Factor Setup Divide the frequency and provide clock for the system clock respectively; in different working modes, the valid bits of PSC have difference, specifically as follows: In infrared low-power mode: PSC[7:0] is valid. 00000000: Reserved 00000001: 1 divided frequency 00000010: 2 divided frequency …… 11111111: 255 divided frequency In infrared normal mode: PSC can only be set to 00000001 In smart card mode: PSC[7:5] invalid, PSC[4:0] valid 00000: Reserved 00001: 2 divided frequency 00010: 4 divided frequency 00011: 6 divided frequency …… 11111: 62 divided frequency This bit does not exist on UART4 and UART5.
15:8	GRDT	R/W	Guard Time Value Setup After transmitting data, TXCFLG can be set after the protection time; the time unit is baud clock; it can be applied to smart card mode; this bit does not exist on UART4 and UART5.
31:16	Reserved		

20 Internal Integrated Circuit Interface (I2C)

20.1 Full Name and Abbreviation Description of Terms

Table 58 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Serial Data	SDA
Serial Clock	SCL
System Management Bus	SMBus
Clock	CLK
Serial Clock High	SCLH
Serial Clock Low	SCLL
Address Resolution Protocol	ARP
Negative Acknowledgement	NACK
Packet Error Checking	PEC
Address Resolution Protocol	ARP

20.2 Introduction

I2C is a short-distance bus communication protocol. In physical implementation, I2C bus is composed of two signal lines (SDA and SCL) and a ground wire. These two signal lines can be used for bidirectional transmission.

- Two signal lines, SCL clock line and SDA data line. SCL provides timing for SDA, and SDA transmits/receives data in series
- Both SCL and SDA signal lines are bidirectional
- The ground is common when the two systems use I2C bus for communication

20.3 Main Characteristics

（1） Multi-master function

（2） The master can generate the clock, start bit and stop bit

（3） Slave function

- Programmable I2C address detection
- Double-address mode
- Detection stop bit

（4） 7-bit and 10-bit addressing mode

（5） Response to broadcast

（6） Two communication speeds
- Standard mode
- Fast mode

（7） Programmable clock extension

（8） State flag
- Transmitter/Receiver mode flag
- Flag for end of byte transmission
- Flag of busy bus

（9） Error flag
- Arbitration loss
- Acknowledgment error
- Wrong start bit or stop bit detected

（10） Interrupt source
- Address/Data communication succeeded
- Error interrupt

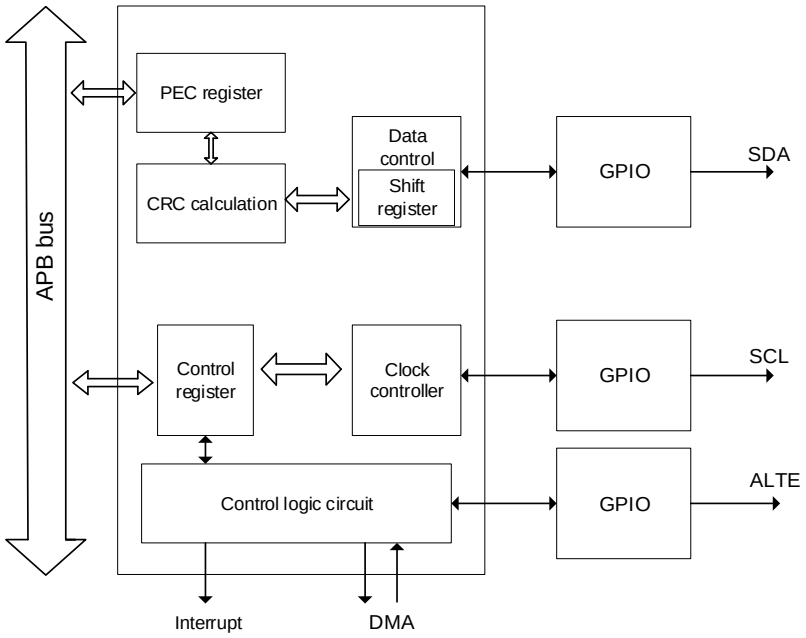
（11） Support DMA function

（12） Programmable PEC
- Final transmission in transmission mode
- PEC error check after the last byte is received

（13） SMBus specific function
- Hardware PEC
- Address resolution protocol

20.4 Structure Block Diagram

Figure 75 I2C Function Structure Diagram



The interface can be configured to the following modes:

- Slave transmitting
- Slave receiving
- Master transmitting
- Master receiving

In the initial state of I2C interface, the working mode is slave mode. After I2C interface sends the start signal, it will automatically switch from slave mode to master mode.

20.5 Functional Description

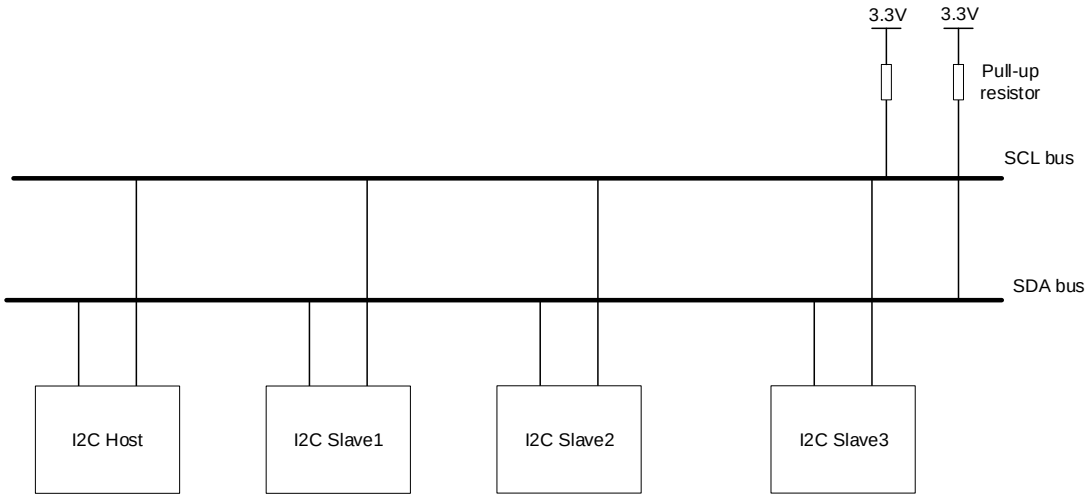
Table 59 Description of Special Terms of I2C Bus

Special terms	Instruction
Transmitter	Device transmitting data to the bus
Receiver	Device receiving data from the bus
Master	Device that initiates data transmission, generates clock signals and ends data transmission
Slave	Device addressed by master
Multiple masters	Multiple masters that control the bus at the same time without destroying information
Synchronous	The process of synchronizing the clock signals between two or more devices
Arbitration	If more than one master tries to control the bus at the same time, only one master can control the bus, and the information of the controlled master will not be destroyed

20.5.1 I2C Physical Layer

The commonly used connection modes between I2C communication devices are shown in the figure below:

Figure 76 Commonly Used I2C Communication Connection Diagram



Characteristics of physical layer:

（1） Bus supporting multiple devices (signal line shared by multiple devices), which, in I2C communication bus, can connect multiple communication masters and communication slaves.

（2） An I2C bus only uses two bus lines, namely, a bidirectional serial data line (SDA) and a serial clock line (SCL). The data line is used for data transmission, and the clock line is used for synchronous receiving and transmission of data.

（3） Each device connected to the bus has an independent address (seven or ten bits), and the master addresses and accesses the slave device according to the address of the device.

（4） The bus needs to connect the pull-up resistor to the power supply. When I2C bus is idle, the output is in high-impedance state. When all devices are idle, the output is in high-impedance state, and the pull-up resistor pulls the bus to high level.

（5） Three communication modes: Standard mode (up to 100KHz), fast mode (up to 400KHz), and fast mode plus (up to 1MHz).

（6） When multiple masters use the bus at the same time, to prevent the data conflict, the bus arbitration mode is adopted to determine which device occupies the bus.

（7） Can program setup and hold time, and program the high-level time and low-level time of SCL in I2C.

20.5.2 I2C Protocol Layer

Characteristics of protocol layer

（1） Data is transmitted in the form of frame, and each frame is composed of 1 byte (8 bits).

（2） In the rising edge phase of SCL, SDA needs to keep stable and SDA changes during the period when SCL is low.

（3） In addition to data frame, I2C bus also has start signal, stop signal and acknowledge signal.

- Start bit: During the stable high level period of SCL, a falling edge of SDA starts transmission.
- Stop bit: During the stable high level period of SCL, a rising edge of SDA stops transmission.
- Acknowledge bit: Used to indicate successful transmission of one byte. After the bus transmitter (regardless of the master or slave) transmits 8-bit data, SDA will release (from output to input). During the ninth clock pulse, the receiver will pull down SDA to respond to the received data.

I2C communication reading and writing process

Figure 77 Master Writes Data to Slave

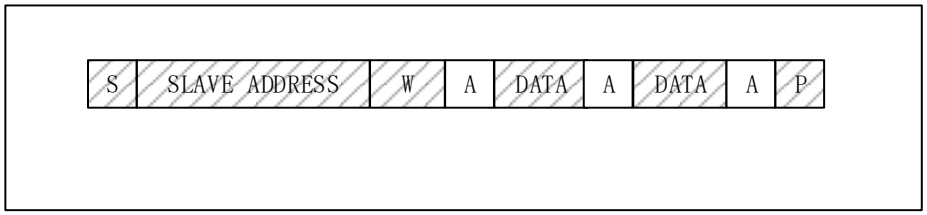
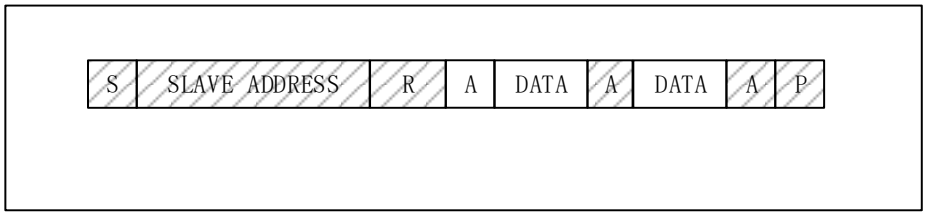


Figure 78 Master Reads Data from Slave



Remarks:

（1）  : This data is transferred from master to slave

（2） S: Start signal

（3） SLAVE ADDRESS: Slave address

（4） □: This data is transferred from slave to master

（5） R/W: Selection bit of transmission direction

（6） 1 means read

（7） 0 means write

（8） P: Stop signal

After the start signal is generated, all slaves will wait for the slave address signal transmitted by the master. In I2C bus, the address of each device is unique. When the address signal matches the device address, the slave will be selected, and the unselected slave will ignore the future data signal.

When the master direction is writing data

After broadcasting the address and receiving the acknowledge signal, the master will transmit data to the slave, the data length is one byte, and every time the master transmits one byte of data, it needs to wait for the answer signal transmitted by the slave. After all the bytes have been transmitted, the master will transmit a stop signal (STOP) to the slave, indicating that the transmission is completed.

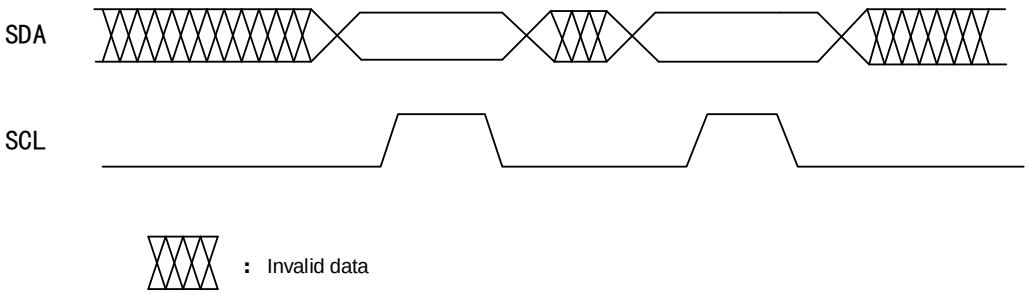
When the master direction is reading data

After broadcasting the address and receiving the acknowledge signal, the slave will transmit the data to the master. The size of the data package is 8 bits. Every time the slave sends one byte of data, it needs to wait for the acknowledge signal of the master. When the master wants to stop receiving data, it needs to return a non-acknowledge signal to the slave, then the slave will stop transmitting the data automatically.

20.5.3 Data Validity

In the process of data transmission, the data on SDA line must be stable when the clock signal SCL is at high level. Only when the SCL is at the low level, can the level state of SDA be changed, and the bit transmission of each data needs a clock pulse.

Figure 79 SDA Timing Diagram



20.5.4 Start and Stop Signals

All data transfer must have start signal (START) and stop signal (STOP).

Figure 80 START signal is defined as: when SCL is at high level, SDA will convert from high level to low level

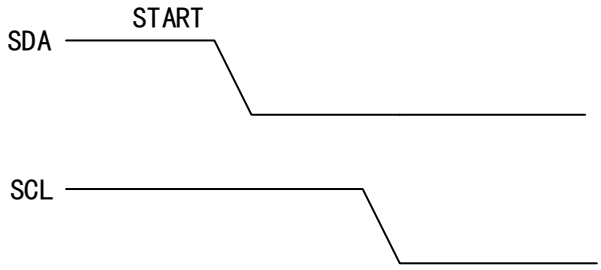
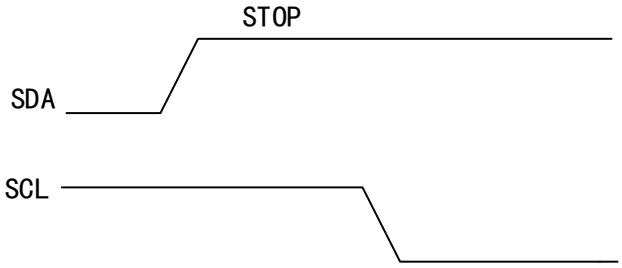


Figure 81 STOP signal is defined as: when SCL is at high level, SDA will convert from low level to high level



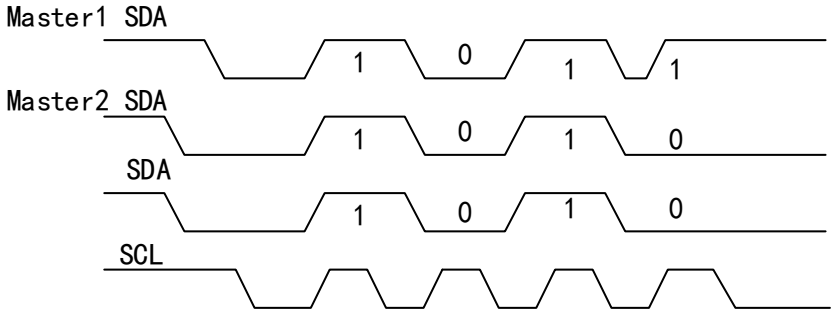
20.5.5 Arbitration

Arbitration is also used to solve the bus control conflict in case of multiple masters. The arbitration process takes place on the master and has nothing to do with the slave.

The master can start transmission only when the bus is idle. Two masters may generate an effective START signal on the bus within the shortest hold time of the START signal. In this situation, it is required by arbitration to decide which master completes the transmission.

Arbitration is conducted by bit. During each arbitration, when SCL is high, each master will check whether the SDA level is the same as that transmitted by itself. The arbitration process needs to last for many bits. Theoretically, if two masters transmit exactly the same content, they can successfully transmit without arbitration failure. If one master transmits high level, but it is detected that SDA is at low level, an arbitration failure error will occur, the SDA output of the master will be closed, and the other master will complete its own transmission.

Figure 82 SDA Timing Diagram



Note: Master 1 arbitration failure

20.5.6 SMBus Specific Function

System management bus (SMBus) is a simple single-end double-wire bus, which can meet the requirements of lightweight communication.

SMBus is commonly used in computer motherboard, mainly for power transmission ON/OFF instructions. SMBus is the derivative bus of I2C. It is mainly used for communication of low-bandwidth devices on computer motherboard, and power-related chip.

Address resolution protocol

SMBus specification includes an address resolution protocol, which can realize dynamic address assignment. Dynamic recognition hardware and software enable the bus to support hot plugging, and the bus devices will be automatically identified and assigned with a unique address.

SMBus alarm

SMBus alarm is an optional signal with an interrupt line for pins that are sacrificed to extend their control ability.

20.5.7 Error Flag Bit

Table 60 The following several error flag bits exist in I2C communication

Error flag bit	Description of error flag bit
Answer error flag bit (AEFLG)	No answer received
Bus error flag bit (BERRFLG)	An external stop or start condition is detected
Arbitration loss flag bit (ALFLG)	Arbitration loss is detected by the interface
Overrun/Underrun error flag bit (OVRURFLG)	In slave mode, the received data is not read out, the next data has arrived, and an overrun error occurs. The transmitting data clock has arrived, but the data has not been written into the DATA register, and an underrun error occurs.
Timeout or Tow error flag bit (TTEFLG)	SCL is pulled down for more than a certain time
PEC comparison error flag bit (PECEFLG)	CRC values are not equal

20.5.8 Message Error Check (PEC)

I2C module has a PEC module, which checks the message of I2C data by CRC-8 calculator. The CRC-8 polynomial used by the calculator is: $C(x)= X^8+X^2+X+1$.

When PECEN bit is set to 1 and PEC function is enabled, PEC module will calculate all data transmitted by I2C bus, including address data.

20.5.9 DMA Mode

According to the software process of I2C, when the transmitter register is empty or the receiver register is full, MCU needs to write or read bytes, then we can complete the operation more quickly through the DMA function of I2C.

DMA transmission

Set the DMAEN bit in I2C_CTRL2 register to enabe the DMA mode. When the transmitter register is empty (TXBEFLG is set to 1), the data will be directly loaded from the memory area to the DATA register through DMA.

DMA receiving

Set DMAEN in I2C_CTRL2 register to enable DMA mode. When the receiving register is full (RXBNEFLG is set to 1), DMA will transmit DATA register data to the set storage area.

20.5.10 I2C Interrupt

Table 61 I2C Interrupt Request

Interrupt event	Event flag bit	Interrupt control bit
Transmitting start bit completed	STARTFLG	EVIEN
Transmission completed/Address matching address signal	ADDRFLG	
10-bit address head segment transmission completed	ADDR10FLG	
Received stop signal	STOPFLG	
Data byte transmission completed	BTCFLG	
Receive buffer not empty	RXBNEFLG	EVIEN and BUFIEN
Transmit buffer empty	TXBEFLG	
Bus error	BERRFLG	ERRIEN
Arbitration loss	ALFLG	
Answer failed	AEFLG	
Overrun/Underrun	OVRURFLG	
PEC error	PECEFLG	
Timeout or Tlow error	TTEFLG	
SMBus alert	ALERTEN	

20.6 Register Address Mapping

Table 62 I2C Register Address Mapping

Register name	Description	Offset address
I2C_CTRL1	Control register 1	0x00
I2C_CTRL2	Control register 2	0x04
I2C_SADDR1	Slave address register 1	0x08
I2C_SADDR2	Slave address register 2	0x0C
I2C_DATA	Data register	0x10
I2C_STS1	State register 1	0x14
I2C_STS2	State register 2	0x18
I2C_CLKCTRL	Master clock control register	0x1C
I2C_RISETMAX	Maximum rising time register	0x20
I2C_SWITCH	I2C Switch register	0x100

20.7 Register Functional Description

20.7.1 Control register 1 (I2C_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	I2CEN	R/W	I2C Enable 0: Disable 1: Enable
1	SMBEN	R/W	SMBus Mode Enable 0: I2C mode 1: SMBus mode
2	Reserved		
3	SMBTCFG	R/W	SMBus Type Configure 0: SMBus device 1: SMBus master
4	ARPEN	R/W	ARP Enable 0: Disable 1: Enable If SMBTCFG=0, use the default address of SMBus device If SMBTCFG=1, use the primary address of SMBus
5	PECEN	R/W	PEC Enable 0: Disable 1: Enable
6	SRBEN	R/W	Slave Responds Broadcast Enable 0: Disable 1: Enable Note: The broadcast address is 0x00
7	CLKSTRETCHD	R/W	Slave Mode Clock Stretching Disable 0: Enable 1: Disable In slave mode, enabling extending the low-level time of the clock can avoid overrun and underrun errors.
8	START	R/W	Start Bit Transfer This bit can be set to 1 and cleared by software; when transmitting the start bit or I2CEN=0, it is cleared by hardware. 0: Not transmit 1: transmit
9	STOP	R/W	Stop Bit Transfer This bit can be set to 1 or cleared by software; when sending the stop bit, it is cleared by hardware; when timeout error is detected, it is set to 1 by hardware. 0: Not send 1: Send
10	ACKEN	R/W	Acknowledge Transfer Enable

Field	Name	R/W	Description
			This bit can be set to 1 or cleared by software; when I2CEN=0, it is cleared by hardware. 0: Not send 1: Send
11	ACKPOS	R/W	Acknowledge /PEC Position Configure This bit can be set to 1 or cleared by software; when I2CEN=0, it is cleared by hardware. 0: When receiving current byte, whether sending NACK/ACK, whether PEC is in shift register 1: When receiving next byte, whether sending NACK/ACK and whether PEC is in the next byte of shift register
12	PEC	R/W	Packet Error Check Transfer Enable This bit can be set to 1 or cleared by software; when sending PEC, or sending the start bit and stop bit, or when I2CEN=0, it is cleared by hardware. 0: Disable 1: Enable
13	ALERTEN	R/W	SMBus Alert Enable This bit can be set to 1 or cleared by software; when I2CEN=0, it is cleared by software. 0: Release the SMBAlert pin to make it higher, and remind to send the response address header immediately after sending the NACK signal 1: Drive SMBAlert pin to make it lower, and remind to send the response address header immediately after sending the ACKEN signal
14	Reserved		
15	SWRST	R/W	Software Configure I2C under Reset State 0: Not reset 1: Reset; before I2C reset, ensure that I2C pin is released and the bus is in idle state.

20.7.2 Control register 2 (I2C_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
5:0	CLKFCFG	R/W	I2C Clock Frequency Configure The clock frequency is the clock of I2C module, namely, the clock input from APB bus. 0: Disable 1: Disable 2：2MHz ... 50：50MHz Greater than 100100: Disable. Minimum clock frequency of I2C bus: the standard mode is 1MHz, and the fast mode is 4MHz.

Field	Name	R/W	Description
7:6	Reserved		
8	ERRIEN	R/W	Error Interrupt Enable 0: Disable 1: When the position 1 of any of the following state register is enabled, the interrupt will be generated: SMBALTFLG, TTEFLG, PECEFLG, OVRURFLG, AEFLG, ALFLG, and STS1_BERRFLG
9	EVIEN	R/W	Event Interrupt Enable 0: Disable 1: When the position 1 of any of the following state registers is enabled, the interrupt will be generated: STARTFLG, ADDRFLG, ADDR10FLG, STOPFLG, BTCFLG, TXBEFLG is set to 1 and BUFIEN is set to 1, RXBNEFLG is set to 1 and BUFIEN is set to 1.
10	BUFIEN	R/W	Buffer Interrupt Enable 0: Disable 1: Enable; when the bit of any of the following state register is set to 1, the interrupt will be generated: TXBEFLG and RXBNEFLG
11	DMAEN	R/W	DMA Requests Enable 0: Disable 1: When TXBEFLG=1 or RXBNEFLG=1, enable DMA request
12	LTCFG	R/W	DMA Last Transfer Configure Configure whether the EOT of the next DMA is the last transmission received, and only used for the master receiving mode. 0: No 1: Yes
15:13	Reserved		

20.7.3 Slave mode address register 1 (I2C_SADDR1)

Offset address: 0x08

Reset value: 0x0000

Field	Name	R/W	Description
0	ADDR[0]	R/W	Slave Address Setup When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the 0 bit of the address.
7:1	ADDR[7:1]	R/W	Slave Address Setup Slave address 7:1 bit
9:8	ADDR[9:8]	R/W	Slave Address Setup When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the 9:8 bit of the address.
14:10	Reserved		
15	ADDRLEN	R/W	Slave Address Length Configure 0: 7-bit address mode 1: 10-bit address mode

20.7.4 Slave address register 2 (I2C_SADDR2)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	ADDRNUM	R/W	Slave Address Number Configure In the slave 7-bit address mode, it can be configured to identify the single-address mode and double-address mode; only ADDR1 is identified in single-address mode; both ADDR1 and ADDR2 can be identified in double-address mode Single or double address registers can be identified in 7-bit address mode, specifically as follows: 0: Identify one address (ADDR1) 1: Identify two addresses (ADDR1 and ADDR2)
7:1	ADDR2[7:1]	R/W	Slave Dual Address Mode Address Setup bit7:1 of the address in double-address mode
15:8	Reserved		

20.7.5 Data register (I2C_DATA)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
7:0	DATA	R/W	Data Register In I2C transmission mode, write the data to be transmitted to this register; in I2C receiving mode, read the received data from this register.
15:8	Reserved		

20.7.6 State register 1 (I2C_STS1)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	STARTFLG	R	Start Bit Sent Finished Flag 0: Not transmit 1: Transmitted When the start bit is transmitted, this bit can be set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then writes the DATA register; when I2CEN=0, it can be cleared by hardware.
1	ADDRFLG	R	Address Transfer Complete /Receive Match Flag Whether the matching address is received in slave mode: 0: Not received 1: Received Whether finishing sending the address in master mode: 0: Not completed 1: Completed The bit is set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then reads STS2 register; when I2CEN=0, it can be cleared by hardware.
2	BTCFLG	R	Byte Transfer Complete Flag 0: Not completed 1: Completed

Field	Name	R/W	Description
			When receiving data, if failing to read the data received in DATA register, and a new data is received then, set to 1 by hardwre; When sending data, if the DATA register is empty, to send the data in the shift register, set to 1 by hardware. This bit can be cleared after the software first reads STS1 register, and then reads or writes the DATA register; this bit can be cleared by hardware by sending a start bit or stop bit during the transmission, or when I2CEN=0.
3	ADDR10FLG	R	10-Bit Address Header Sent Flag 0: Not transmit 1: Transmitted The bit is set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then writes the DATA register; when I2CEN=0, it can be cleared by hardware.
4	STOPFLG	R	Stop Bit Detection Flag 0: Not detected 1: Detected If ACKEN=1, after one answer, when the slave detects the stop bit on the bus, it will be set to 1 by hardwre; This bit can be cleared after the software first reads STS1 register and then writes CTRL1 register; when I2CEN=0, it can be cleared by hardware.
5	Reserved		
6	RXBNEFLG	R	Receive Buffer Not Empty Flag 0: The receive buffer is empty 1: The receive buffer is not empty This bit can be set to 1 by hardware when there is data in DATA register; When BTCFLG is set to 1, since the data register is still full, the RXBNEFLG bit cannot be cleared by reading DATA register; This bit can be cleared after the software reads and writes DATA register; when I2CEN=0, it can be cleared by hardware.
7	TXBEFLG	R	Transmit Buffer Empty Flag 0: The transmit buffer is not empty 1: The transmit buffer is empty This bit can be set to 1 by hardware when the content of DATA register is empty; When the software writes the first data to the DATA register, it will immediately move the data to the shift register, then the data in the DATA register is empty and this bit cannot be cleared; This bit can be cleared after the software writes data to DATA register; after sending the start bit or stop bit, or when I2CEN=0, it can be cleared by hardware.
8	BERRFLG	RC_W0	Bus Error Flag 0: No bus error 1: Bus error occurred Bus error means exception of start bit or stop bit; when an error is detected, this bit can be set to 1 by hardware; this bit can be

Field	Name	R/W	Description
			cleared after the software writes 0; when I2CEN=0, it can be cleared by hardware.
9	ALFLG	RC_W0	Master Mode Arbitration Lost Flag 0: No arbitration loss 1: In case of arbitration loss, I2C interface will automatically switch back to slave mode "Arbitration loss in master mode" means the master loses the control of buses; this bit is set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it is cleared by hardware.
10	AEFLG	RC_W0	Acknowledge Error Flag 0: No acknowledgment error 1: Acknowledgment error occurred This bit can be set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it can be cleared by hardware.
11	OVRURFLG	RC_W0	Overrun/Underrun Flag 0: Not occur 1: Occurred This bit can be set to 1 by hardware when CLKSTRETCHD=1 and one of the following conditions is met: (1) In the slave receiving mode, when the data in the DATA register is not read out, but a new data is received (this data will be lost), overrun occurs; (2) In the slave transmission mode, no data is written in the data register but it still needs to send data (the same data is transmitted twice), and then underrun occurs. This bit can be cleared by writing 0 by software; or be cleared by hardware when I2CEN=0.
12	PECEFLG	RC_W0	PEC Error in Reception Flag 0: No PEC error: when ACKEN=1, after receiving PEC, the receiver will return ACKEN 1: There is PEC error; regardless of the value of ACKEN, as long as PEC is received, the receiver will return NACK This bit can be cleared by writing 0 by software; or be cleared by hardware when I2CEN=0.
13	Reserved		
14	TTEFLG	RC_W0	Timeout or Tlow error flag (Timeout or Tlow Error Flag) 0: No timeout error 1: When a timeout error occurs, in slave mode, the slave is reset and the bus is released; in master mode, the hardware sends the stop bit. This bit can be set to 1 by hardware when timeout error occurs in any of the following situations: (1) SCL maintains low level for more than 25ms; (2) SCL low-level extension time of the main device is more than 10ms; (3) SCL low-level extension time of the slave device is more than 25ms.

Field	Name	R/W	Description
			This bit can be cleared by writing 0 by software; or be cleared by hardware when I2CEN=0.
15	SMBALTFLG	RC_W0	SMBus Alert Occur Flag 0: SMBus master mode, without alarm; SMBus slave mode, without alarm, SMBAlert pin level unchanged 1: SMBus master mode, with an alarm generated on the pin; SMBus slave mode, receiving an alarm, causing SMBAlert pin level to become low This bit can be set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it can be cleared by hardware.

20.7.7 State register 2 (I2C_STS2)

Offset address: 0x18

Reset value: 0x0000

Field	Name	R/W	Description
0	MSFLG	R	Master Slave Mode Flag 0: Slave mode 1: Master mode This bit can be set to 1 by hardware when I2C is configured as master mode; This bit can be cleared by hardware when one of the following conditions is met: (1) Stop bit is generated (2) Bus arbitration is lost (3)I2CEN=0
1	BUSBSYFLG	R	Bus Busy Flag 0: The bus is idle (no communication) 1: The bus is busy (in the progress of communication) This bit can be set to 1 by hardware when SDA or SCL is at low level; cleared by hardware after the stop bit is generated.
2	TRFLG	R	Transmitter / Receiver Mode Flag 0: The device is in receiver mode (read) 1: The device is in transmitter mode (write) Decide the bit value according to R/W bit; This bit can be cleared by hardware when one of the following conditions is met: (1) Stop bit is generated (2) Repeated start bit is generated (3) Bus arbitration loss (4)I2CEN=0
3	Reserved		
4	GENCALLFLG	R	Slave Mode Received General Call Address Flag 0: Failed to receive the broadcast address 1: Received broadcast address This bit can be set to 1 by hardware; and be cleared by hardware when one of the following conditions is met:

Field	Name	R/W	Description
			(1) Stop bit is generated (2) Repeated start bit is generated (3)I2CEN=0
5	SMBDADDRFLG	R	SMBus Device Received Default Address Flag in Slave Mode 0: Failed to receive the default address 1: Received the default address when ARPEN=1 This bit can be set to 1 by hardware; and be cleared by hardware when one of the following conditions is met: (1) Stop bit is generated (2) Repeated start bit is generated (3)I2CEN=0
6	SMMHADDR	R	SMBus Device Received Master Header Flag in Slave Mode 0: Failed to receive the master head address 1: Received the master head address when SMBTSEL=1 and ARPEN=1 This bit can be set to 1 by hardware; and be cleared by hardware when one of the following conditions is met: (1) Stop bit is generated (2) Repeated start bit is generated (3)I2CEN=0
7	DUALADDRFLG	R	Slave Mode Received Dual Address Match Flag 0: The received address matches the content of ADDR1 register 1: The received address matches the content of ADDR2 register This bit can be set to 1 by hardware; and be cleared by hardware when one of the following conditions is met: (1) Stop bit is generated (2) Repeated start bit is generated (3)I2CEN=0
15:8	PECVALUE	R	Save Packet Error Checking Value When PECEN=1, the internal PEC value is saved in PECVALUE.

20.7.8 Master clock control register (I2C_CLKCTRL)

Offset address: 0x1C

Reset value: 0x0000

Field	Name	R/W	Description
11:0	CLKS [11:0]	R/W	Clock Setup in Fast/Standard Master Mode In I2C standard mode or SMBus mode: T_{high}=CLKS × T_{PCLK1} T_{low}=CLKS × T_{PCLK1} In I2C fast mode: When FDUTYCFG=0: T_{high}=CLKS×T_{PCLK1} T_{low}=2×CLKS× T_{PCLK1} When FDUTYCFG=1: T_{high}=9 × CLKS × T_{PCLK1} T_{low}=16 × CLKS × T_{PCLK1}

Field	Name	R/W	Description
13:12	Reserved		
14	FDUTYCFG	R/W	Fast Mode Duty Cycle Configure Here define the duty cycle=t_{low}/t_{high} 0: SCLK duty cycle is 2 1: SCLK duty cycle is 16/9
15	SPEEDCFG	R/W	Master Mode Speed Configure 0: Standard mode 1: Fast mode

20.7.9 Maximum rising time register (I2C_RISETMAX)

Offset address: 0x20

Reset value: 0x0002

Field	Name	R/W	Description
5:0	RISETMAX	R/W	Master Mode Maximum Rise Time in Fast/Standard Mode The time unit is T_{PCLK1}, and RISETMAX is the maximum rising time of SCL plus 1.
15:6	Reserved		

20.7.10 I2C switch register (I2C_SWITCH)

Offset address: 0x100

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SWITCH	R/W	I2C Switch 0: I2C uses I2C1/I2C2 1: I2C uses I2C3/I2C4
31:1	Reserved		

21 Serial Peripheral Interface/On-chip Audio Interface (SPI/I2S)

21.1 Full Name and Abbreviation Description of Terms

Table 63 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Most Significant Bit	MSB
Least Significant Bit	LSB
Master Out Slave In	MOSI
Master In Slave Out	MISO
Serial Clock	SCK
Serial Data	SD
Master Clock	MCK
Word Select	WS
Pulse-code Modulation	PCM
Inter-IC Sound	I2S
Transmit	TX
Receive	RX
Busy	BSY

21.2 Introduction

SPI interface can be configured to support SPI protocol and I2S audio protocol. It works in SPI mode by default, and the functions can be switched in I2S mode through software.

Serial peripheral interface (SPI) provides data transmitting and receiving functions based on SPI protocol, which allows chips to communicate with external devices in half duplex, full duplex, synchronous and serial modes, and can work in master or slave mode.

The on-chip audio interface (I2S) supports four audio standards: Philips I2S standard, MSB alignment standard, LSB alignment standard and PCM standard. It can work in master/slave mode of half-duplex communication.

21.3 Main Characteristics

21.3.1 Main Characteristics of SPI

（1） Master and slave operation with 3-wire full duplex synchronous transmission and receiving

（2） Simplex synchronous transmission can be realized by two wires (the third bidirectional data line can be included/not included)

（3） Select 8-bitt or 16-bit transmission frame format

（4） Support multiple master device mode

（5） Support special transmission and receiving mark and can trigger interrupt

（6） Have SPI bus busy state flag

（7） Fast communication in master/slave mode, up to 18MHz

（8） Clock polarity and phase are programmable

（9） Data sequence is programmable; select MSB or LSB first

（10） Interrupt can be triggered by master mode fault, overrun and CRC error flag

（11） Have DMA transmit and receive buffers

（12） Calculation, transmission and verification can be conducted through hardware CRC

21.3.2 Main Characteristics of I2S

（1） Have master/slave mode of simplex communication (only transmit/receive)

（2） Four audio standards
- I2S Philips standard
- MSB alignment standard
- LSB alignment standard
- PCM standard

（3） 16/24/32-bit data length can be selected

（4） 16-bit or 32-bit channel length

（5） Clock polarity is programmable

（6） 16-bit data register is used for transmitting and receiving

（7） MSB is always the first in the data direction

（8） Transmitting and receiving supports DMA function

21.4 SPI Functional Description

21.4.1 Description of SPI Signal Line

Table 64 SPI Signal Line Description

Pin name	Description
SCK	Master device: SPI clock outputs Slave device: SPI clock inputs
MISO	Master device: Input the pin and receive data Slave device: Output the pin and send data Data direction: From slave device to master device
MOSI	Master device: Output the pin and send data Slave device: Input the pin and receive data Data direction: From master device to slave device
NSS	Software NSS mode: NSS pin can be used for other purposes. NSS mode of master device hardware: NSS output, single master mode. NSS closed output: Operation of multiple master environments is allowed. NSS mode of slave device hardware: NSS signal is set to low level as chip selection signal of slave.

21.4.2 Phase and Polarity of Clock Signal

The clock polarity and clock phase are CPOL and CPHA bits of SPI_CTRL1 register.

Clock polarity CPOL means the level signal of SCK signal line when SPI is in idle state.

- When CPOL=0, SCK signal line is in idle state and at low level
- When CPOL=1, SCK signal line is in idle state and at high level

Clock phase CPHA means the sampling moment of data

- When CPHA=0, the signal on MOSI or MISO data line will be sampled by the "odd edge" on SCK clock line.
- When CPHA=1, the signal on MOSI or MISO data line will be sampled by the "even edge" on SCK clock line.

SPI can be divided into four modes according to the states of clock phase CPHA and clock polarity CPOL.

Table 65 Four Modes of SPI

SPI mode	CPHA	CPOL	Sampling moment	Idle SCK clock
0	0	0	Odd edge	Low level
1	0	1	Odd edge	High level

SPI mode	CPHA	CPOL	Sampling moment	Idle SCK clock
2	1	0	Even edge	Low level
3	1	1	Even edge	High level

21.4.3 Data Frame Format

Set MSB or LSB to be first by configuring LSBSEL bit in SPI_CTRL1 register. Select to transmit/receive in 8/16-bit data frame format by configuring DFLSEL bit in SPI_CTRL1 register.

21.4.4 NSS Mode

Software NSS mode: Select to enable or disable this mode by configuring SSEN bit of SPI_CTRL1 register, and the internal NSS signal level is driven by ISSEL bit of SPI_CTRL1 register.

Hardware NSS mode:

- Turn on NSS output: When SPI is in master mode, enable SSOEN bit, NSS pin will be pulled to low level and SPI will automatically enter the slave mode.
- Turn off NSS output: Operation is allowed in multiple master environments.

21.4.5 SPI Mode

21.4.5.1 SPI master mode

In master mode, generate serial clock on SCK pin

Master mode configuration

- Configure MSMSEL=1 in SPI_CTRL1 register
- Select the polarity and phase by configuring CPOL and CPHA bits in SPI_CTRL1 register.
- Select 8/16-bit data frame format by configuring DFLSEL bit in SPI_CTRL1 register
- Select LSB or MSB first by configuring LSBSEL in SPI_CTRL1 register
- NSS configuration:
  - NSS pin works in input mode: in hardware mode, it is required to connect NSS pin to high level during the entire data frame transmission; in software mode, it is required to set SSEN bit and ISSEL bit in SPI_CTRL1 register
  - NSS works in output mode and it is required to configure SSOEN bit of SPI_CTRL2 register
- Enable SPI by configuring SPIEN bit in SPI_CTRL1 register

In master mode: MOSI pin is data output, which MISO is data input

21.4.5.2 SPI slave mode

In slave mode, SCK pin receives the serial clock transmitted from the master device

Configuration of slave mode

- Configure MSMSEL=0 in SPI_CTRL1 register
- Select the polarity and phase by configuring CPOL and CPHA bits in SPI_CTRL1 register.
- Select 8/16-bit data frame format by configuring DFLSEL bit in SPI_CTRL1 register
- Select LSB or MSB first by configuring LSBSEL in SPI_CTRL1 register
- NSS configuration:
  - In hardware mode: NSS pin must be at low level in the whole data frame transmission process
  - In software mode: Set SSEN bit in SPI_CTRL1 register and clear ISSEL bit
- Enable SPI by configuring SPIEN bit in SPI_CTRL1 register

In slave mode: MOSI pin is data input, which MISO is data output

21.4.5.3 Half-duplex communication of SPI

One clock line and one bidirectional data line

- Enable this mode by setting BMEN of SPI_CTRL1 register
- Control the data line to be input or output by setting BMOEN bit of SPI_CTRL1 register
- SCK pin is used as clock, MOSI pin is used in master device to transmit data, and MISO pin is used in slave device to transmit data

21.4.5.4 Simplex communication of SPI

One clock line and one unidirectional data line

In this mode, SPI module can only receive or only transmit

Send-only mode:

- Data are transmitted on send pin (MOSI in master mode, MISO in slave mode)
- Then the receive pin can be used as general I/O (MISO in master mode, MOSI in slave mode).

Receive-only mode:

- In master mode, enable SPI to initiate communication, clear SPEN bit of SPI_CTRL1 register, and it will stop receiving data immediately, not needing to read BSYFLG flag (always 1).
- Slave mode: When NSS is pulled to low level, SPI will receive all the time as long as SCK has clock pulse.

In receive-only mode, SPI output can be disabled by setting RXOMEN bit in SPI_CTRL1 register. At this time, release the transmit pin (MOSI in master mode, MISO in slave mode), which can be used for other functions.

21.4.6 Data Sending and Receiving Process in Different SPI Modes

Table 66 Run Mode of SPI

Mode	Configure	Data pin
Full duplex mode of master device	BMEN=0, RXOMEN=0	MOSI sends; MISO receives
Unidirectional receiving mode of master device	BMEN=0, RXOMEN=1	MOSI is not used; MISO receives
Bidirectional sending mode of master device	BMEN=1, BMOEN=1	MOSI sends; MISO is not used
Bidirectional receiving mode of master device	BMEN=1, BMOEN=0	MOSI is not used; MISO receives
Full duplex mode of slave device	BMEN=0, RXOMEN=0	MOSI receives, and MISO transmits
Unidirectional receiving mode of slave device	BMEN=0, RXOMEN=1	MOSI receives, while MISO is not used
Bidirectional sending mode of slave device	BMEN=1, BMOEN=1	MOSI is not used, and MISO transmits
Bidirectional receiving mode of slave device	BMEN=1, BMOEN=0	MOSI receives, while MISO is not used

Figure 83 Connection in Full Duplex Mode

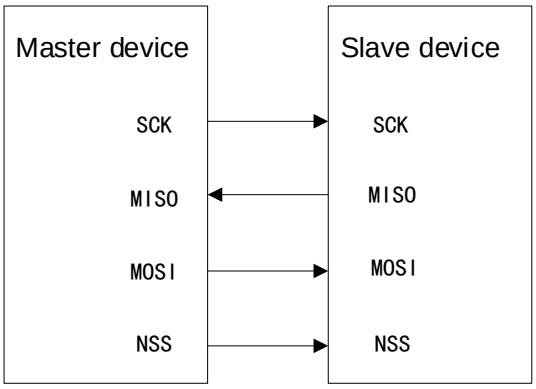


Figure 84 Connection in Simplex Mode (the master is used for receiving, while the slave is used for sending)

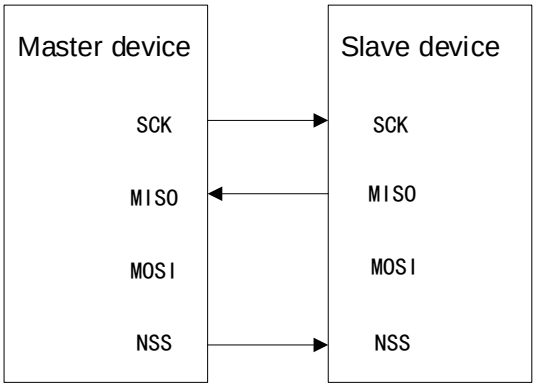


Figure 85 Connection in Simplex Mode (the master only sends, while the slave receives)

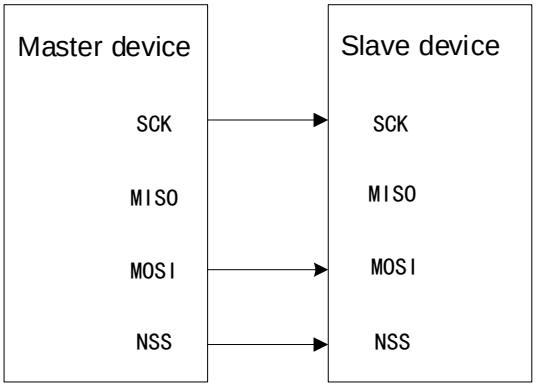
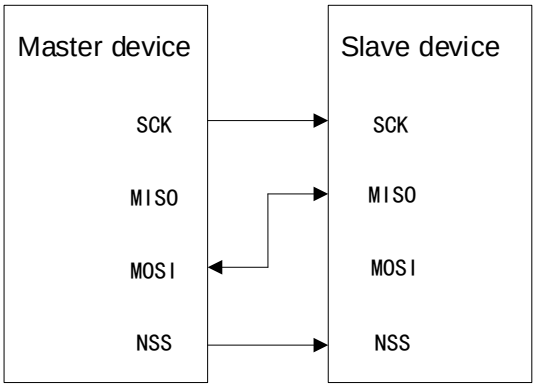


Figure 86 Bidirectional Line Connection



21.4.6.1 Transmitting and receiving of processed data

Data transmission

After the mode configuration is completed, the SPI module is enabled to remain idle.

Master mode: The software writes a data frame to the transmit buffer, and the transmission process starts

Slave mode: The SCK signal on the SCK pin starts to jump, while the NSS pin level is low, and the transmission process starts (before starting data transmission, make sure that the data has been written to the transmit buffer in advance).

When SPI is transmitting a data frame, it will load the data frame from the data buffer to the shift register, and then start to transmit data. After one bit of data frame is transmit, TXBEFLG is set to 1. If you need to continue to transmit data, the software needs to wait until TXBEFLG=1 writes data to the SPI_DATA register. (TXBEFLG flag is set to 1 by hardware and cleared by software).

Data receiving

BSYFLG flag is always set to 1 in the data transmission process.

At the last edge of the sampling clock, the received data is transferred from the shift register to the receive buffer; set the RXBNEFLG flag, and the software reads the data in data register (SPI_DATA) to obtain the content of the receive buffer; if RXBNEIEN bit of SPI_CTRL2 register is set, an interrupt will be generated, and after data is read, the BSYFLG flag will be automatically cleared.

21.4.6.2 Full duplex transmitting and receiving mode in master/slave device

Full duplex mode in master device

- After writing data to SPI_ DATA register (transmit buffer), data transmission starts.
- When SPI transmits the first bit of data, the data is transferred from the transmit buffer to the shift register and then transferred to the MOSI pin serially according to the sequence.
- The data received on MISO pin is serially transferred to SPI_DATA register (receive buffer) according to the sequence.

Transmitting and receiving are synchronous.

Full duplex mode under slave device

- When the slave device receives the clock signal and the first data bit appears on the MOSI pin, data transmission starts, and the subsequent data bits will be transferred to the shift register in turn.
- When SPI sends the first bit of data, the data is transferred from the transmit buffer to the shift register, and then transferred to the MISO pin serially according to the sequence.
- The software must ensure that the data to be transmit is written before the SPI master device starts to transmit data.

Sending and receiving are synchronous

Full duplex transmitting and receiving process under master/slave device

（1） Enable SPI module: Configure SPIEN=1 of SPI_CTRL1 register.

（2） Write the first data to be transmit to SPI_DATA register, and the TXBEFLG flag will be cleared.

（3） Wait until TXBEFLG flag bit is set to 1 (control by hardware), and write the second data bit to be transmit.

（4） Wait until RXBNEFLG flag bit is set to 1 (control by hardware), read the first received data in the SPI_DATA register, at the same time, clear the RXBNEFLG flag (cleared by software). Repeat the operation, and send and receive data at the same time.

（5） Wait until RXBNEFLG=1 and receive the last data.

（6） Wait until TXBEFLG=1 and disable SPI module after BSYFLG=0.

21.4.6.3 Bidirectional sending mode of master/slave device

Bidirectional transmission of master device

- Write data to SPI_ DATA register, and the transmission starts
- The data in the transmit buffer is transferred to the shift register in parallel, and then transferred to the MOSI pin serially according to the sequence.

Bidirectional transmission of slave device

- When the slave device receives the clock signal and the first data bit appears on the MISO pin, data transmission starts.
- At the same time, the data to be transmit by the transmit buffer is transferred to the shift register in parallel, and then transmit to the MISO pin in serial (before data transmission, make sure that the data has been written to the transmit buffer in advance).

Bidirectional transmission process of master/slave device

（1） Enable SPI module: Configure SPIEN=1 of SPI_CTRL1 register.

（2） Write the first data to be transmit to SPI_DATA register, and the TXBEFLG flag will be cleared.

（3） Wait until TXBEFLG=1, write the second data, repeat the operation and send the subsequent data

（4） After writing the last data, wait for TXBEFLG=1 and BSYFLG=0 and transmission is completed

21.4.6.4 One-way/Two-way receiving mode under master/slave device

（1） Enable SPI module: Configure SPIEN=1 of SPI_CTRL1 register.

（2） In the master device: Generate SCK clock immediately, and continuously receive data before SPI is disabled.

（3） Slave device: When SPI master device pulls down NSS and generates clock, receive data.

（4） Wait until the RXBNEFLG flag is set to 1, read data through SPI_DATA, and repeat the operation to receive data.

21.4.7 CRC Functions

SPI module contains two CRC computing units, which are used for data receiving and data transmission respectively.

CRC computing unit is used to define polynomials in SPI_CRCPOLY register.

Enable CRC computing by configuring CRCEN bit in SPI_CTRL1 register; at the same time, reset the CRC register (SPI_RXCRC and SPI_TXCRC).

To obtain the CRC value of transmission calculation, after the last data is written to the transmit buffer, it is required to set CRCNXT bit of SPI_CTRL1; indicate that the hardware sends the CRC value after the last data is transmit, and the CRCNXT bit will be cleared; at the same time, compare the values of CRC and SPI_RXCRC, and if they do not match, it is required to set CRCEFLG bit of SPI_STS register, and after ERRIEN bit of SPI_CTRL2 regiser is set, an interrupt will occur.

Note:

(1) If SPI is under slave device and CRC function is used, CRC computing will continue when NSS pin is at high level. For example, when the master device communicates with multiple slave devices alternately, the above situation will occur, so it is necessary to avoid faulty operation of CRC.

(2) In the process of a slave device from being unselected (NSS is at high level) to being selected (NSS is at low level 0), it is required to clear the CRC value at both ends of the master and slave devices to keep the next CRC computing results of the master and slave devices synchronized.

(3) When SPI is in slave mode, CRC computing can be enabled after the clock is stable.

(4) When the SPI clock frequency is too high, the CPU operation will affect the SPI bandwidth. It is recommended to use DMA mode to avoid the reduction of SPI speed.

(5) When the SPI clock frequency is too high, during the CRC transmission period, the CPU utilization frequency is reduced, and the function call is disabled in the CRC transmission process to avoid errors when receiving the last data and CRC.

(6) When NSS hardware mode is used in slave mode, NSS pin should be kept low during data transmission and CRC transmission period.

Sequence of clearing CRC values

（1） SPI Disabled (SPIEN=0)

（2） Clear CRCEN bit

（3） Set CRCEN bit to 1

（4） Enable SPI (SPIEN=1)

21.4.8 DMA Function

For high-speed data transmission, the request/response DMA mechanism in SPI improves the system efficiency and can transfer data to SPI transmit buffer promptly, and the receive buffer can read the data in time to prevent overflow.

When SPI only sends data, it is only needed to enable DMA transmission channel; when SPI only receives data, it is only needed to enable DMA receiving channel.

DMA function of SPI mode can be enabled by configuring TXDEN and RXDEN bits of SPI_CTRL2 register.

- When sending: When TXBEFLG flag bit is set to 1, issue the DMA request, DMA controller writes data to SPI_DATA register, and then the TXBEFLG flag bit will be cleared.
- When receiving: When setting RXBNEFLG flag bit to 1, issue the DMA request, DMA controller reads data from SPI_DATA register, and then RXBNEFLG flag bit is cleared.

By monitoring BSYFLG flag bit, confirm whether SPI communication is over after DMA has transferred all data to be transmit in sending mode, which can avoid damaging the transmission of last data.

DMA function with CRC

By the end of communication, if SPI enables both CRC operation and DMA function, sending and receiving of CRC bytes will be completed automatically.

At the end of data and CRC transmission, if CRCEFLG flag bit of SPI_STS register is set to 1, it indicates that an error occurred during transmission.

21.4.9 SPI Disable

After data transmission is over, end the communication by closing SPI module. In some configurations, if SPI is disabled before data transmission is completed, data transmission error may be caused. Different methods are required in different operation modes to disable SPI

Full duplex mode under master/slave device

（1） Wait until RXBNEFLG flag bit is set to 1, and receive the last data

（2） Wait until TXBEFLG flag bit is set to 1

（3） Wait for clearing BSYFLG flag bit

（4） Disable SPI (set SPIEN=0 of SPI_CTRL1 register)

One-way/Two-way receive-only mode under master/slave device

（1） Wait No. n-1 RXBNEFLG flag bit is set to 1

（2） Wait for one SPI clock cycle before SPI is disabled (set SPIEN=0 of SPI_CTRL1 register)

（3） Before entering the stop mode, wait until the last RXBNEFLG flag bit is set to 1

Receive-only/Two-way receiving mode in slave mode

SPI can be disabled at any time (set SPIEN=0 of SPI_CTRL1 register) and it will be disabled when the transmission is over. If you want to enter the stop mode, wait until BSYFLG flag bit is cleared.

21.4.10 SPI Interrupt

21.4.10.1 State flag bit

There are three flag bits for fully monitoring the state of SPI bus

Transmit buffer empty flag TXBEFLG

TXBEFLG=1 indicates that the transmit buffer bit is empty, and the next data to be transmit can be written. When the data is written to SPI_DATA register, clear the TXBEFLG flag bit.

Receive buffer non-empty flag RXBNEFLG

RXBNEFLG=1 indicates that the receive buffer contains valid data and the data can be read through SPI_DATA register; then clear the RXBNEFLG flag

Busy flag BSYFLG

BSYFLG flag is set and cleared by hardware, which can indicate the state of SPI communication layer. When BSYFLG=1, it indicates SPI is communicating, but in the two-line receiving mode under the master device, BSYFLG=0 during the period of receiving of data.

BSYFLG flag can be used to detect whether transmission is over to avoid damaging the last transmit data.

BSYFLG flag bit can be used to avoid conflict when writing data in multi-master mode.

BSYFLG flag will be cleared when the transmission ends (except for continuous

communication in master mode), SPI is disabled and the master mode fails.

BSYFLG=0 between data item and data item when communication is discontinuous.

When communication is continuous:

- In master mode: BSYFLG=1 in the whole transmission process
- In slave mode: BSYFLG is kept low within one SCK clock cycle between transmission of each data

Note: It is best to use TXBEFLG and RXBNEFLG flags to process the transmitting and receiving of each data item.

21.4.10.2 Error flag bit

Master mode error MEFLG

MEFLG is an error flag bit. The master mode error occurs when: in hardware NSS mode, the NSS pin of the master device is pulled down; in software NSS mode, ISSEL bit is cleared; MEFLG bit is set automatically.

Influence of master mode failure: MEFLG is set to 1, and SPI interrupt is generated when ERRIEN is set; SPIEN is cleared (output stops, SPI interface is disabled); MSMSEL is cleared and the device is forced into the slave mode.

Operation of clearing the MEFLG flag bit: When MEFLG flag bit is set to 1, it is required to read or write SPI_STS register, and then write to SPI_CTRL1 register.

When the MEFLG flag bit is 1, it is not allowed to set the SPIEN and MSMSEL bits

Overrun error OVRFLG

Overrun error: After the master device sends the data, the RXBNEFLG flag bit is still 1, which indicates that the overrun error occurred. Then OVRFLG bit is set to 1, and if the ERRIEN bit is also set, an interrupt will be generated.

After an overrun error occurs, the data in the receive buffer is not the data transmit by the master device, and then the read data in SPI_DATA register is the data not read before, while the data transmit later will not be read.

OVRFLG flag can be cleared by reading SPI_DATA register and SPI_STS register according to the sequence.

CRC error flag CRCEFLG

By setting CRCEN bit of SPI_CTRL1 register, start CRC computing, CRC error flag, and check whether the received data is valid.

When the value transmits by SPI_TXCRC register does not match the value in

SPI_RXCRC register, a CRC error will be generated, and CRCEFLG flag bit in SPI_STS register will be set to 1.

CRCEFLG can be cleared by writing 0 to CRCEFLG bit of SPI_STS register.

Table 80 SPI Interrupt Request

Interrupt flag	Interrupt event	Enable control bit	Clearing method
TXBEFLG	Transmit buffer empty flag	TXBEIEN	Write SPI_DATA register
RXBNEFLG	Receive buffer non-empty flag	RXBNEIEN	Read SPI_DATA register
MEFLG	Master mode failure event flag	ERRIEN	Read/Write SPI_STS register, and then write SPI_CTRL1 register
OVRFLG	Overrun error flag		Read SPI_DATA register, and then read SPI_STS register
CRCEFLG	CRC error flag		Write 0 to CRCEFLG bit

21.5 I2S Functional Description

Enable I2S function by setting I2SMOD bit of SPI_I2SCFG.

I2S and SPI share three pins:

- SD: Serial data, sending and receiving the data of 2-way time division multiplexing channel
- WS: Chip selection, switching the data of left and right channels
- CK: Serial clock; the clock signal is output in master mode, and is input in slave mode
- MCK: Master clock; in master mode, when MCOEN bit of SPI_I2SPSC register is set to 1, it can be used as the pin for outputting the extra clock signal.

21.5.1 I2S Audio Standard

I2S audio standard is selected by setting I2SSSEL bit and PFSSEL bit of SPI_I2SCFG register, and four audio standards can be selected: I2S Philips standard, MSB alignment standard, LSB alignment standard and PCM standard. Except PCM standard, other audio standards have two channels: left and right channels.

The data length and channel length can be configured by DATALEN and CHLEN bits in SPI_I2SCFG register. The channel length must be greater than or equal to the data length. There are four data formats to send data: 16-bit data packed into 16-bit frame, 16-bit data packed into 32-bit frame, 24-bit data packed into 32-bit frame, and 32-bit data packed into 32-bit frame.

When the 16-bit data is extended to 32 bits, the first 16 bits are valid data, and the last 16 bits are forced to be 0. No external intervention is needed in this process.

Since the data buffers used for sending and receiving are all 16 bits, SPI_DATA needs to read/write twice when 24-bit and 32-bit data are transmitted. If DMA is used, it needs to be transmit twice.

For all communication standards and data formats, the most significant bit of data is always transmitted first.

For time division multiplexing, the left channel is always transmitted first, and then the right channel is transmitted.

21.5.1.1 I2S Philips standard

In I2S Philips standard, the pin WS can indicate the data being transmitted comes from the left channel or the right channel.

In I2S Philips standard, both WS and SD change on the falling edge of CK clock signal.

The sender will change the data on the falling edge of the clock signal CK, while the receiver will change the data on the rising edge of the clock signal CK.

Figure 87 I2S Philips Protocol Waveform (16/32 bits)

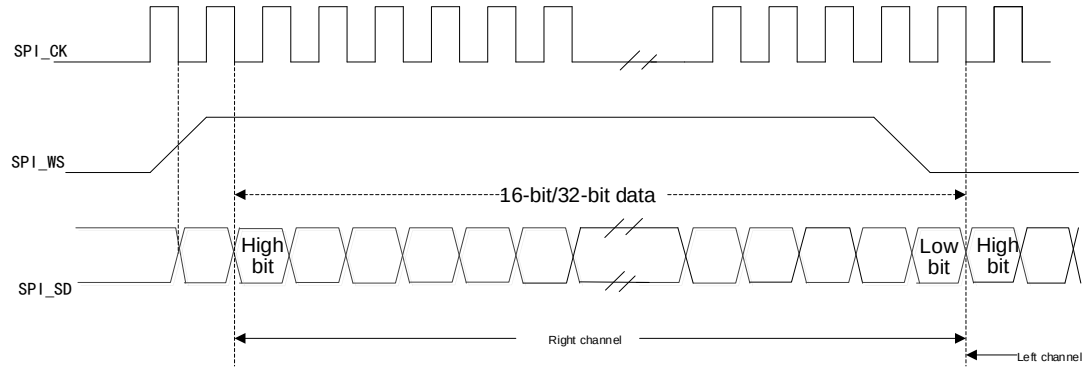
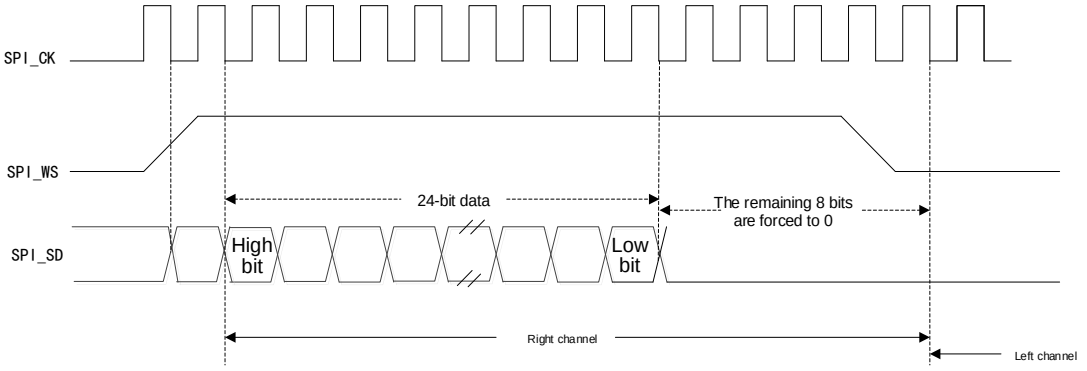


Figure 88 I2S Philips Protocol Waveform (24 bits)



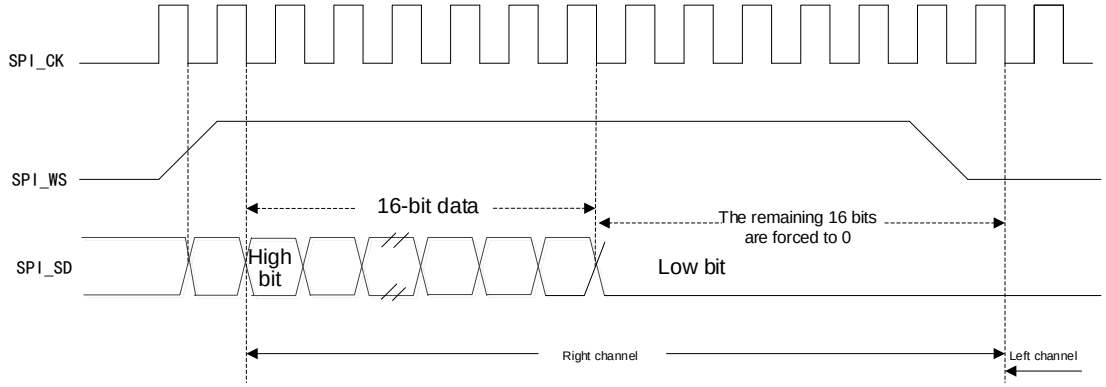
In I2S Philips standard, if you want to send/receive 24-bit and 32-bit data, the SPI_DATA register needs to read/write twice; for example:

- If you need to send 0x9FBB88 (24-bit data), write 0x9FBB to SPI_DATA register for the first time, and write 0x88XX to the register for the second time.
- If you need to receive 0x9FBB88 (24-bit data), read out 0x9FBB from SPI_DATA register for the first time and read out 0x8800 from the register for the second time.

In I2S configuration, when selecting the frame format of extending from 16-bit data to 32-bit data frame, it is required to access SPI_DATA register, and the remaining 16-bit data will be set to 0x0000 by hardware by forece; for example:

- The data to be received or transmit is 0x62D8, which becomes 0x62D80000 after it is expanded to 32 bits, and it is necessary to write 0x62D8 to SPI_DATA register or read out from SPI_DATA register.

Figure 89 I2S Philips Protocol Waveform (extending from 16 bits to 32 bits)



In the transmission process, the MSB should be written to the register SPI_DATA, and when TXBEFLG flag bit is set to 1, new data can be written; if there is corresponding interrupt, an interrupt can be generated.

In the receiving process, every time the MSB is received, the RXBNEFLG flag bit will be set to 1; if there is corresponding interrupt, an interrupt can be generated.

21.5.1.2 MSB alignment standard

In MSB standard, WS signal and the first data bit are generated at the same time

In the transmission process, the data is changed on the falling edge of the clock signal; in the receiving process, the data is read on the rising edge of the clock signal.

Figure 90 MSB Alignment Standard Waveform (16/32-bit data)

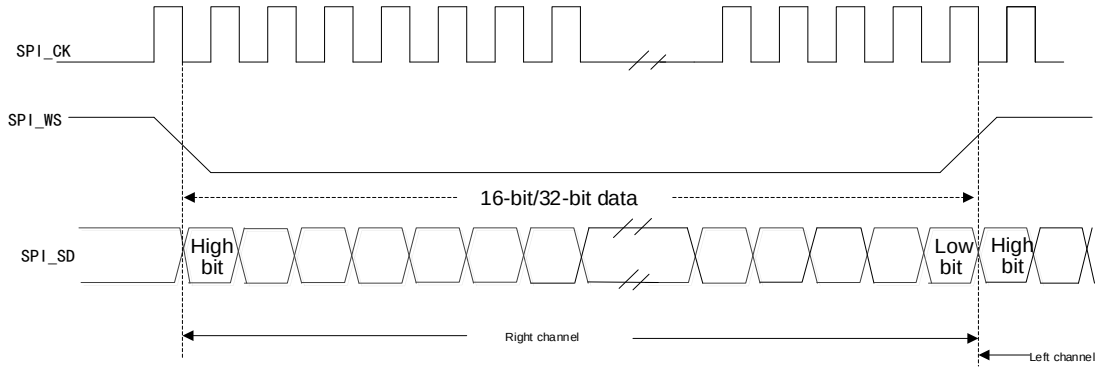


Figure 91 MSB Alignment Standard Waveform (24-bit data)

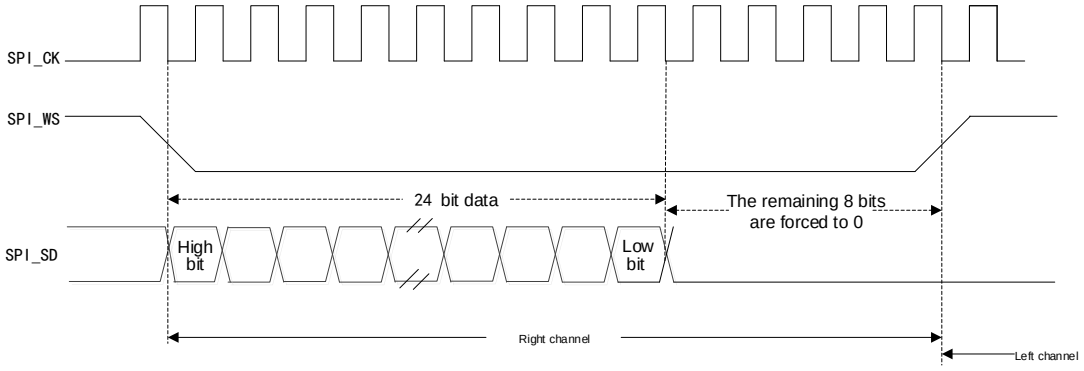
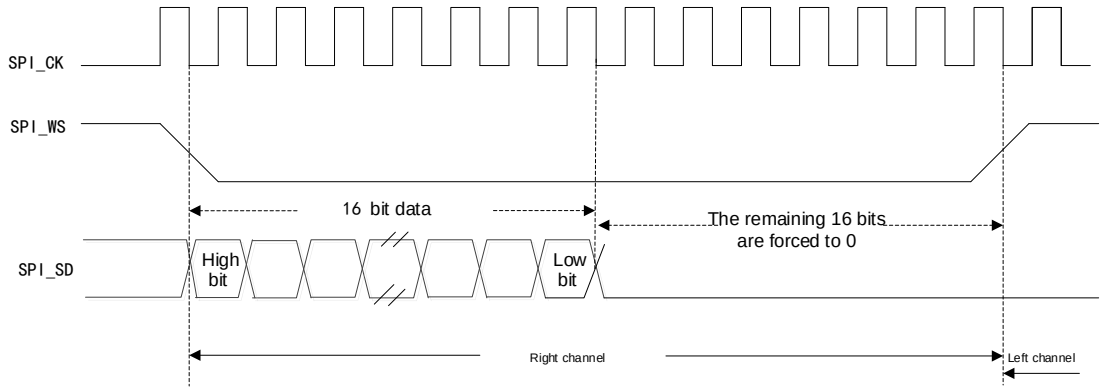


Figure 92 MSB Alignment Standard Waveform (extending from 16 bits to 32 bits)



21.5.1.3 LSB alignment standard

In the transmission process of LSB alignment standard, the data is changed on the falling edge of the clock signal; in the receiving process, the data is read on the rising edge of the clock signal. When the channel length is the same as the data length, the LSB alignment standard is the same as the MSB alignment standard. If the channel length is larger than the data length, the valid data of the LSB alignment standard is aligned with the lowest bit.

Figure 93 LSB Alignment Standard Waveform (16/32-bit data)

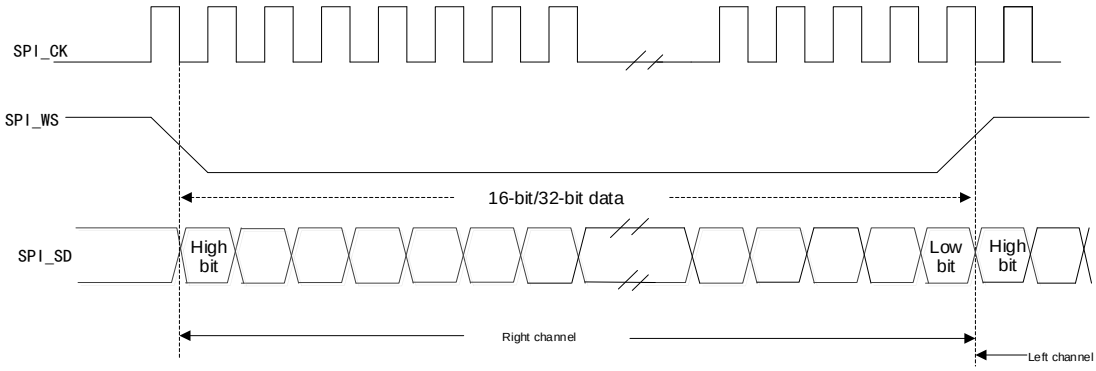
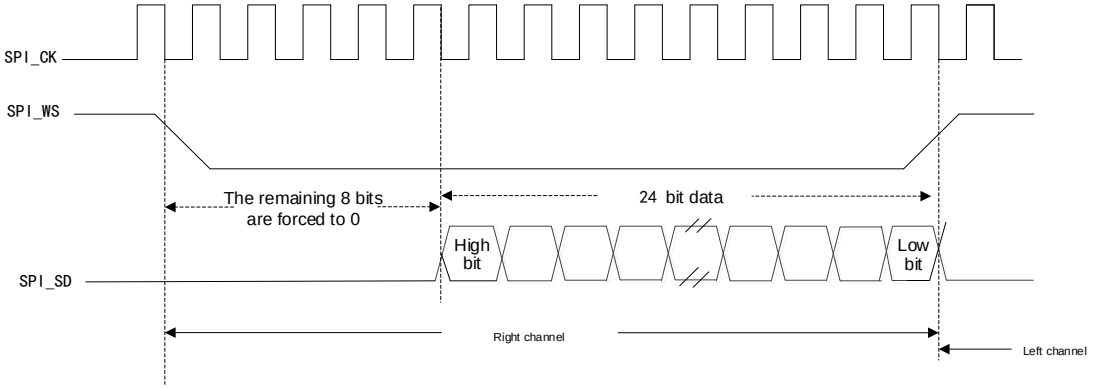


Figure 94 LSB Alignment Standard Waveform (24-bit data)



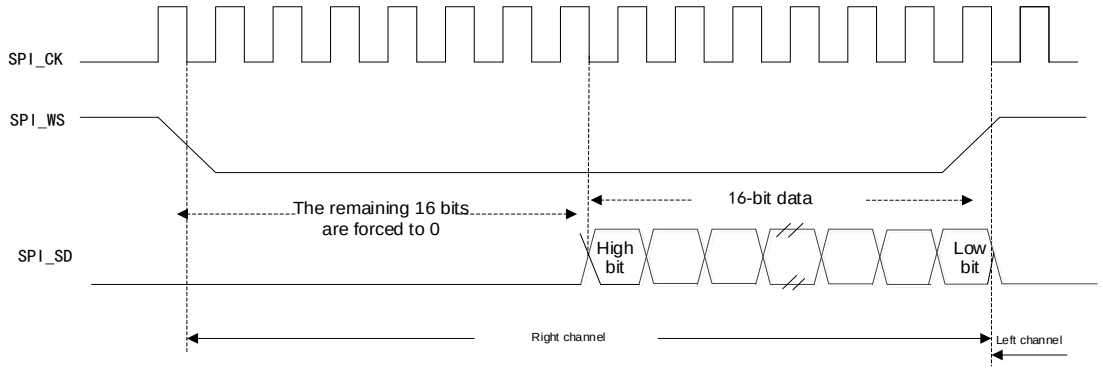
In the transmission process, if you want to send/receive 24-bit data, it is required to read/write the SPI_DATA register twice; for example:

- When you need to send 0x56EA98, write 0xXX56 to SPI_DATA register for the first time, and write 0xEA98 to SPI_DATA for the second time.
- When you need to receive 0x56EA98, read out 0x0056 from SPI_DATA registr for the first time, ad read out 0xEA98 from SPI_DATA register for the second time.

In I2S configuration, when selecting the frame format of extending from 16-bit data to 32-bit data frame, it is required to access SPI_DATA register, and the high 16-bit data will be set to 0x0000 by hardware by forece; for example:

- The data to be received or transmit is 0x98A5, which becomes 0x000098A5 after it is expanded to 32 bits, and it is necessary to write 0x98A5 to SPI_DATA register or read out from SPI_DATA register.

Figure 95 Under LSB Alignment Standard (extending from 16 bits to 32 bits)

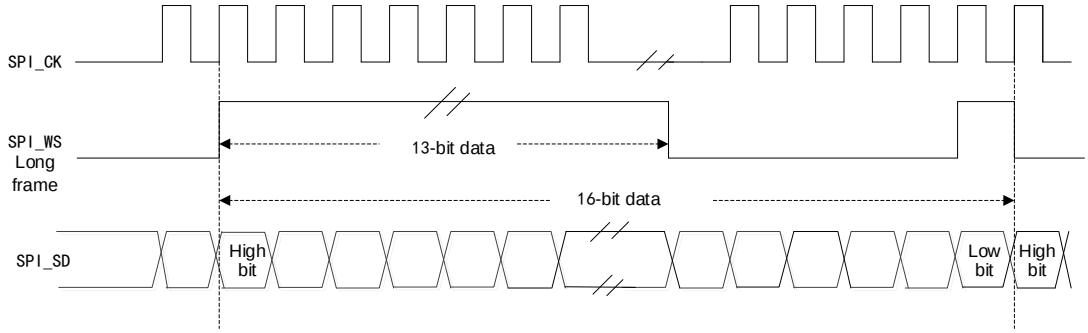


21.5.1.4 PCM standard

There is no sound channel selection in PCM standard. Short frame and long frame of PCM standard are selected by configuring PFSSEL bit in SPI_I2SCFG register.

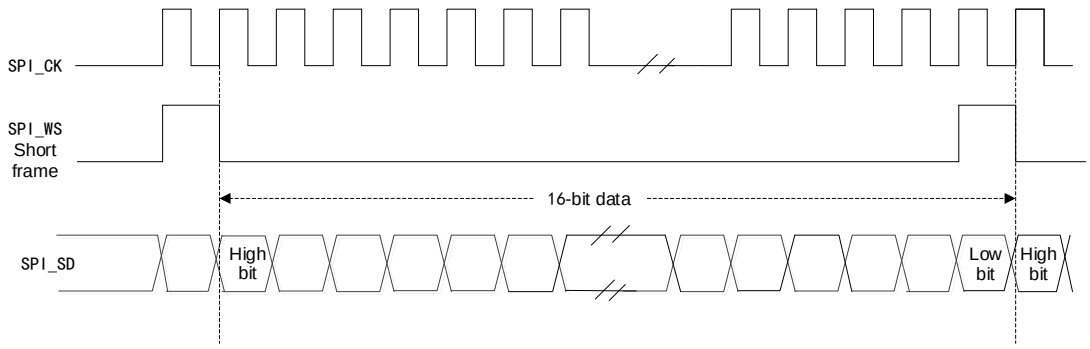
In the master mode, the valid time of synchronous WS signal of the long frame structure is 13 bits.

Figure 96 PCM Standard Waveform



In the master mode, the length of the synchronous WS signal of the short frame structure is 1 bit.

Figure 97 PCM Standard Waveform



21.5.2 I2S Clock

The clock source of I2SxCLK is system clock (HSICLK, HSECLK or PLL of AHB clock)

The bit rate of I2S determines the data stream on I2S data line and the clock signal frequency of I2S.

- I2S bit rate = the number of bits per channel × the number of sound channels × audio sampling frequency
- There are two channels of 16 bit audio signal: I2S bit rate=16×2×Fs

The relationship between audio sampling frequency (Fs) and I2S bit rate (I2S) is defined by the following formula:

Table 67 Audio Sampling Frequency (Fs) Formula

MCOEN	CHLEN	Audio sampling frequency (Fs)
1	0	I2SxCLK/[（16*2）*（(2*I2SPSC）+ODDPSC）*8]
1	1	I2SxCLK/[（32*2）*（(2*I2SPSC）+ODDPSC）*4]
0	0	I2SxCLK/[（16*2）*（(2*I2SPSC）+ODDPSC）]
0	1	I2SxCLK/[（32*2）*（(2*I2SPSC）+ODDPSC）]

21.5.3 I2S Mode

Table 68 I2S Run Mode

Run mode	SD	WS	CK	MCK
Master transmitting	Output	Output	Output	Output/Not used
Master receiving	Input	Output	Output	Output/Not used
Slave transmitting	Output	Input	Input	Output/Not used
Slave receiving	Input	Input	Input	Output/Not used

21.5.3.1 I2S master mode configuration process

（1） Configure I2SPSC bit and ODDPSC bit of SPI_I2SPSC register to define the baud rate of serial clock and the actual frequency division factor corresponding to the audio sampling frequency.

（2） Configure CPOL bit of SPI_I2SCFG register to define the clock polarity of SPI in idle state.

（3） Configure I2SMOD bit of SPI_I2SCFG register to activate I2S function and configure I2SMOD and PFSSEL bits of SPI_I2SCFG register to select I2S standard; configure DATALEN bit of SPI_I2SCFG register to select the data bits of the sound channel, and configure I2SMOD bit to select I2S master mode as transmitting terminal/receiving terminal.

（4） Configure SPI_CTRL2 register to select to enable the interrupt and DMA function or not (select required or not).

（5） Configure WS pin and CK pin to output mode; when MCOEN bit of SPI_I2SPSC is set to 1, the MCK pin should also be configured to output mode.

（6） Set the running mode of I2S by configuring the I2SMOD bit of SPI_I2SCFG.

（7） Set I2SEN bit of SPI_I2SCFG register to 1.

21.5.3.2 I2S master mode transmission process

When the data is written to the transmit buffer, the transmission will start, and the data will be transferred from the transmit buffer to the shift register, the TXBEFLG flag position is set to 1, and the SCHDIR flag bit indicates the corresponding sound channel of the currently transmit data. And the value of SCHDIR flag bit will be updated when TXBEFLG flag bit is 1.

When sending the first bit of data, 16-bit data will be transferred to the 16-bit shift register in parallel, and then transmit from the pin MISO/SD in serial. The next data needs to be written to SPI_DATA register when TXBEFLG flag bit is 1. If TXBEIEN bit of SPI_CTRL2 is 1, an interrupt will be generated.

Before the completion of the current data transmission, write the next data to be transmit to ensure continuous transmission of audio data.

When I2S is disabled, I2SEN can be cleared only when the flag bit TXBEFLG is 1 and BSYFLG is 0.

21.5.3.3 I2S master mode receiving process

RXBNEFLG flag is used to control the receiving sequence. RXBNEFLG flag indicates whether the receive buffer is empty; when the receive buffer is full, the RXBNEFLG flag bit will be set to 1. If RXBNEIEN bit ofSPI_CTRL2 is configured, an interrupt will occur and after the user reads out the data from SPI_DATA register, the RXBNEFLG flag bit will be cleared. Make sure to receive new data after reading operation; otherwise, overrun will occur and the OVRFLG flag bit will be set to 1.

The value of SCHDIR should be updated immediately after receiving data, and it depends on the WS signal generated by I2S.

Regardless of the data type and the channel length, the audio data is always received in the form of 16 bits. According to the configured data and the length of the channel, the data needs to be transmit to the receive buffer once or twice.

Turn off the I2S function, and for different audio protocols, the data length and channel length operation steps are as follows:

The data length is 16 bits, and 32-bit channel length (DATALEN=00, CHLEN=1, I2SSSEL=10) in LSB alignment mode

- Wait until the penultimate RXBNEFLG is set to 1
- Wail for 17 I2S clock cycles (software delay)

- I2SEN flag bit is cleared

The data length is 16 bits, and 32-bit channel length (DATALEN=00, CHLEN=1, I2SSSEL=10) in MSB alignment mode

- Wait until the last RXBNEFLG is set to 1
- Wail for one I2S clock cycle (software delay)
- I2SEN flag bit is cleared

All the other situations

- Wait until the penultimate RXBNEFLG is set to 1
- Wail for one I2S clock cycle (software delay)
- I2SEN flag bit is cleared

BSYFLG flag clock is low during data transmission

21.5.3.4 I2S slave mode configuration process

The configuration method of slave mode is basically the same as that of master mode. In slave mode, the clock signal and WS signal are provided by external I2S device instead of I2S.

（1） Configure I2SMOD bit of SPI_I2SCFG register to activate I2S function.

（2） Configure I2SSSEL bit of SPI_I2SCFG register to select the I2S standard; configure DATALEN[1:0] bit of SPI_I2SCFG register to select the bits of data; configure CHLEN bit of SPI_I2SCFG register to select the data bits per channel; configure I2SMOD bit of SPI_I2SCFG register to select I2S slave mode as transmitting terminal/receiving terminal.

（3） Configure SPI_CTRL2 register to select to enable the interrupt and DMA function or not (select required or not).

（4） Set I2SEN bit of SPI_I2SCFG register to 1.

21.5.3.5 I2S slave mode transmission process

Enable the slave device, write the data to the I2S data register, the external master device will start to communicate, and the external master device will send the clock signal, and when the data transmission starts, the sending process will begin.

When the first bit data is transmit, the 16-bit data will be transferred to the 16-bit shift register in parallel, and then transmit from the pin MOSI/SD in series. When the data is transferred from the data register to the shift register, the TXBEFLG flag bit is set to 1; at this time if TXBEIEN bit of SPI_CTRL2 register is set, an interrupt will be generated. In order to ensure the continuity of data transmission, the next data should be written to SPI_DATA register before the data transmission is completed; otherwise, "underrun" will occur, and the UDRFLG flag bit will be set to 1.

SCHDIR bit of SPI_STS register indicates the channel corresponding to the transmit data. In the slave mode, the SCHDIR bit is determined by the WS signal of the external master device.

In MSB and LSB alignment mode of I2S, the first data written to the data register corresponds to the data of the left channel.

Disable I2S, and after the TXBEFLG flag bit is set to 1, BSYFLG flag bit can be cleared.

21.5.3.6 I2S slave mode receiving process

RXBNEFLG flag is used to control the receiving sequence. The RXBNEFLG flag indicates whether the receive buffer is empty; after the receive buffer is full, the RXBNEFLG flag bit will be set to 1; if RXBNEIEN bit of SPI_CTRL2 register is set, an interrupt will occur, and after the data are read out from SPI_DATA register, RXBNEFLG flag bit will be cleared; make sure to receive new data after read operation; otherwise, "overrun" will occur, and the OVRFLG flag bit will be set to 1.

The value of SCHDIR should be updated immediately after receiving data, and it depends on the WS signal generated by I2S.

Regardless of the data type and the channel length, the audio data is always received in the form of 16 bits. According to the configured data and the length of the channel, the data needs to be transmit to the receive buffer once or twice.

Disable I2S, and when receiving the last RXBNEFLG set to 1, I2SEN flag bit will be cleared.

21.5.4 I2S Interrupt

21.5.4.1 State flag bit

There are three state flag bits in I2S to monitor the state of I2S bus.

Transmit buffer empty flag bit TXBEFLG

When the TXBEFLG flag bit is 1, it indicates that the transmit buffer is empty, and the data to be transmit can be written to the transmit buffer; after data is written, the TXBEFLG flag bit will be cleared. (When I2S is disabled, the TXBEFLG flag bit is 0).

Receive buffer non-empty flag bit RXBNEFLG

When the RXBNEFLG flag bit is 1, it indicates that the receive buffer has data to be received; after read operation is performed on the SPI_DATA register, RXBNEFLG flag bit will be cleared.

Busy flag bit BSYFLG

When the BSYFLG flag bit is 1, it indicates that I2S is in communication state (set and cleared by hardware), but in the master receiving mode, the BSYFLG flag bit is always 0 during the receiving period.

When I2S is disabled and data transmission is over, the BSYFLG flag bit will be cleared.

During continuous communication

- In the master sending mode, the BSYFLG flag bit is always high during the transmission period.
- In the slave mode, during transmission of each data item, the BSYFLG flag bit is set to 0 within one I2S clock cycle.

Channel flag bit SCHDIR

In the sending mode, the SCHDIR flag bit indicates the data transmit on the SD pin is in the left channel or the right channel. This flag bit is refreshed when TXBEFLG=1.

In the sending process of slave mode, if there is an underrun error, the value of SCHDIR flag bit will be invalid. If needing to restart the communication, the I2S function should be turned off and then turned on.

In the receiving mode, the SCHDIR flag bit indicates the received data is from the left channel or the right channel. This flag bit is refreshed when SPI_DATA register receives data.

If there is an underrun error in the receiving mode, the value of SCHDIR flag bit will be invalid. If needing to restart the communication, the I2S function should be turned off and then turned on.

As there is no channel selection in PCM standard, the SCHDIR flg bit is meaningless.

When OVRFLG and UDRFLG flag bits of SPI_STS register is 1 and ERRIEN=1 for SPI_CTRL2, interrupt will be generated. The interrupt flag can be cleared by reading the value of SPI_STS register.

21.5.4.2 Error flag bit

I2S includes two error flag bits

Underrun flag bit UDRFLG

In the sending mode, if new data to be transmit is written to SPI_DATA register before the data is transmit, UDRFLG flag bit will be set to 1; at this time if ERRIEN bit of SPI_CTRL2 register is set to 1, an interrupt will be generated.

This flag bit will take effect only after I2SMOD bit of SPI_I2SCFG is set to 1. Clear the UDRFLG flag bit by reading SPI_STS register.

Overrun flag bit OVRFLG

In the receiving mode, if a new data is received before the data is read,

OVRFLG flag bit will be set to 1. At this time if ERRIEN bit of SPI_CTRL2 register is set to 1, an interrupt will be generated, indicating the occurrence of the error.

Read SPI_DATA register to return the last correctly received data, and all the other newly received data will be lost. OVRFLG flag can be cleared by first reading SPI_STS register and then reading SPI_DATA register.

Table 69 I2C Interrupt Request

Interrupt flag	Interrupt event	Enable control bit	Clearing method
TXBEFLG	Transmit buffer empty flag	TXBEIEN	Write SPI_DATA register
RXBNEFLG	Receive buffer non-empty flag	RXBNEIEN	Read SPI_DATA register
OVRFLG	Underrun flag bit	ERRIEN	Read SPI_STS register
UDRFLG	Overrun flag bit		Read SPI_STS register Read SPI_DATA register again

21.5.4.3 DMA function

In I2S mode, the work mode of DMA is the same as that of SPI, except that it does not support CRC function.

21.6 Register Address Mapping

Table 70 SPI and I2S Register Mapping

Register name	Description	Offset address
SPI_CTRL1	SPI control register 1	0x00
SPI_CTRL2	SPI control register 2	0x04
SPI_STS	SPI state register	0x08
SPI_DATA	SPI data register	0x0C
SPI_CRCPOLY	SPI CRC polynomial register	0x10
SPI_RXCRC	SPI receive CRC register	0x14
SPI_TXCRC	SPI transmit CRC register	0x18
SPI_I2S_CFG	SPI I2S configuration register	0x1C
SPI_I2SPSC	SPI I2S prescaler register	0x20

21.7 Register Functional Description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

21.7.1 SPI control register 1 (SPI_CTRL1) (not used in I2S mode)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CPHA	R/W	Clock Phase Configure This bit indicates on the edge of which clock to start sampling 0: On the edge of No. 1 clock 1: On the edge of No. 2 clock Note: This bit cannot be modified during communication.
1	CPOL	R/W	Clock Polarity Configure Level state maintained by SCK when SPI is in idle state. 0: Low level 1: High level Note: This bit cannot be modified during communication
2	MSMCFG	R/W	Master/Salve Mode Configure 0: Configure as slave mode 1: Configure as master mode Note: This bit cannot be modified during communication
5:3	BRSEL	R/W	Baud Rate Divider Factor Select 000：DIV=2 001：DIV=4 010：DIV=8 011：DIV=16 100：DIV=32 101：DIV=64 110：DIV=128 111：DIV=256 Baud rate=FPCLK/DIV Note: This bit cannot be modified during communication
6	SPIEN	R/W	SPI Device Enable 0: Disable 1: Enable Note: When SPI device is disabled, please operate according to the process of closing SPI.
7	LSBSEL	R/W	LSB First Transfer Select 0: First send the most significant bit (MSB) 1: First send the least significant bit (LSB)
8	ISSEL	R/W	Internal Slave Device Select When CTRL1_SSEN=1 (software NSS mode), select internal NSS level by configuring the bit 0: Internal NSS is low 1: Internal NSS is high

Field	Name	R/W	Description
9	SSEN	R/W	Software Slave Device Enable 0: Software NSS mode is disabled, and the internal NSS level is determined by external NSS pin 1: Software NSS mode is enabled, and the internal NSS level is determined by external ISSEL pin
10	RXOMEN	R/W	Receive Only Mode Enable 0: Transmit and receive at the same time 1: Receive-only mode RXOMEN bit and BMEN bit together determine the transmission direction in the two-line and two-way mode. In the configuration of multiple slave devices, in order to avoid data transmission conflict, it is necessary to set RXOMEN bit to 1 on the slave devices that are not accessed.
11	DFLSEL	R/W	Data Frame Length Format Select 0: 8-bit data frame format 1: 16-bit data frame format Only when SPIEN=0, can this bit be written to change the data frame length.
12	CRCNXT	R/W	CRC Transfer Next Enable 0: The next transmitted data is from transmit buffer 1: The next transmitted data is from CRC register Note: After the last data is written to SPI_DATA register, set CRCNXT bit immediately.
13	CRCEN	R/W	CRC Calculate Enable 0: Disable 1: Enable CRC check function only applies to full duplex mode; only when SPIEN=0, can this bit be changed.
14	BMOEN	R/W	Bidirectional Mode Output Enable 0: Disable, namely, receive-only mode 1: Enable, namely, transmit-only mode When BMEN=1, namely, in single-line/double-line mode, this bit decides the transmission direction of transmission line.
15	BMEN	R/W	Bidirectional Mode Enable 0: Double-line unidirectional mode 1: Single-line bidirectional mode Single-line two-way transmission means: the transmission between MOSI pin of data master and MISO pin of slave

21.7.2 SPI control register 2 (SPI_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
0	RXDEN	R/W	Receive Buffer DMA Enable When RXDEN=1, once RXBNEFLG flag is set, DMA request will be issued. 0: Disable 1: Enable
1	TXDEN	R/W	Transmit Buffer DMA Enable When this bit is set, once TXBEFLG flag is set, DMA request will be issued. 0: Disable 1: Enable
2	SSOEN	R/W	SS Output Enable SS output in master mode 0: SS output is disabled, and it can work in multi-master mode. 1: SS output is enabled, and it cannot work in multi-master mode. Note: Not used in I2S mode.
4:3	Reserved		
5	ERRIEN	R/W	Error interrupt Enable 0: Disable 1: Enable When an error occurs, ERRIEN bit controls whether to generate the interrupt.
6	RXBNEIEN	R/W	Receive Buffer Not Empty Interrupt Enable 0: Disable 1: Enable When RXBNEFLG flag bit is set to 1, an interrupt request will be generated
7	TXBEIEN	R/W	Transmit Buffer Empty Interrupt Enable 0: Disable 1: Enable When TXBEFLG fag bit is set to 1, an interrupt request will be generated
15:8	Reserved		

21.7.3 SPI state register (SPI_STS)

Offset address: 0x08

Reset value: 0x0002

Field	Name	R/W	Description
0	RXBNEFLG	R	Receive Buffer Not Empty Flag 0: Empty 1: Not empty
1	TXBEFLG	R	Transmit Buffer Empty Flag 0: Not empty 1: Empty

Field	Name	R/W	Description
2	SCHDIR	R	Sound Channel Direction Flag 0: Indicate that the left channel is transmitting or receiving the required data 1: Indicate that the right channel is transmitting or receiving the required data Note: Not used in SPI mode, without left and right channels in PCM mode.
3	UDRFLG	R	Underrun Occur Flag 0: Not occur 1: Occurred This flag bit is set by hardware, and it can be cleared by writing 0 to this bit by software. Not used in SPI mode
4	CRCEFLG	RC_W0	CRC Error Occur Flag This bit indicates whether the received CRC value matches the value of RXCRC register 0: Match 1: Not match This bit is set by hardware, can be cleared by writing 0 to this bit by software, and is not used in I2S mode.
5	MEFLG	R	Mode Error Occur Flag 0: Not occur 1: Occurred This bit is set by hardware, can be cleared by writing 0 to this bit by software, and is not used in I2S mode.
6	OVRFLG	R	Overrun Occur Flag 0: Not occur 1: Occurred This bit is set by hardware, and it can be cleared by writing 0 to this bit by software.
7	BSYFLG	R	SPI Busy Flag 0: SPI is idle 1: SPI is communicating It is set or cleared by hardware.
15:8	Reserved		

21.7.4 SPI data register (SPI_DATA)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	DATA	R/W	Transmit Receive Data register When writing this register, the data will be written to the transmit buffer; when reading this register, the data in receive buffer will be read. The size of the buffer is consistent with the length of the data frame, that is, for 8-bit data, only DATA[7:0] is used when sending and receiving data, and DATA[15:8] is invalid; for 16-bit data, DATA[15:0] will be used when sending and receiving data.

21.7.5 SPI CRC polynomial register (SPI_CRCPOLY) (not used in I2S mode)

Offset address: 0x10

Reset value: 0x0007

Field	Name	R/W	Description
15:0	CRCPOLY	R/W	CRC Polynomial Value Setup This register contains CRC polynomial of CRC computing, which can be modified, and the reset value is 0x0007.

21.7.6 SPI receive CRC register (SPI_RXCRC) (not used in I2S mode)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
15:0	RXCRC	R	Receive Data CRC Value The CRC data of receive data calculated by hardware are stored in this register; the bits and the length of data frames are consistent, that is, if the received data are 8 bits, the CRC computing is made based on CRC8; if the received data are 16 bits, the CRC computing is made based on CRC16. When CRCEN is set, the hardware clears the register. Note: When BSYFLG bit is set to 1, the value of reading RXCRC register may be wrong.

21.7.7 SPI transmit CRC register (SPI_TXCRC)

Offset address: 0x18

Reset value: 0x0000

Field	Name	R/W	Description
15:0	TXCRC	R	Transmit Data CRC Value The CRC data of transmitted data calculated by hardware are stored in this register; the bits and the length of data frames are consistent, that is, if the transmitted data are 8 bits, the CRC computing is based on CRC8; if the transmitted data are 16 bits, the CRC computing is based on CRC16. When CRCEN is set, the hardware clears the register. Note: When BSYFLG bit is set to 1, the value of reading RXCRC register may be wrong.

21.7.8 SPI_I2S configuration register (SPI_I2SCFG)

Offset address: 0x1C

Reset value: 0x0000

Field	Name	R/W	Description
0	CHLEN	R/W	Channel Length Configure The channel length refers to the data bits per audio channel 0: 16-bit width 1: 32-bit width The vocal tract length can be configured successfully only when the vocal tract length is greater than the data length; otherwise, the hardware will automatically adjust the vocal tract length; this bit can only be configured when I2SEN=0, and is not used in SPI mode.

Field	Name	R/W	Description
2:1	DATALEN	R/W	Configure the Length of the sData to Be Transferred 00: 16-bit data length 01: 24-bit data length 10: 32-bit data length 11: Not allowed This bit can only be configured when I2SEN=0, and is not used in SPI mode.
3	CPOL	R/W	Idle State Clock Polarity Configure 0: Low level 1: High level This bit can only be configured when I2SEN=0, and is not used in SPI mode.
5:4	I2SSSEL	R/W	I2S Standard Selection 00: I2S Philips standard 01: High-byte alignment standard (left alignment) 10: Low-byte alignment standard (right alignment) 11: PCM standard This bit can only be configured when I2SEN=0, and is not used in SPI mode.
6	Reserved		
7	PFSSEL	R/W	PCM Frame Synchronization Mode Select 0: Synchronization of short frames 1: Synchronization of long frames Apply only to PCM standard (I2SSSEL=11); this bit can only be configured when I2SEN=0, and is not used in SPI mode.
9:8	I2SMOD	R/W	I2S Master/Slave Transmit/Receive Mode Configure 00: Slave device transmits 01: Slave device receives 10: Master device transmits 11: Master device receives This bit can only be configured when I2SEN=0, and is not used in SPI mode.
10	I2SEN	R/W	I2S Enable 0: I2S is disabled 1: I2S is enabled Note: It is not used in SPI mode.
11	MODESEL	R/W	SPI/I2S Mode Select 0: Select SPI mode 1: Select I2S mode Note: This bit can be set only when SPI or I2S is disabled.
15:12	Reserved		

21.7.9 SPI_I2S prescaler register (SPI_I2SPSC) (not used in SPI mode)

Offset address: 0x20

Reset value: 0x0002

Field	Name	R/W	Description
7:0	I2SPSC	R/W	I2S Linear Prescaler Factor Configure I2SPSC cannot be set to 0 and 1; this bit can be configured only when I2SEN=0, and it is not used in SPI mode.
8	ODDPSC	R/W	Configure the prescaler factor to be odd 0: Actual division factor=I2SPSC*2 1: Actual division factor=(I2SPSC*2) +1 This bit can only be configured when I2SEN=0, and is not used in SPI mode.
9	MCOEN	R/W	Master Device Clock Output Enable 0: Disable 1: Enable This bit can only be configured when I2SEN=0, and is not used in SPI mode.
15:10	Reserved		

22 Controller Area Network (CAN)

22.1 Full Name and Abbreviation Description of Terms

Table 71 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
First Input First Output	FIFO
Request	REQ

22.2 Introduction

CAN is abbreviation of Controller Area Network, and is serial communication protocol of ISO international standardization and supports CAN Protocol 2.0A and 2.0B. In CAN protocol, the sender sends the message to all receivers in the form of broadcast. When the node receives the message, it will go through the filter group and decide whether the message is needed according to the identifier. This design saves the CPU overhead.

22.3 Main Characteristics

（1） Support CAN protocol 2.0A and 2.0B

（2） The maximum baud rate of communication is 1Mbit/s

（3） Transmission function

- There are three transmitting mailboxes
- The priority of transmitting message can be configured
- Record the transmission time

（4） Receiving function

- Have two receive FIFO with three depth levels
- CAN1 has 28 fiflter groups. Groups 0-13 control the filtering conditions of CAN1, and groups 14-27 control the filtering conditions of CAN2. CAN1 must be enabled before CAN2 can be used.
- Record the receiving time

（5） Memory

- CAN1 and USBD1 share 512Byte SRAM
- CAN2 and USBD2 share 512Byte SRAM
- CAN1 and USBD2 are used at the same time
- CAN2 and USBD1 are used at the same time
- CAN1 and CAN2 are used at the same time

22.4 Functional Description

22.4.1 Characteristics of CAN Physical Layer

There can be multiple communication nodes on the CAN bus, each node consists of a CAN controller and a transceiver. The controller and transceiver are connected through CAN_TX and CAN_RX to transmit logic signals; the transceiver and bus are connected through CAN_High and CAN_Low to transmit differential signals.

22.4.2 Message Structure

Figure 98 Standard Data Frame

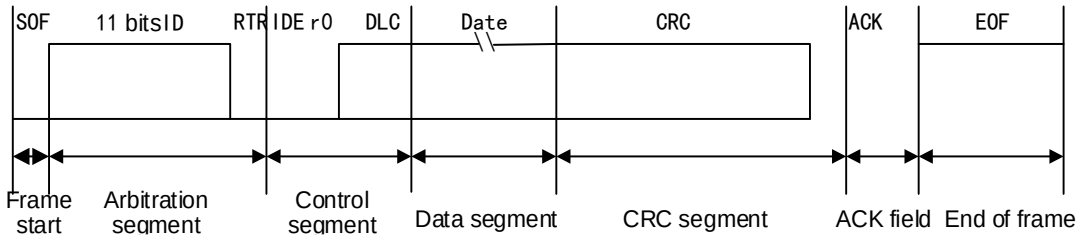
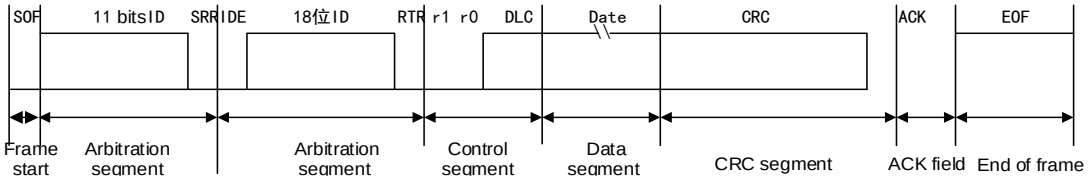


Figure 99 Extended Data Frame



Note:

(1) Frame start: used to inform each node that there will be data for transmission.

(2) Arbitration segment: It is used to decide which message can be transmitted when multiple messages are transmitted. Main content of this segment is ID information, the ID in standard format is 11 bits, and the ID in extended format is 29 bits.

(3) Control segment: The main content of this segment is data length code (DLC), which is used to indicate how many bytes the data segment has in the message. The data segment has up to 8 bytes.

(4) Data segment: Include the data information to be transmitted by the node.

(5) CRC segment: CRC check code is used to ensure correct transmission of the messages.

(6) ACK segment: This segment includes ACK slot bit and ACK delimiter bit. The transmitting node in ACK slot sends recessive bits, while the receiving node sends the dominant bit in this bit to acknowledge.

(7) Frame end: Seven recessive bits transmitted by the transmitting nodes are used to indicate the end.

22.4.3 Working Mode

CAN has three main working modes: initialization mode, normal mode and sleep mode.

22.4.3.1 Initialization mode

Set the INITREQ bit of the configuration register CAN_MCTRL to 1 to request to enter the initialization mode; clear the INITFLG bit to confirm entering the initialization mode.

Clear the INITREQ bit of the configuration register CAN_MCTRL to request to exit the initialization mode; clear the INITFLG bit to confirm exiting the initialization mode.

Message receiving and transmitting is disabled in initialization mode.

22.4.3.2 Normal mode

Clear the INITREQ bit of the configuration register CAN_MCTRL through software to request to enter the normal mode from the initialization mode; wait for the hardware to clear the INITFLG bit to enter the normal mode.

Message receiving and transmitting is allowed in normal mode.

22.4.3.3 Sleep mode

Set the SLEEPREQ bit of the configuration register CAN_MCTRL to 1 to request to enter the sleep mode.

The clock of CAN stops work in sleep mode, the software can normally access the mailbox register, and the CAN is in low-power state.

22.4.4 Communication Mode

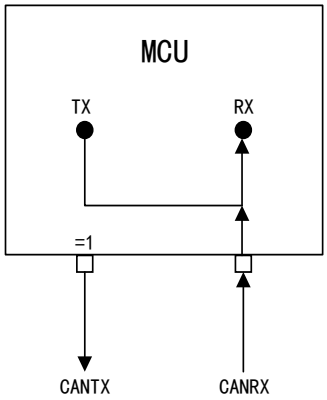
There are four communication modes: silent mode, loopback mode, silent loopback mode and normal mode. Different communication modes can be selected only in initialization mode.

22.4.4.1 Silent mode

Set the SILMEN bit of the configuration register CAN_BITTIM to 1 and select the silent mode.

In this mode, only recessive bit (logic 1)can be transmitted to the bus, while the dominant bit (logic 0) cannot be transmitted, and the data can be received from the bus.

Figure 100 CAN Works in Silent Mode

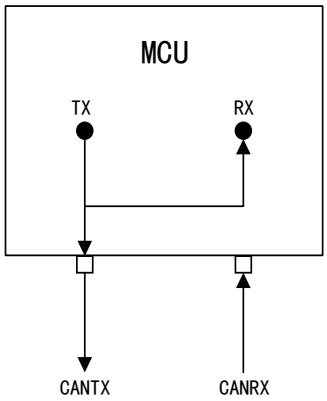


22.4.4.2 Loopback mode

Set the LBKMEN bit of the configuration register CAN_BITTIM to 1 and select the loopback mode.

In this mode, the transmitted data are directly transmitted to the input end for receiving, the data are not received from the bus, and all data can be transmitted to the bus.

Figure 101 CAN Works in Loopback Mode

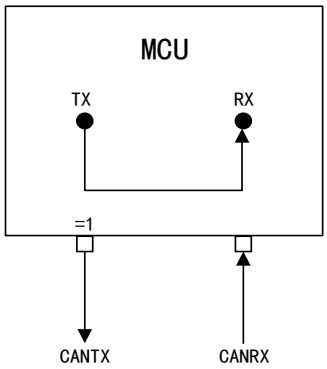


22.4.4.3 Loopback silent mode

Set the LBKMEN and SILMEN bits of the configuration register CAN_BITTIM to 1 and select the loopback silent mode.

In this mode, the transmitted data are directly transmitted to the input end for receiving, and the data are not received from the bus; only recessive bit (logic 1) can be transmitted to the bus, while the dominant bit (logic 0) cannot be transmitted.

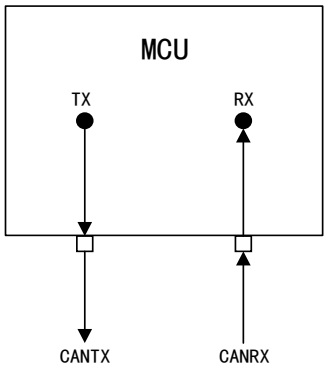
Figure 102 CAN Works in Silent Loopback Mode



22.4.4.4 Normal mode

In this mode, data can be transmitted to the bus and be received from the bus.

Figure 103 CAN Works in Normal Mode



22.4.5 Data Transmission

22.4.5.1 Conversion of transmitting mailbox state

Conversion process of transmitting mailbox state:

（1） First select an empty mailbox to set, submit the transmitting request to the CAN bus controller by setting the TXMREQ bit of the configuration register CAN_TXMIDx to 1, and then the mailbox immediately enters the registration state.

（2） When multiple mailboxes are in the registered state, conduct priority scheduling. When a mailbox has the highest priority, it will enter the predetermined state.

（3） When the message in the transmitting mailbox is transmitted to the bus, it will enter the transmitting state.

（4） After the message is transmitted successfully, the mailbox will become idle again.

22.4.5.2 Transmitting priority

When multiple messages are waiting for transmitting, determine the transmitting sequence through the TXFPCFG bit of the configuration register CAN_MCTRL:

- When the TXFPCFG bit is set to 0, the priority is determined by the message identifier, the identifier is the lowest, the priority is the highest, the identifier is equal, and the message with small mailbox number will be transmitted first
- When the TXFPCFG bit is set to 1, the priority will be determined by the sequence of transmitting request

22.4.5.3 Abort

Transmit the abort request by setting the ABREQFLG bit of the configuration register CAN_TXSTS to 1.

If the mailbox is in registered or predetermined state, stop transmitting the request immediately; if the mailbox is in the transmitting state, there are two conditions: one is that the mailbox is successfully transmitted, the mailbox becomes empty, in such case, the TXSUSFLG bit of the CAN_TXSTS register is set to 1 by hardware; the other is that the mailbox fails to transmit, the mailbox becomes predetermined and the transmitting request is aborted.

22.4.5.4 Automatic retransmission is disabled

Generally, in time triggered communication mode, automatic retransmission should be disabled.

In the mode that the automatic retransmission is disabled, the message is transmitted only once, and no matter what the result is (success, error or arbitration loss), the hardware will not transmit the message again automatically.

When the transmitting process is finished, set the REQCFLG bit of the CAN_TXSTS register to 1, and the transmitting result will be on the TXSUSFLG, ARBLSTFLG and TXERRFLG bits

22.4.6 Data Receiving

22.4.6.1 Receive FIFO

CAN has two receive FIFOs, each FIFO has three mailboxes, the FMNUM[1:0] bit of the register CAN_RXF reflects the number of messages currently stored; set the RFOM bit to1 to release the output mailbox of receive FIFO; FFULLFLG is the full state flag bit; FOVRFLG is overrun state flag bit.

22.4.6.2 Receive FIFO state conversion

At the beginning FIFO is in empty state, and after receiving the message, it will become registered.

When FIFO is in registered state and three mailboxes are full, after receiving next effective message, it will enter the overrun state, and there are two situations for loss of messages in overrun state:

- If FIFO lock function is disabled, the finally received message will be covered by new message

- If FIFO lock function is enabled, the newly received message will be discarded

22.4.7 Filtering Mechanism

Function of the filter: The receiving node decides whether the message is needed according to the message identifier, and only the required message will be received after filtering. CAN controller has 14 filter groups.

22.4.7.1 Bit width

Each group of filters can configure two kinds of bit width.

Figure 104 One 32-bit Filter

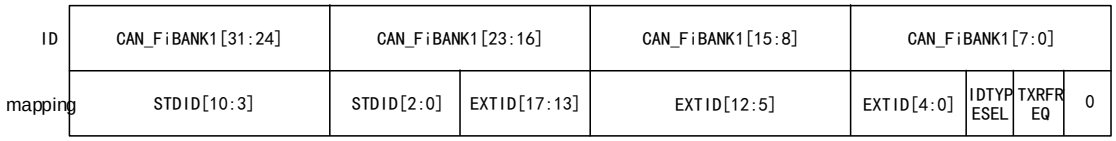
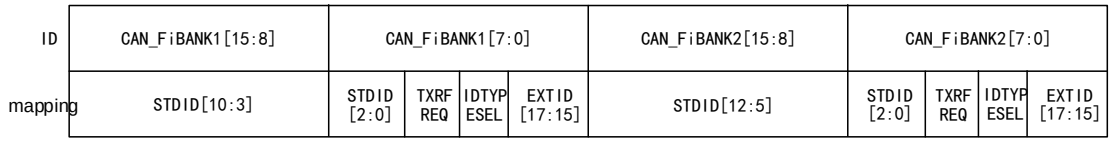


Figure 105 Two 16-bit Filters



22.4.7.2 Filtering mode

Mask bit mode

In this mode, it is only required to use some bits of the message identifier as a list to form the mask, and the message ID should be the same as the mask, and then the message can be received

Table 72 Mask Bit Mode Example

ID	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**…….**
Mask	1	0	1	1	1	0	0	1	……
Screened ID	1	X	1	1	0	X	X	0	……

Identifier list mode

In this mode, each bit of the message ID needs to be the same as the filter identifier, and then the message can be received.

Table 73 Identifier List Mode Example

ID	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**1**
ID	1	1	1	0	1	0	0	1	1
Screened ID	1	1	1	0	1	0	0	1	1

22.4.7.3 Filter priority

The priority rules are as follows:

- The priority of the filter with width of 32 bits is higher than that with width of 16 bits
- Under the condition of the same bit width, the priority of the identifier list mode is higher than that of mask bit mode
- Under the condition of the same bit width and mode, the priority of the small filtering number is high

22.4.8 Bit Timing and Baud Rate

22.4.8.1 Bit timing

The CAN peripheral bit timing of APM32 contains three segments: synchronization segment (SYNC_SEG), time segment 1 (BS1) and time segment 2 (BS2), and the sampling points are at the junction of BS1 and BS2 segments.

- Synchronization segment (SYNC_SEG): This bit occupies one time cell
- Time segment 1 (BS1): This segment occupies one to 16 time cells, and it contains PROP_SEG and PHASE_SEG1 in CAN standard
- Time segment 2 (BS2): This segment occupies one to eight time cells, and it represents PHASE_SEG2 in CAN standard

22.4.8.2 Calculation of baud rate

Time of BS1 segment: $T_{s1}=T_q*$ (TIMSEG1[3:0]+1)

Time of BS2 segment: $T_{s2}=T_q*$ (TIMSEG2[2:0]+1)

Time of one data bit: $T1bit=1T_q+T_{s1+}T_{s2}$

Baud rate=1/ T1bit

T_q =（BRPSC+1）* T_{PCLK}

22.4.9 Error Management

Transmit the error counter through the TXERRCNT bit of the configuration register CAN_ERRSTS and receive the error counter through the RXERRCNT bit of the register CAN_ERRSTS to reflect the error management of CAN bus.

Control the generation of interrupt in error state through the ERRIEN bit of the configuration register CAN_INTEN.

22.4.9.1 Bus-off recovery

When the TXERRCNT of the CAN error state register is greater than 255, the CAN bus controller will enter the bus-off state, then the BOFLG bit of the register CAN_ERRSTS is set to 1, and in this state, the CAN bus controller cannot receive and transmit messages.

Decide the bus-off recovery mode through the ALBOFFM bit of the configuration register CAN_MCTRL:

- If the ALBOFFM bit is set to 1, once the hardware detects 11 continuous recessive bits for 128 times, it will exit the bus-off state automatically;
- If the ALBOFFM bit is set to 0, after the software requests to enter and then exit the initialization mode, it will exit the bus-off state.

22.4.10 Interrupt

Events generating transmitting interrupt:

- The hardware sets REQCFLG0 bit of the register CAN_TXSTS to 1, and the transmitting mailbox 0 becomes idle
- The hardware sets REQCFLG1 bit of the register CAN_TXSTS to 1, and the transmitting mailbox 1 becomes idle
- The hardware sets REQCFLG2 bit of the register CAN_TXSTS to 1, and the transmitting mailbox 2 becomes idle

Events generating FIFO0 interrupt:

- Set the FMNUM0[1:0] bit of the register CAN_RXF0 to a number rather than 0 by the hardware, and FIFO0 will receive a new message
- Set the FFULLFLG0 bit of the register CAN_RXF0 to 1 by the hardware, and FIFO0 will be full
- Set the FOVRFLG0 bit of the register CAN_RXF0 to 1 by the hardware and FIFO0 will overrun

Events generating FIFO1 interrupt:

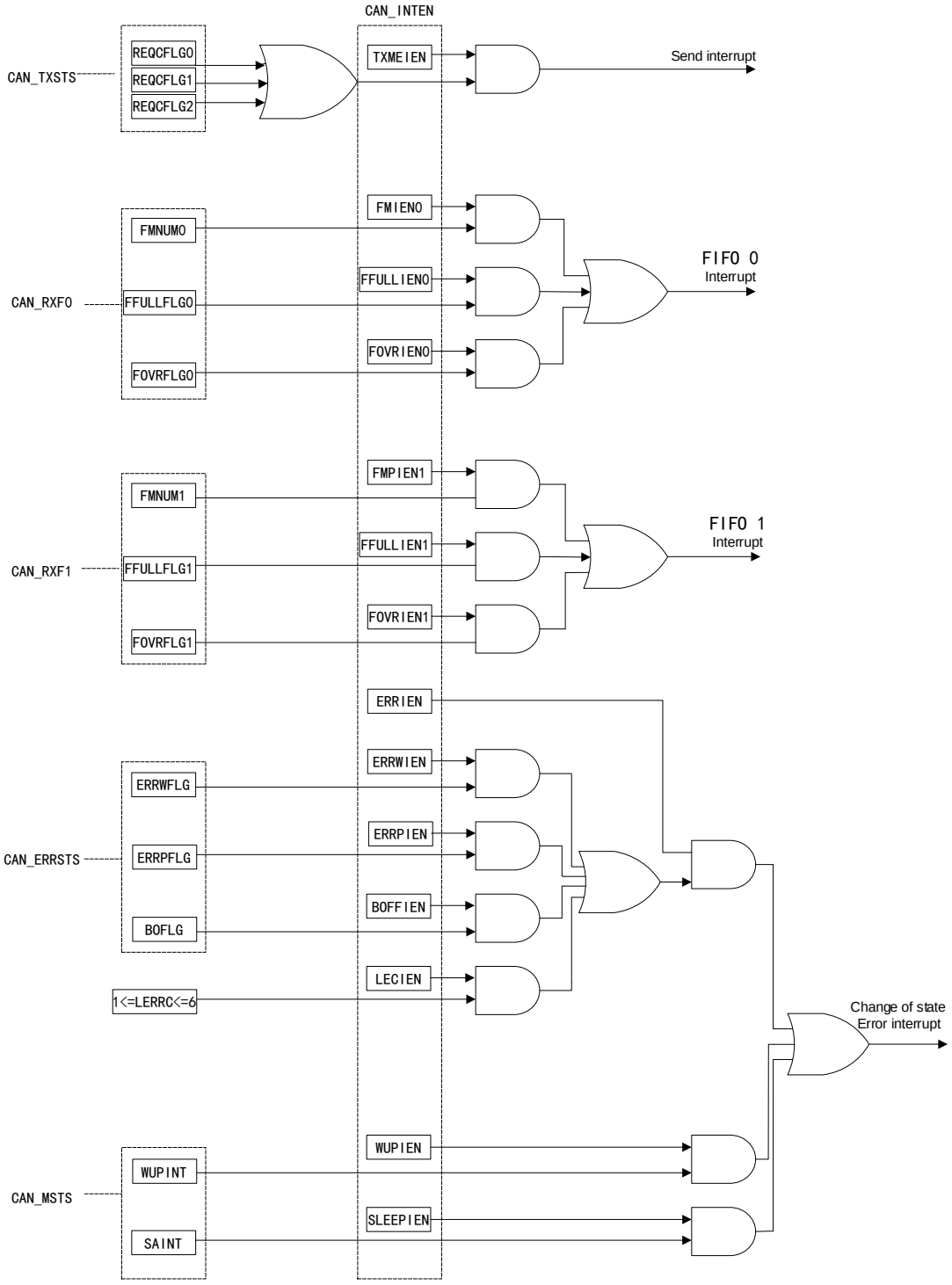
- Set the FMNUM1[1:0] bit of the register CAN_RXF1 to a number rather than 0 by the hardware, and FIFO1 will receive a new message
- Set the FFULLFLG1 bit of the register CAN_RXF1 to 1 by the hardware, and FIFO1 will be full
- Set the FOVRFLG1 bit of the register CAN_RXF1 to 1 by the hardware and FIFO1 will overrun

Events generating state change and error interrupt:

- Set the SLEEPIEN bit of the register CAN_INTEN to 1 by the hardware and it will enter the sleep mode
- Set the WUPIEN bit of the register CAN_INTEN to 1 by the hardware and interrupt enable will be woken up
- Set the ERRWFLG bit of the register CAN_ERRSTS to 1 by the hardware, and it means that the number of errors has reached the threshold
- Set the ERRPFLG bit of the register CAN_ERRSTS to 1 by the hardware, and it means that the number of errors has reached the threshold of passive error

- Set the LERRC[2:0] bit of the register CAN_ERRSTS by the hardware, and it indicates the condition of last error

Figure 106 Event Flag and Interrupt Generation



22.5 Register Address Mapping

CAN1 base address: 0x4000_6400

CAN2 base address: 0x4000_6800

Note: Except base address, the register and offset addresses of CAN1 and CAN2 are exactly the same.

Table 74 CAN Register Address Mapping

Register name	Description	Offset address
CAN_MCTRL	CAN main control register	0x00
CAN_MSTS	CAN main state register	0x04
CAN_TXSTS	CAN transmit state register	0x08
CAN_RXF0	CAN receive FIFO 0 register	0x0C
CAN_RXF1	CAN receive FIFO 1 register	0x10
CAN_INTEN	CAN interrupt enable register	0x14
CAN_ERRSTS	CAN error state register	0x18
CAN_BITTIM	CAN bit timing register	0x1C
CAN_TXMIDx	Transmitting mailbox identifier register	0x180, 0x190, 0x1A0
CAN_TXDLENx	Transmitting mailbox data length register	0x184, 0x194, 0x1A4
CAN_TXMDLx	Transmitting mailbox low-byte data register	0x188, 0x198, 0x1A8
CAN_TXMDHx	Transmitting mailbox high-byte data register	0x18C, 0x19C, 0x1AC
CAN_RXMIDx	Receive FIFO mailbox identifier register	0x1B0, 0x1C0
CAN_RXDLENx	Receive FIFO mailbox data length register	0x1B4, 0x1C4
CAN_RXMDLx	Receive FIFO mailbox low-byte data register	0x1B8, 0x1C8
CAN_RXMDHx	Receive FIFO mailbox high-byte data register	0x1BC, 0x1CC
CAN_FCTRL	CAN filter main control register	0x200
CAN_FMCFG	CAN filter mode register	0x204
CAN_FSCFG	CAN filter bit width register	0x20C
CAN_FFASS	CAN filter FIFO association register	0x214
CAN_FACT	CAN filter activation register	0x21C
CAN_FiBANKx	Register x of CAN filter group i	0x240..0x2AC

22.6 Register Functional Description

22.6.1 CAN control and state register

22.6.1.1 CAN main control register (CAN_MCTRL)

Offset address: 0x00

Reset value: 0x0001 0002

Field	Name	R/W	Description
0	INITREQ	R/W	Request to Enter Initialization Mode

Field	Name	R/W	Description
			0: Enter the normal work mode from the initialization mode 1: Enter the initialization mode from the normal work mode
1	SLEEPREQ	R/W	Request to Enter Sleep Mode 0: Exit the sleep mode 1: Request to enter the sleep mode. If the AWUPCFG bit is set to 1, when the RX signal detects CAN message, this bit will be cleared by hardware; after reset, reset this bit to 1; after reset, it will enter the sleep mode.
2	TXFPCFG	R/W	Transmit FIFO Priority Configure This bit is used to determine which parameters determine the transmission priority when multiple messages are waiting for transmission. 0: Determined by the message identifier 1: Determined by the sequence of transmission request
3	RXFLOCK	R/W	Receive FIFO Locked Mode Configure This bit is used to determine whether FIFO is locked when receiving overrun, and how to deal with the next received message when the message of the receive FIFO has not been read out. 0: Unlocked; If the message of the receive FIFO is not read out, the next received message will cover the original message 1: Locked; when the message of the received FIFO is not read out, the next received message will be discarded
4	ARTXMD	R/W	Automatic Retransmission Message Disable 0: Automatic retransmission is enabled, and the message will be retransmitted automatically until it is transmitted successfully 1: Automatic retransmission is disabled and the message is transmitted only once
5	AWUPCFG	R/W	Automatic Wakeup Mode Configure 0: Software wakes up the sleep mode by clearing the SLEEPREQ bit of the CAN_MCTRL register 1: Hardware wakes up the sleep mode by detecting CAN message
6	ALBOFFM	R/W	Automatic Leaving Bus-Off Status Condition Management 0: After the software resets the INITREQ bit of the CAN_MCTRL register to 1 and then clears it, when the hardware detects 11 continuous recessive bits for 128 times, it will exit from the bus-off state 1: When the hardware detects 11 continuous recessive bits for 128 times, it will exit from the bus-off state automatically
14:7	Reserved		
15	SWRST	R/S	Software Reset CAN 0: Work normally 1: CAN is reset by force, and after reset, CAN enters the sleep mode; the hardware will clear this bit automatically
16	DBGFRZE	R/W	Debug Freeze 0: Invalid 1: During debugging, CAN cannot receive/transmit, but it still can read and write and control the receive FIFO normally
31:17	Reserved		

22.6.1.2 CAN main state register (CAN_MSTS)

Offset address: 0x04

Reset value: 0x0000 0C02

Field	Name	R/W	Description
0	INITFLG	R	Being Initialization Mode Flag This bit is set to 1 or cleared by hardware. 1: Exit the initialization mode 1: Being in the initialization mode; this bit is confirmation for initialization request bit of the CAN_MCTRL register.
1	SLEEPFLG	R	Being Sleep Mode Flag This bit is set to 1 or cleared by hardware 0: Exit the sleep mode 1: Being in the sleep mode; this bit is confirmation for sleep moderequest bit of the CAN_MCTRL register.
2	ERRIFLG	RC_W1	Error Interrupt Occur Flag This bit is set to 1 by hardware and written to 1 and cleared by software. 0: Not occur 1: Occurred
3	WUPIFLG	RC_W1	Wakeup Interrupt Occur Flag When entering the sleep mode and detecting SOP wake-up, the bit is set to 1 by hardware; it is written to 1 and cleared by software. 0: Failed to wake up from the sleep mode 1: Woke up from the sleep mode
4	SLEEPIFLG	RC_W1	Being Sleep Mode Interrupt Flag When entering the sleep mode, this bit is set to 1 by hardware and corresponding interrupt will be triggered; when exiting the sleep mode, this bit is cleared by hardware and is written as 1 and cleared by software. 0: Failed to enter the sleep mode 1: Entered the sleep mode
7:5	Reserved		
8	TXMFLG	R	Being Transmit Mode Flag 0: CAN is not in transmission mode 1: CAN is in transmission mode
9	RXMFLG	R	Being Receive Mode Flag 0: CAN is not in receiving mode 1: CAN is in receiving mode
10	LSAMVALUE	R	CAN Rx Pin Last Sample Value
11	RXSIGL	R	CAN Rx Pin Signal Level
31:12	Reserved		

22.6.1.3 CAN transmit state register (CAN_TXSTS)

Offset address: 0x08

Reset value: 0x1C00 0000

Field	Name	R/W	Description
0	REQCFLG0	RC_W1	Mailbox 0 Request Completed Flag When the last transmission or abortion request of the mailbox 0 is completed, this bit is set to 1 by hardware; when receiving the transmission request, this bit is cleared by hardware; it is written to 1 or cleared by software. 0: Being transmitted 1: Transmission completed
1	TXSUSFLG0	RC_W1	Mailbox 0 Transmission Success Flag When mailbox 0 attempts to transmit successfully, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Last transmission attempt failed 1: Last transmission attempt succeeded
2	ARBLSTFLG0	RC_W1	Mailbox 0 Arbitration Lost Flag When the mailbox 0 loses arbitration, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Meaningless 1: Lost
3	TXERRFLG0	RC_W1	Mailbox 0 Transmission Error Flag When mailbox 0 fails to transmit, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Meaningless 1: Failed to transmit
6:4	Reserved		
7	ABREQFLG0	R/S	Mailbox 0 Abort Request Flag If there is no message waiting for transmitting in mailbox 0, this bit is ineffective. 0: The transmitting message of mailbox 0 is cleared, and this bit is cleared by hardware 1: Set this bit to 1 to abort the transmission request of mailbox 0
8	REQCFLG1	RC_W1	Mailbox 1 Request Completed Flag When the last request of mailbox 1 is transmitted or aborted, this bit is set to 1 by hardware; When receiving the transmission request, this bit is cleared by hardware, and written to 1 and cleared by software. 0: Being transmitted 1: Transmission completed
9	TXSUSFLG1	RC_W1	Mailbox 1 Transmission Success Flag When mailbox 1 attempts to transmit successfully, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Last transmission attempt failed 1: Last transmission attempt succeeded
10	ARBLSTFLG1	RC_W1	Mailbox 1 Arbitration Lost Flag When the mailbox 1 loses arbitration, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Meaningless 1: Lost

Field	Name	R/W	Description
11	TXERRFLG1	RC_W1	Mailbox 1 Transmission Error Flag When mailbox 1 fails to transmit, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Meaningless 1: Failed to transmit
14:12	Reserved		
15	ABREQFLG1	R/S	Mailbox 1 Abort Request Flag If there is no message waiting for transmitting in mailbox 1, this bit is ineffective. 0: The transmitting message of mailbox 1 is cleared, and this bit is cleared by hardware 1: Set this bit to 1 to abort the transmission request of mailbox 1
16	REQCFLG2	RC_W1	Mailbox 2 Request Completed Flag When the last transmission or abortion request of the mailbox 2 is completed, this bit is set to 1 by hardware; when receiving the transmission request, this bit is cleared by hardware; it is written to 1 or cleared by software. 0: Being transmitted 1: Transmission completed
17	TXSUSFLG2	RC_W1	Mailbox 2 Transmission Success Flag When mailbox 2 attempts to transmit successfully, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Last transmission attempt failed 1: Last transmission attempt succeeded
18	ARBLSTFLG2	RC_W1	Mailbox 2 Arbitration Lost Flag When the mailbox 2 loses arbitration, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Meaningless 1: Lost
19	TXERRFLG2	RC_W1	Mailbox 2 Transmission Error Flag When mailbox 2 fails to transmit, this bit is set to 1 by hardware; and written to 1 and cleared by software. 0: Meaningless 1: Failed to transmit
22:20	Reserved		
23	ABREQFLG2	R/S	Mailbox 2 Abort Request Flag If there is no message waiting for transmitting in mailbox 2, this bit is ineffective. 0: The transmitting message of mailbox 2 is cleared, and this bit is cleared by hardware 1: Set this bit to 1 to abort the transmission request of mailbox 2
25:24	EMNUM[1:0]	R	Empty Mailbox Number This bit is applicable when there is empty mailbox. When all the transmitting mailboxes are empty, it means the number of the transmitting mailbox with the lowest priority; when the mailbox is not empty but not all empty, it means the number of next mailbox to be transmitted.

Field	Name	R/W	Description
26	TXMEFLG0	R	Transmit Mailbox 0 Empty Flag When the transmitting mailbox 0 is empty, this bit is set to 1 by hardware. 0: There is message to be transmitted in mailbox 0 1: There is no message to be transmitted in mailbox 0
27	TXMEFLG1	R	Transmit Mailbox 1 Empty Flag When the transmitting mailbox 1 is empty, this bit is set to 1 by hardware. 0: There is message to be transmitted in mailbox 1 1: There is no message to be transmitted in mailbox 1
28	TXMEFLG2	R	Transmit Mailbox 2 Empty Flag When the transmitting mailbox 2 is empty, this bit is set to 1 by hardware. 0: There is message to be transmitted in mailbox 2 1: There is no message to be transmitted in mailbox 2
29	LOWESTP0	R	the Lowest Transmission Priority Flag for Mailbox 0 0: Meaningless 1: The priority of mailbox 0 is the lowest among those mailboxes waiting to transmit messages Note: If there is only one mailbox waiting, LOWESTP[2:0] is cleared.
30	LOWESTP1	R	the Lowest Transmission Priority Flag for Mailbox 1 0: Meaningless 1: The priority of mailbox 1 is the lowest among those mailboxes waiting to transmit messages
31	LOWESTP2	R	the Lowest Transmission Priority Flag for Mailbox 2 0: Meaningless 1: The priority of mailbox 2 is the lowest among those mailboxes waiting to transmit messages

22.6.1.4 CAN receive FIFO 0 register (CAN_RXF0)

Offset address: 0x0C

Reset value: 0x00

Field	Name	R/W	Description
1:0	FMNUM0[1:0]	R	the number of Message in receive FIFO0 These bits are used to reflect the number of messages stored in current receive FIFO0. Every time a new message is received, add 1 to FMNUM0 bit; every time the mailbox message is released and outputted, subtract 1 from FMNUM0 bit.
2	Reserved		
3	FFULLFLG0	RC_W1	Receive FIFO0 Full Flag When there are three messages in FIFO0, it means the FIFO0 has been full; this bit is set to 1 by hardware and written to 1 and cleared by software. 0: Not full 1: Full

Field	Name	R/W	Description
4	FOVRFLG0	RC_W1	Receive FIFO 0 Overrun Flag When there are three messages in FIFO0 and then a new message is received, it means the FIFO0 overrun; this bit is set to 1 by hardware and written to 1 and cleared by software. 0: No overrun 1: Overrun is generated
5	RFOM0	R/S	Release Receive FIFO0 Output Mailbox to Receive Massage This bit is set to 1 by hardware and cleared by software. If there is no message in FIFO, this bit is invalid. When FIFO contains more than two messges, the output mailbox must be first released to acess the second message. 0: Meaningless 1: Release the output mailbox of receive FIFO0
31:6	Reserved		

22.6.1.5 CAN receive FIFO 1 register (CAN_RXF1)

Offset address: 0x10

Reset value: 0x00

Field	Name	R/W	Description
1:0	FMNUM1[1:0]	R	the number of Message in receive FIFO1 These bits are used to reflect the number of messages stored in current receive FIFO1. Every time a new message is received, add 1 to FMNUM1 bit; every time the mailbox message is released and outputted, subtract 1 from FMNUM1 bit.
2	Reserved		
3	FFULLFLG1	RC_W1	Receive FIFO0 Full Flag When there are three messages in FIFO1, it means the FIFO1 has been full; this bit is set to 1 by hardware and written to 1 and cleared by software. 0: Not full 1: Full
4	FOVRFLG1	RC_W1	Receive FIFO1 Overrun Flag When there are three messages in FIFO1 and then a new message is received, it means the FIFO1 overrun; this bit is set to 1 by hardware and written to 1 and cleared by software. 0: No overrun 1: Overrun is generated
5	RFOM1	R/S	Release Receive FIFO1 Output Mailbox to Receive Massage This bit is set to 1 by hardware and cleared by software. If there is no message in FIFO, this bit is invalid. When FIFO contains more than two messges, the output mailbox must be first released to acess the second message. 0: Meaningless 1: Release the output mailbox of receive FIFO1
31:6	Reserved		

22.6.1.6 CAN interrupt enable register (CAN_INTEN)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TXMEIEN	R/W	Transmit Mailbox Empty Interrupt Enable When REQCFLGx bit is set to 1, it means transmission has been completed, and the transmitting mailbox is empty; if this bit is set to 1, an interrupt will be generated. 0: No interrupt 1: Interrupt generated
1	FMIEN0	R/W	Interrupt Enable When the Number of FIFO0 Message Is Not 0 When FMNUM0[1:0] bit of FIFO 0 is not zero, it means that the number of messages in FIFO0 is not zero; if this bit is set to 1, an interrupt will be generated. 0: No interrupt 1: Interrupt generated
2	FFULLIEN0	R/W	FIFO0 Full Interrupt Enable When the FFULLFLG0 bit of FIFO0 is set to 1, it means that the message of FIFO0 is full; if this bit is set to 1, an interrupt will be generated. 0: No interrupt 1: Interrupt generated
3	FOVRIEN0	R/W	FIFO0 Overrun Interrupt Enable When the FOVRFLG0 bit of FIFO0 is set to 1, it means that the FIFO0 has been overloaded; if this bit is set to 1, an interrupt will be generated. 0: No interrupt 1: Interrupt generated
4	FMPIEN1	R/W	Interrupt Enable when the Number of FIFO1 Message is Not 0 When FMNUM1[1:0] bit of FIFO 1 is not zero, it means that the number of messages in FIFO1 is not zero; if this bit is set to 1, an interrupt will be generated. 0: No interrupt 1: Interrupt generated
5	FFULLIEN1	R/W	FIFO1 Full Interrupt Enable When the FFULLFLG1 bit of FIFO1 is set to 1, it means that the message of FIFO1 is full; if this bit is set to 1, an interrupt will be generated. 0: No interrupt 1: Interrupt generated
6	FOVRIEN1	R/W	FIFO1 Overrun Interrupt Enable When the FOVRFLG1 bit of FIFO1 is set to 1, it means that the FIFO1 has been overloaded; if this bit is set to 1, an interrupt will be generated. 0: No interrupt 1: Interrupt generated
7	Reserved		

Field	Name	R/W	Description
8	ERRWIEN	R/W	Error Warning Interrupt Enable When ERRWFLG bit is set to 1, an error warning will occur; if this bit is set to 1, ERRIFLG shall be set and a warning error interrupt will be generated. 0: ERRIFLG bit is not set 1: ERRIFLG bit is set to 1
9	ERRPIEN	R/W	Error Passive Interrupt Enable When ERRPFLG bit is set to 1, a pssive error will occur; if this bit is set to 1, ERRIFLG shall be set and a passive error interrupt will be generated. 0: ERRIFLG bit is not set 1: ERRIFLG bit is set to 1
10	BOFFIEN	R/W	Bus-Off Interrupt Enable When BOFFFLG bit is set to 1, bus-off will occur; if this bit is set to 1, ERRIFLG shall be set and a bus-off error interrupt will be generated. 0: ERRIFLG bit is not set 1: ERRIFLG bit is set to 1
11	LECIEN	R/W	Last Error Code Interrupt Enable When an error is detected and the hardware sets LERRC[2:0], the last error code is recorded. If this bit set to 1, the ERRIFLG is set to generate the last error interrupt. 0: ERRIFLG bit is not set 1: ERRIFLG bit is set to 1
14:12	Reserved		
15	ERRIEN	R/W	Error interrupt Enable When the corresponding error state register is set to 1, if this bit is set to 1, an error interrupt will be generated. 0: No interrupt 1: Interrupt generated
16	WUPIEN	R/W	Wakeup Interrupt Enable When WUPINT bit is set to 1, if this bit is set to 1, a wake-up interrupt will be generated. 0: No interrupt 1: Interrupt generated
17	SLEEPIEN	R/W	Sleep Interrupt Enable When SLEEPIFLG bit is set to 1, if this bit is set to 1, a sleep interrupt will be generated. 0: No interrupt 1: Interrupt generated
31:18	Reserved		

22.6.1.7 CAN error state register (CAN_ERRSTS)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ERRWFLG	R	Error Warning Occur Flag When the value of the receiving error counter or transmitting error counter ≥96, this bit is set to 1 by hardware. 0: No error warning 1: Error warning occurred
1	ERRPFLG	R	Error Passive Occur Flag When the value of the receiving error counter or transmitting error counter ≥127, this bit is set to 1 by hardware. 0: No passive error 1: Passive error appears
2	BOFLG	R	Enter Bus-Off Flag When the value of the transmitting error counter TXERRCNT is greater than 255, CAN will enter the bus-off state and this bit is set to 1 by hardware. 0: CAN not in bus-off state 1: CAN in bus-off state
3	Reserved		
6:4	LERRC	R/W	Record Last Error Code When the error on CAN bus is detected, it is set by hardware according to the error category; when the message is transmitted or received correctly, this bit is cleared by hardware. 000: No error 001: Bit stuffing error 010: Form (Form) error 011: Acknowledgment (ACK) error 100: Recessive bit error 101: Dominant bit error 110: CRC error 111: Set by software
15:7	Reserved		
23:16	TXERRCNT	R	Least Significant Byte of The 9-Bit Transmit Error Counter The counter is implemented according to the transmission part of fault definition mechanism of CAN protocol.
31:24	RXERRCNT	R	Receive Error Counter The receiving error counter is implemented according to the receiving part of fault definition mechanism of CAN protocol. When receiving error occurs, according to the condition of error, add 1 or 8 to the counter, and subtract 1 after receiving successfully. When the value of the counter is greater than 127, set the counter value to 120.

22.6.1.8 CAN bit timing register (CAN_BITTIM)

Offset address: 0x1C

Reset value: 0x0123 0000

Field	Name	R/W	Description
9:0	BRPSC	R/W	Baud Rate Prescaler Factor Setup

			Time cell t_q =(BRPSC+1)× t_{PCLK}
15:10	Reserved		
19:16	TIMSEG1	R/W	Time Segment 1 Setup Time occupied by time period 1 t_{BS1} = t_{CAN} x (TIMSEG1+1).
22:20	TIMSEG2	R/W	Time Segment 2 Setup Time occupied by time period 2 t_{BS2} = t_{CAN} x (TIMSEG2+1).
23	Reserved		
25:24	RSYNJW	R/W	Resynchronization Jump Width Time that CAN hardware can extend or shorten in this bit t_{RJW}=t_{CAN} x (RSYNJW+1).
29:26	Reserved		
30	LBKMEN	R/W	Loop Back Mode Enable 0: Disable 1: Enable
31	SILMEN	R/W	Silent Mode Enable 0: Normal state 1: Silent mode

Note: When CAN is in initialization mode, this register can be accessed only by software

22.6.2 CAN mailbox register

This section describes the transmitting and receiving mailbox registers.

The transmitting and receiving mailboxes are almost the same except the following examples:

- FMIDX domain of CAN_RXDLENx register;
- The receiving mailbox is read-only;
- The transmitting mailbox is writable only when it is empty, and if the corresponding TXMEFLG bit of CAN_TXSTS register is 1, it means the transmitting mailbox is empty.

There are three transmitting mailboxes and two receiving mailboxes in total. Each receiving mailbox is FIFO with three levels of depth, and can only access the message that is received first in FIFO.

22.6.2.1 Transmitting mailbox identifier register (CAN_TXMIDx) (x=0..2)

Offset address: 0x180, 0x190, 0x1A0

Reset value: 0xXXXX XXXX, X=undefined bit (except Bit 0, TXMREQ=0 after reset)

Field	Name	R/W	Description
0	TXMREQ	R/W	Transmit Mailbox Data Request 0: When the data in the mailbox is transmitted, the mailbox is empty and this bit is cleared by hardware 1: Software writes 1, to enable request to transmit mailbox data
1	TXRFREQ	R/W	Transmit Remote Frame Request 0: Data frame 1: Remote frame

Field	Name	R/W	Description
2	IDTYPESEL	R/W	Identifier Type Select 0: Stanard identifier 1: Extended identifier
20:3	EXTID[17:0]	R/W	Extended Identifier Setup Low byte of extended identity label.
31:21	STDID[10:0]/EXTID[28:18]	R/W	Standard Identifier or Extended Identifier According to the content of IDTYPESEL bit, these bits are standard identifier STDID[10:0] and high byte EXTID[28:18] of extended identifier.

Note: 1. When its mailbox is in the state of waiting for transmission, this register is write-protection

2. This register realizes transmission request control function (No. 0 bit) - the reset value is 0

22.6.2.2 Transmitting mailbox data length register (CAN_TXDLENx) (x=0..2)

When the mailbox is not idle, all bits of this register are write-protected.

Offset address: 0x184, 0x194, 0x1A4

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
3:0	DLCODE	R/W	Transmit Data Length Code Setup
31:4	Reserved		

22.6.2.3 Transmitting mailbox low-byte data register (CAN_TXMDLx) (x=0..2)

When the mailbox is not idle, all bits of this register are write-protected, and the message contains 0 to 7-byte data and starts from the byte 0.

Offset address: 0x188, 0x198, 0x1A8

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
7:0	DATABYTE0	R/W	Data Byte 0 of the Message
15:8	DATABYTE1	R/W	Data Byte 1 of the Message
23:16	DATABYTE2	R/W	Data Byte 2 of the Message
31:24	DATABYTE3	R/W	Data Byte 3 of the Message

22.6.2.4 Transmitting mailbox high-byte data register (CAN_TXMDHx) (x=0..2)

When the mailbox is not idle, all bits of this register are write-protected.

Offset address: 0x18C, 0x19C, 0x1AC

Reset value: 0xXXXX XXXX, X=undefined bit

Field	Name	R/W	Description
7:0	DATABYTE4	R/W	Data Byte 4 of the Message
15:8	DATABYTE5	R/W	Data Byte 5 of the Message
23:16	DATABYTE6	R/W	Data Byte 6 of the Message
31:24	DATABYTE7	R/W	Data Byte 7 of the Message

22.6.2.5 Receive FIFO mailbox identifier register (CAN_RXMIDx) (x=0..1)

Offset address: 0x1B0, 0x1C0

Reset value: 0xXXXX XXXX, X=undefined bit

Field	Name	R/W	Description
0	Reserved		
1	RFTXREQ	R	Remote Frame Transmission Request 0: Data frame 1: Remote frame
2	IDTYPESEL	R	Identifier Type Select 0: Stanard identifier 1: Extended identifier
20:3	EXTID[17:0]	R	Extended Identifier Setup Low byte of extended identifier.
31:21	STDID[10:0]/EXTID[28:18]	R	Standard Identifier or Extended Identifier According to the content of IDTYPESEL bit, these bits are standard identifier STDID[10:0] and high byte EXTID[28:18] of extended identifier.

Note: All receiving mailbox registers are read-only.

22.6.2.6 Receive FIFO mailbox data length register (CAN_RXDLENx) (x=0..1)

Offset address: 0x1B4, 0x1C4

Reset value: 0xXXXXX XXXX

Field	Name	R/W	Description
3:0	DLCODE	R	Receive Data Length Code Setup This bit represents the data length in the frame; for remote frame, DLCODE is constantly 0.
7:4	Reserved		
15:8	FMIDX	R	Filter Match Index Setup
31:16	Reserved		

Note: All receiving mailbox registers are read-only.

22.6.2.7 Receive FIFO mailbox low-byte data register (CAN_RXMDLx) (x=0..1)

Offset address: 0x1B8, 0x1C8; the message contains 0 to 8-byte data, which starts from the byte 0.

Reset value: 0xXXXXX XXXX

Field	Name	R/W	Description
7:0	DATABYTE0	R	Data Byte 0 of the Message
15:8	DATABYTE1	R	Data Byte 1 of the Message
23:16	DATABYTE2	R	Data Byte 2 of the Message
31:24	DATABYTE3	R	Data Byte 3 of the Message

Note: All receiving mailbox registers are read-only.

22.6.2.8 Receive FIFO mailbox high-byte data register (CAN_RXMDHx) (x=0..1)

Offset address: 0x1BC, 0x1CC

Reset value: 0xXXXX XXXX, X=undefined bit

Field	Name	R/W	Description
7:0	DATABYTE4	R	Data Byte 4 of the Message
15:8	DATABYTE5	R	Data Byte 5 of the Message
23:16	DATABYTE6	R	Data Byte 6 of the Message
31:24	DATABYTE7	R	Data Byte 7 of the Message

Note: All receiving mailbox registers are read-only.

22.6.3 CAN filter register

22.6.3.1 CAN filter main control register (CAN_FCTRL)

Offset address: 0x200

Reset value: 0x2A1C 0E01

Field	Name	R/W	Description
0	FINITEN	R/W	Filter Init Mode Enable 0: Normal mode 1: Initialization mode
7:1	Reserved		
13:8	CAN2SB	R/W	CAN2 Start Bank This bit is used to define the starting storage area of CAN2, range: 0-27. Note:(1) When CAN2SB = 28d, all filters of CAN1 can be used; When CAN2SB=0, all filters of CAN2 can be used.
31:14	Reserved		

Note: The non-reserved bit of this register is completely controlled by software.

22.6.3.2 CAN filter mode configuration register (CAN_FMCFG)

Offset addres: 0x204

Reset value: 0x0000 0000

Field	Name	R/W	Description
27:0	FMCFGx	R/W	Filter Mode Configure The value of x is within 0-27. 0: Identifier mask bit mode 1: Identifier list mode
31:28	Reserved		

Note: Only when CAN_FCTRL (FINITEN =1) is set to make the filter in initialization mode, can this register be written.

22.6.3.3 CAN filter bit width register (CAN_FSCFG)

Offset address: 0x20C

Reset value: 0x0000 0000

Field	Name	R/W	Description
27:0	FSCFGx	R/W	Filterx Scale Configure The value of x is within 0-27. 0: Two 16 bits 1: Single 32 bits
31:28	Reserved		

Note: Only when CAN_FCTRL (FINITEN =1) is set to make the filter in initialization mode, can this register be written.

22.6.3.4 CAN filter FIFO association register (CAN_FFASS)

Offset address: 0x214

Reset value: 0x0000 0000

Field	Name	R/W	Description
27:0	FFASSx	R/W	Configure Filterx Associated with FIFO The value of x is within 0-27. 0: The filter is associted with FIFO0 1: The filter is associted with FIFO1
31:28	Reserved		

Note: Only when CAN_FCTRL (FINITEN =1) is set to make the filter in initialization mode, can this register be written.

22.6.3.5 CAN filter activation register (CAN_FACT)

Offset address: 0x21C

Reset value: 0x0000 0000

Field	Name	R/W	Description
27:0	FACTx	R/W	Filterx Active The value of x is within 0-27. 0: Disable 1: Active
31:28	Reserved		

22.6.3.6 Register x of CAN filter group x (CAN_FiBANKx) (i = 0..27； x=1..2)

Offset address: 0x240..0x31C

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
31:0	FBIT[31:0]	R/W	Filter Bits Setup Identifier list mode: 0: FBITx bit is dominant bit 1: FBITx bit is recessive bit Identifier mask bit mode: 0: FBITx is not used for comparison 1: FBITx must match Note: The value of x is 0~31, indicating the bit number of FBIT.

Note: The product has 14 filter groups, i=0..27. Each set of filters consists of two 32-bit registers and CAN_FiBANK[2:1]. The corresponding filter registers can be modified only when the corresponding FACTx bit of CAN_FACT register is cleared or the FINITEN bit of CAN_FCTRL register is 1.

23 USB OTG_FS

23.1 Introduction

OTG_FS can support both host and slave functions to comply with the On-The-Go supplementary standard of USB 2.0 specification, and can also be configured as " Host only" or "Slave only" mode, to fully comply with USB 2.0 specification, and support host negotiation protocol (HNP) and session request protocol (SRP). In host mode, it supports full-speed (FS, 12Mb/s) and low-speed (LS, 1.5Mb/s) transmission, and in slave mode, it only supports full-speed (FS, 12Mb/s) transmission.

It should be noted that when using the device mode of USB OTG_FS for communication, a pull-up resistor needs to be configured. When using it, the user can activate the internal resistor by connecting a high level to the PA9 pin, or connect an external pull-up resistor.

23.2 OTG_FS global register address mapping

Table 75 OTG_FS Global Register Address Mapping

Register name	Description	Offset address
OTG_FS_GCTRLSTS	Full-speed OTG control state register	0x00
OTG_FS_GINT	Full-speed OTG interrupt register	0x04
OTG_FS_GAHBCFG	Full-speed OTG AHB configuration register	0x08
OTG_FS_GUSBCFG	Full-speed OTG USB configuration register	0x0C
OTG_FS_GRSTCTRL	Full-speed OTG reset control register	0x10
OTG_FS_GCINT	Full-speed OTG module interrupt register	0x14
OTG_FS_GINTMASK	Full-speed OTG module interrupt mask register	0x18
OTG_FS_GRXSTS	Full-speed OTG read debug receive state register	0x1C
OTG_FS_GRXSTSP	Full-speed OTG state read and pop register	0x20
OTG_FS_GRXFIFO	Full-speed OTG receive FIFO size register	0x24
OTG_FS_GTXFCFG	Full-speed OTG TXFIFIO configuration register	0x28
OTG_FS_GNPTXFQSTS	Full-speed OTG non-periodic TXFIFIO queue state register	0x2C
OTG_FS_GGCCFG	Full-speed OTG general module configuration register	0x38
OTG_FS_GCID	Full-speed OTG module ID register	0x3C
OTG_FS_GHPTXFSIZE	Full-speed OTG host periodic TXFIFO size register	0x100

Register name	Description	Offset address
OTG_FS_DTXFIFO1	Full-speed OTG device IN endpoint TXFIFO size register 1	0x104
OTG_FS_DTXFIFO2	Full-speed OTG device IN endpoint TXFIFO size register 2	0x108
OTG_FS_DTXFIFO3	Full-speed OTG device In endpoint TXFIFO size register 3	0x10C

23.3 OTG_FS global register functional description

23.3.1 Full-speed OTG control state register (OTG_FS_GCTRLSTS)

Offset address: 0x00

Reset value: 0x0001 0000

Field	Name	R/W	Description
0	SREQSUC	R	Session Request Success 0: Session request fails 1: Session request succeeds Note: It can be used only in device mode
1	SREQ	R/W	Session Request 0: No request session 1: Request session When HNSUCCHG bit of OTG_FS_GINT register is set, this bit will be cleared by writing 0. This bit will be cleared to 0 when HNSUCCHG is cleared to 0. When USB 1.1 full-speed serial transceiver interface is used for session request, wait for V_{BUS} to discharge to 0.2 V after the BSVD bit of the register is cleared to 0. The discharge time may be different according to different PHY. Note: It can be used only in device mode
7:2	Reserved		
8	HNSUC	R	Host Negotiation Success This bit will be cleared to 0 when HNPREQ of this register is set to 1 0: Host negotiation fails 1: Host negotiation succeeds Note: It can be used only in device mode
9	HNPREQ	R/W	Host Negotiation Protocol Request (HNP Request) 0: Not transmit HNP request 1: Transmit HNP request When HNSUCCHG bit of OTG_FS_GINT register is set, this bit will be cleared by writing 0. This bit will be cleared to 0 when HNSUCCHG is cleared to 0. Note: It can be used only in device mode
10	HHNPEN	R/W	Host Set HNP Enable 0: Disable 1: Enable

Field	Name	R/W	Description
			Note: It can be used only in master mode
11	DHNPEN	R/W	Device HNP Enable 0: Disable 1: Enable Note: It can be used only in device mode
15:12	Reserved		
16	CIDSTS	R	Connector ID Status 0: OTG_FS controller is in Device A mode 1: OTG_FS controller is in Device B mode Note: It can be used in both device and master modes
17	LSDEBT	R	Long/Short Debounce Time Indicate the detected debounce time. The long debounce time is used for physical connection, and the short debounce time is used for software (program) connection. 0: Long debounce time (100ms+2.5μs) 1: Short debounce time (2.5μS) Note: It can be used only in master mode
18	ASVD	R	A-Session Valid 0: Invalid 1: Valid Note: It can be accessed only in master mode
19	BSVD	R	B-Session Valid In OTG mode, this bit is used to confirm whether the device is in connected status. 0: Invalid 1: Valid Note: It can be accessed only in device mode
31:20	Reserved		

23.3.2 Full-speed OTG interrupt register (OTG_FS_GINT)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
1:0	Reserved		
2	SEFLG	RC_W1	Session End Flag When V_{BUS}<0.8V, it means that V_{BUS} is not used for B-session, and this bit will be set to 1.
7:3	Reserved		
8	SREQSUCCHG	RC_W1	Session Request Success Bit Change If the value of SREQSUC bit changes, this bit will be set to 1.
9	HNSUCCHG	RC_W1	Host Negotiation Success Bit Change If the value of HNSUC bit changes, this bit will be set to 1.
16:10	Reserved		

Field	Name	R/W	Description
17	HNFLG	RC_W1	Host Negotiation Flag When USB host negotiation request is detected, this bit will be set to 1.
18	ADTOFLG	RC_W1	A-Device Timeout Flag If this bit is set to 1, it indicates timeout when A-device is waiting for B-device to connect.
19	DEBDFLG	RC_W1	Debpouncce Done Flag When the equipment is connected and debounce is completed, this bit shall be set to 1; when an interrupt is generated, the USB will be reset. This bit is valid only when HNPEN and SRPEN bits of OTG_FS_GUSBCFG register are set to 1. Note: It can be accessed only in master mode
31:20	Reserved		

23.3.3 Full-speed OTG AHB configuration register (OTG_FS_GAHBCFG)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	GINTMASK	R/W	Global Interrupt Mask 0: Mask global interrupt 1: Unmask global interrupt
6:1	Reserved		
7	TXFEL	R/W	TXFIFO Empty Level In device mode: 0: TXFE interrupt means that IN endpoint TXFIFIO is half-empty 1: TXFE interrupt means that IN endpoint TXFIFIO is all-empty In master mode: 0: NPTXFEM interrupt means that non-periodic TXFIFO is half-empty 1: NPTXFEM interrupt means that non-periodic TXFIFO is all-empty
8	PTXFEL	R/W	Periodic TXFIFO Empty Level 0: PTXFE interrupt means that periodic TXFIFIO is half-empty 1: PTXFE interrupt means that periodic TXFIFIO is all-empty Note: It can be accessed only in master mode
31:9	Reserved		

23.3.4 Full-speed OTG USB configuration register (OTG_FS_GUSBCFG)

Offset address: 0x0C

Reset value: 0x0000 1440

Field	Name	R/W	Description
2:0	SEFLG	R/W	FS Timeout Calibrate The additional delay of PHY includes the number of PHY clocks and FS timeout interval. The status of data line may be different for different PHY.. The timeout value of OTG_FS is 16~18-bit time.

Field	Name	R/W	Description
6:3	Reserved		
7	FSSTSEL	W	Full-Speed Serial Transceiver Select 0: USB2.0 full-speed ULPI PHY 1: USB1.1 full-speed serial transceiver This bit is always 1.
8	SRPEN	R/W	SRP Enable 0: Disable 1: Enable If the SRP function is disabled, connecting the device cannot be requested to activate V_{BUS} and the session cannot be started.
9	HNPEN	R/W	HNP Enable 0: Disable 1: Enable
13:10	TRTIM	R/W	USB Turnaround Time f_{PHYCLK}=48MHZ, in f_{PHYCLK}. TRTIM=4×f_{AHBCLK}+f_{PHYCLK} Example: When f_{AHBCLK}=72MHz, TRTIM will be set to 7.
28:14	Reserved		
29	FHMODE	R/W	Force Host Mode 0: Normal mode 1: Master mode
30	FDMODE	R/W	Force Device Mode 0: Normal mode 1: Device mode
31	CTXP	R/W	Corrupt TX Packet Debug bit, which cannot be set to 1 Note: It can be accessed in both device and master mode

23.3.5 Full-speed OTG reset register (OTG_FS_GRSTCTRL)

Offset address: 0x10

Reset value: 0x8000 0000

Field	Name	R/W	Description
0	CSRST	R/S	Core Soft Reset This bit controls HCLK and PCLK reset Clear each interrupt and all control state register bits to 0 except the followings: - GCLK bit in OTG_FS_PCGCTRL - PCLKSTOP bit in OTG_FS_PCGCTRL - PHYCLKSEL bit in OTG_FS_HCFG - DSPDSEL bit in OTG_FS_DCFG Reset the AHB slave to the idle state and clear TXFIFO and RXFIFO. When the AHB transmission ends, all transactions of AHB shall be terminated as soon as possible and all transactions on USB shall be terminated immediately.

Field	Name	R/W	Description
			Software reset is used generally in either of the following situations: Software development period. After the user dynamically changes the PHY selection bit in the USB configuration register listed above. When the user changes the PHY, the corresponding clock will be selected for the PHY and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset so as to ensure normal operation.
1	HSRST	R/S	HCLK Soft Reset This bit is used to refresh the control logic of AHB clock domain. When clearing this interrupt, the corresponding mask interrupt state control bit shall be cleared; when the interrupt state bit is not cleared to zero, the event state after this bit is set to 1 can be read.
2	HFCNTRST	R/S	Host Frame Counter Reset Reset the frame counter in the host by writing this bit, and the SOF frame number transmitted subsequently is 0. Note: It can be accessed only in master mode.
3	Reserved		
4	RXFFLU	R/S	RXFIFO Flush This bit is used to refresh the whole RXFIFO. Before writing to this bit, it is required to ensure that the module does not perform read and write operation to RXFIFO. Only after this bit is cleared to 0, can other operations be performed (usually need to wait for 8 clock cycles).
5	TXFFLU	R/S	TXFIFO Flush This bit is used to refresh one or the whole TXFIFO. Before writing to this bit, it is required to ensure that the module does not perform read and write operation to TXFIFO.
10:6	TXFNUM	R/W	TXFIFO Number Refresh the FIFO number with TXFIFO refresh bits, and these bits can only be changed after the refresh TXFFIO is cleared to 0. In master mode: 00000: Refresh non-periodic TXFIFO 00001: Refresh periodic TXFIFO 10000: Refresh all TXFIFO In device mode: 00000: Refresh TXFIFO 0 00001: Refresh TXFIFO 1 …… 00101: Refresh TXFIFO 15 10000: Refresh all TXFIFO
30:11	Reserved		
31	AHBMIDL	R	AHB Master Idle This bit indicates whether the AHB master device is idle.

23.3.6 Full-speed OTG module interrupt register (OTG_FS_GCINT)

Offset address: 0x14

Reset value: 0x1400 8022

In order to avoid generating interrupts before initialization, the software must clear this register to zero before enabling the interrupt bit.

Field	Name	R/W	Description
0	CURMOSEL	R	Current Mode of Operation Select 0: Device mode 1: Master mode
1	MMIS	RC_W1	Mode Mismatch Interrupt This bit will be set to 1 when accessing the following registers: Access the master mode register in device mode Access the device mode register in master mode
2	OTG	R	OTG Interrupt When this bit is set to 1, it indicates that an OTG protocol event has occurred. By reading OTG_FS_GINT register, determine the event that causes the OTG interrupt. This bit can be cleared to zero only after the corresponding bit of the register is cleared.
3	SOF	RC_W1	Start of Frame Interrupt When this bit is set: In master mode, it indicates that USB has transmitted one SOF (FS) or Keep-Alive (LS); In device mode, it indicates that USB has received one SOF, and the current frame number can be obtained by reading the device state register. An interrupt will be generated only when running in FS mode.
4	RXFNONE	R	RXFIFO Nonempty Interrupt This bit indicates that there are still packets in RXFIFO that have not been read.
5	NPTXFEM	R	Nonperiodic TXFIFO Empty Interrupt This interrupt will be triggered when the non-periodic TXFIFO is not empty and there is space for writable entries in the request queue. Note: It can be accessed only in master mode
6	GINNPNAKE	R	Global IN Non-periodic NAK Effective Interrupt This bit indicates that GINAKSET bit of OTG_FS_DCTRL register is valid; this bit can be cleared by clearing GINAKCLR bit of OTG_FS_DCTRL register. As the priority of STALL is higher than that of NAK bit, generation of this interrupt cannot mean that USB has sent NAK signal. Note: It can be accessed only in device mode
7	GONAKE	R	Global OUT NAK Effective Interrupt This bit indicates that GONAKSET bit of OTG_FS_DCTRL register is valid; this bit can be cleared by clearing GONALCLR bit of OTG_FS_DCTRL. Note: It can be accessed only in device mode
9:8	Reserved		
10	ESUS	RC_W1	Early Suspend Interrupt When USB has been idle for 3ms, this bit will be set to 1. Note: It can be accessed only in device mode

Field	Name	R/W	Description
11	USBSUS	RC_W1	USB Suspend Interrupt When USB suspending is detected, this bit will be set to 1; when USB has been idle for 3ms, it will enter pending state. Note: It can be accessed only in device mode
12	USBRST	RC_W1	USB Reset Interrupt This bit will be set to 1 when reset is detected on USB. Note: It can be accessed only in device mode
13	ENUMD	RC_W1	Enumeration Done Interrupt This bit will be set to 1 when speed enumeration is completed. Note: It can be accessed only in device mode
14	ISOPD	RC_W1	Isochronous OUT Packet Dropped Interrupt When the RXFIFO space is insufficient and the module cannot write synchronous OUT data packet to RXFIFO, this bit will be set to 1. Note: It can be accessed only in device mode
15	EOPF	RC_W1	End of Periodic Frame Interrupt This bit indicates that the current frame has reached the period specified by PFITV bit of OTG_FS_DCFG register. Note: It can be accessed only in device mode
17:16	Reserved		
18	INEP	R	IN Endpoint Interrupt This bit will be set to 1 when a pending interrupt occurs to one IN endpoint Determine the number of IN endpoint to which an interrupt occurs by reading OTG_FS_DAEPINT register, and determine the causes of the interrupt by reading OTG_FS_DIEPINTx register. To clear this bit, first clear the corresponding state bit of OTG_FS_DIEPINTx register. Note: It can be accessed only in device mode
19	ONEP	R	OUT Endpoint Interrupt This bit will be set to 1 when a pending interrupt occurs to one OUT endpoint Determine the number of OUT endpoint to which an interrupt occurs by reading OTG_FS_DAEPINT register, and determine the causes of the interrupt by reading OTG_FS_DOEPINTx register. To clear this bit, first clear the corresponding state bit of OTG_FS_DOEPINTx register. Note: It can be accessed only in device mode
20	IIINTX	RC_W1	Incomplete Isochronous IN Transfer Interrupt This bit will be set to 1 when the transmission on at least one synchronous IN endpoint in the current frame is not completed. This interrupt is triggered at the same time with EOPF. Note: It can be accessed only in device mode

Field	Name	R/W	Description
21	IP_OUTTX	RC_W1	Incomplete Periodic Transfer Interrupt When this bit is set to 1, the interrupts indicated by it are different in different modes. In the master mode, if the periodic transaction scheduled to be completed in the current frame is still pending (i.e. incomplete), the incomplete periodic transmission interrupt will be triggered. In device mode, when the transmission on at least one synchronous OUT endpoint in the current frame is not completed, interrupt of incomplete OUT synchronous transmission will be triggered, and this interrupt will be triggered at the same time with EOPF.
23:22	Reserved		
24	HPORT	R	Host Port Interrupt This bit will be set to 1 when the state of full-speed OTG controller port changes in master mode. Note: It can be accessed only in master mode
25	HCHAN	R	Host Channels Interrupt This bit will be set to 1 when a pending interrupt is generated on host channel. Note: It can be accessed only in master mode
26	PTXFE	R	Periodic TXFIFO Empty Interrupt This interrupt will be triggered when the periodic TXFIFO is empty and there is space for writable entries in the request queue. Note: It can be accessed only in master mode
27	Reserved		
28	CINSTSCHG	RC_W1	Connector ID Status Change Interrupt This bit will be set to 1 when the state of connector ID line changes. Note: It can be accessed in both master and device mode
29	DEDIS	RC_W1	Device Disconnect Interrupt This bit will be set to 1 when device disconnection is detected. Note: It can be accessed only in master mode
30	SREQ	RC_W1	Session Request/New Session Interrupt In different modes, the conditions for triggering this interrupt are: Session request is detected in master mode In device mode, V_{BUS} is within the range of B-device
31	RWAKE	RC_W1	Resume/Remote Wakeup Interrupt In different modes, the conditions for triggering this interrupt are: Remote wakeup signal is detected on USB in master mode Resume signal is detected on USB bus in device mode

23.3.7 Full-speed OTG module interrupt mask register (OTG_FS_GINTMASK)

Offset address: 0x18

Reset value: 0x0000 0000

This register is used to mask the interrupt, but the corresponding bit of the interrupt register will still be set to 1.

Field	Name	R/W	Description
0	Reserved		
1	MMISM	R/W	Mode Mismatch Interrupt Mask 0: Mask 1: Not mask
2	OTGM	R/W	OTG Interrupt Mask 0: Mask 1: Not mask
3	SOFM	R/W	Frame Start Interrupt Mask 0: Mask 1: Not mask
4	RXFNONEM	R/W	RXFIFO Nonempty Interrupt Mask 0: Mask 1: Not mask
5	NPTXFEMM	R/W	Nonperiodic TXFIFO Empty Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in master mode
6	GINNPNAKEM	R/W	Global IN Nonperiodic NAK Effective Interrupt Make 0: Mask 1: Not mask Note: It can be accessed only in device mode
7	GONAKEM	R/W	Global OUT NAK Effective Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
9:8	Reserved		
10	ESUSM	R/W	Early Suspend Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
11	USBSUSM	R/W	USB Suspend Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
12	USBRSTM	R/W	USB Reset Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
13	ENUMDM	R/W	Enumeration Done Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
14	ISOPDM	R/W	Isochronous OUT Packet Dropped Interrupt Mask 0: Mask

Field	Name	R/W	Description
			1: Not mask Note: It can be accessed only in device mode
15	EOPFM	R/W	End of Periodic Frame Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
16	Reserved		
17	EPMISM	R/W	Endpoint Mismatch Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
18	INEPM	R/W	IN Endpoint Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
19	OUTEPM	R/W	OUT Endpoint Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
20	IIINTXM	R/W	Incomplete Isochronous IN Transfer Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
21	IP_OUTTXM	R/W	Incomplete Periodic Transfer Interrupt Mask In master mode, this bit controls whether to mask incomplete periodic transmission interrupt. In device mode, this bit controls whether to mask the incomplete OUT synchronous transmission interrupt. 0: Mask 1: Not mask
23:22	Reserved		
24	HPORTM	R	Host Port Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in master mode
25	HCHM	R/W	Host Channels Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in master mode
26	PTXFEM	R/W	Periodic TXFIFO Empty Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in master mode
27	Reserved		

Field	Name	R/W	Description
28	CIDSTSCM	R/W	Connector ID Status Change Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed in both master and device mode
29	DEDISM	R/W	Device Disconnect Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed only in device mode
30	SREQM	R/W	Session Request/New Session Interrupt Mask 0: Mask 1: Not mask
31	RWAKEM	R/W	Resume/Remote Wakeup Interrupt Mask 0: Mask 1: Not mask Note: It can be accessed in both master and device mode

23.3.8 Full-speed OTG read debug receive state register/full-speed OTG state read and pop register (OTG_FS_GRXSTS/OTG_FS_GRXSTSP)

Read offset address: 0x1C

Pop offset address: 0x20

Reset value: 0x4B1E 720C

Master mode

Field	Name	R/W	Description
3:0	CHNUM	R	Channel Number This bit indicates the received data is transmitted by which channel.
14:4	BCNT	R	Byte Count This bit indicates the byte count of received IN data packet.
16:15	DPID	R	Data Packet ID This bit indicates the received data packet ID (PID) 00：DATA0 10：DATA1 01：DATA2 11：MDATA
20:17	PSTS	R	Packet Status This bit indicates the status of the received data packet. 0010: Received IN data packet 0011: IN transmission completed 0101: Data synchronization error 0111: Channel stop Others: Reserved
31:21	Reserved		

Device mode

Field	Name	R/W	Description
3:0	EPNUM	R	Endpoint Number This bit indicates the received data is transmitted by which endpoint.
14:4	BCNT	R	Byte Count This bit indicates the byte count of received data packet
16:15	DPID	R	Data PID This bit indicates the received data packet ID (PID) 00：DATA0 10：DATA1 01：DATA2 11：MDATA
20:17	PSTS	R	Packet Status This bit indicates the status of received data packet 0001: Global OUT NAK 0010: Received OUT data packet 0011: OUT transmission completed 0100: SETUP event completed 0110: Received SETUP data packet Others: Reserved
24:21	FNUM	R	Frame Number These bits are valid when synchronous OUT endpoint is supported. These bits are the 4 least significant bits of the packet frame number received on the USB
31:25	Reserved		

23.3.9 Full-speed OTG receive FIFO size register (OTG_FS_GRXFIFO)

Offset address: 0x24

Reset value: 0x0000 0200

Field	Name	R/W	Description
15:0	RXFDEP	R/W	RXFIFO Depth RXFIFO is in word, and the depth range is: 16~256.
31:16	Reserved		

23.3.10 Full-speed OTG TXFIFO configuration register (OTG_FS_GTXFCFG)

Offset address: 0x28

Reset value: 0x0200 0200

Master mode

Field	Name	R/W	Description
15:0	NPTXSA	R/W	Nonperiodic TXFIFO RAM Start Address This bit indicates the start address of non-periodic TXFIFO RAM.
31:16	NPTXFDEP	R/W	Nonperiodic TXFIFO Depth TXFIFO is in word, and the depth range is: 16~256.

Device mode

Field	Name	R/W	Description
15:0	EPTXSA	R/W	Endpoint0 TXFIFO RAM Start Address This bit indicates the start address of TXFIFO RAM of endpoint 0.
31:16	EPTXFDEP	R/W	Endpoint0 TXFIFO Depth TXFIFO is in word, and the depth range is: 16~256.

23.3.11 Full-speed OTG non-periodic TXFIFO queue state register (OTG_FS_GNPTXFQSTS)

Offset address: 0x2C

Reset value: 0x0008 0200

Field	Name	R/W	Description
15:0	NPTXFSA	R	Nonperiodic TXFFIO Space Available These bits indicate the size of available space of non-periodic TXFIFO. (In 32-bit words) 0x0: Non-periodic TXFIFO is full 0x1: 1 word 0x2: 2 words ….. 0xn: n words are available (0≤n≤256) Others: Reserved
23:16	NPTXRSA	R	Nonperiodic Transmit Request Space Available This bit indicates the available space size of non-periodic transmit request queue. In master mode: Save IN and OUT requests In device mode: There is only IN request 0x0: The queue is full 0x0: 1 position 0x2: 2 positions ….. 0xn: n positions are available (0≤n≤8) Others: Reserved
30:24	NPTXRQ	R	Nonperiodic Transmit Request Queue Bit 24: Terminate (last data selected for channel/endpoint) Bit [26:25]: 00: IN/OUT token 01: The transmit data packet length is 0 (IN in device mode/OUT in master mode) 10: PING/CPLIT token 11: Stop channel instruction Bit [30:27]: Channel/endpoint number
31	Reserved		

23.3.12 Full-speed OTG general module configuration register (OTG_FS_GGCCFG)

Offset address: 0x38

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	Reserved		
16	PWEN	R/W	Power Down Enable This bit is used to activate the transceiver. 0: Power down is activated 1: Power down inactivated (activate the transceiver)
17	Reserved		
18	ADVBSEN	R/W	A Device V_{BUS} Sensing Enable 0: Disable 1: Enable
19	BDVBSEN	R/W	B Device V_{BUS} Sensing Enable 0: Disable 1: Enable
20	SOFPOUT	R/W	SOF Pulse Available on PAD Output This bit selects whether SOF pulse can be output from PAD. 0: No 1: Yes
31:21	Reserved		

23.3.13 Full-speed OTG module ID register (OTG_FS_GCID)

Offset address: 0x3C

Reset value: 0x0000 1000

Field	Name	R/W	Description
31:0	PID	R/W	Product ID Product ID can be programmed by this bit.

23.3.14 Full-speed OTG host periodic TXFIFO size register (OTG_FS_GHPTXFSIZE)

Offset address: 0x100

Reset value: 0x0200 0600

Field	Name	R/W	Description
15:0	HPDTXFSA	R/W	Host Periodic TXFIFO Start Address
31:16	HPDTXFDEP	R/W	Host Periodic TXFIFO Depth TXFIFO is in word, and the minimum value is 16.

23.3.15 Full-speed OTG device IN endpoint TXFIFO size register x (OTG_FS_DIEPTXFIFOx) (x=1~3)

Offset address: 0x104+4(x-1)

Reset value: x=1：0x0200 0400

x=2：0x0200 0600

x=3：0x0200 0800

x is FIFO number.

Field	Name	R/W	Description
15:0	INEPTXFRSA	R/W	IN Endpoint TXFIFOx Transmit RAM Start Address These bits indicate the start address of the IN endpoint TXFIFOx RAM and need to be aligned with the 32-bit memory.
31:16	INEPTXFDEP	R/W	IN Endpoint TXFIFO Depth TXFIFO is in word, and the minimum value is 16.

23.4 OTG_FS host mode register address mapping

Table 90 OTG_FS Host Mode Register Address Mapping

Register name	Description	Offset address
OTG_FS_HCFG	Full-speed OTG host configuration register	0x400
OTG_FS_HFIVL	Full-speed OTG host frame interval register	0x404
OTG_FS_HFIFM	Full-speed OTG host frame information register	0x408
OTG_FS_HPTXSTS	Full-speed OTG host periodic transmission state register	0x410
OTG_FS_HACHINT	Full-speed OTG host all-channel interrupt register	0x414
OTG_FS_HACHIMASK	Full-speed OTG host all-channel interrupt mask register	0x418
OTG_FS_HPORTCSTS	Full-speed OTG host port control state register	0x440
OTG_FS_HCHX	Full-speed OTG host channel-X characteristics register (X=0…7)	0x500+20*X
OTG_FS_HCHINTX	Full-speed OTG host channel-X interrupt register (X=0…7)	0x508+20*X
OTG_FS_HCHIMASKX	Full-speed OTG host channel-X interrupt mask register (X=0…7)	0x50C+20*X
OTG_FS_HCHTSIZEX	Full-speed OTG host channel-X transmission size register (X=0…7)	0x510+20*X

23.5 OTG_FS host mode register functional description

23.5.1 Full-speed OTG host configuration register (OTG_FS_HCFG)

Offset address: 0x400

Reset value: 0x0020 0000

Field	Name	R/W	Description
1:0	PHYCLKSEL	R/W	FS/LS PHY Clock Select In FS mode: 01: PHY clock is 48MHz Others: Reserved In LS mode: 00: Reserved 01: PHY clock is 48MHz 10: PHY clock is 6MHz 11: Reserved Note: Software reset is required after the value of this bit is changed.
2	FSSPT	R	FS Support After the host is connected to the device, select whether the host follows the maximum speed supported by the device. If this bit is set to 1, even if the device supports HS mode, the host supports FS at most. 0: The host can support HS/FS/LS 1: The host only supports FS/LS
31:3	Reserved		

23.5.2 Full-speed OTG host frame interval register (OTG_FS_HFIVL)

Offset address: 0x404

Reset value: 0x0000 17D7

This register can be edited only after the port (PEN bit of OTG_FS_HPORTCSTS register is set to 1) is enabled.

Field	Name	R/W	Description
15:0	FIVL	R/W	Frame Interval This bit is used to control the time interval between two continuous SOF (FS), micro-SOF (HS), and Keep-Alive (LS). Time interval=frame duration×PHY clock
31:16	Reserved		

23.5.3 Full-speed OTG host frame information register (OTG_FS_HFIFM)

Offset address: 0x408

Reset value: 0x2B72 0000

Field	Name	R/W	Description
15:0	FNUM	R	Frame Number This bit is used to indicate the current frame number. This bit will be cleared to zero when reaching 0x3FFF.
31:16	FRTIME	R	Frame Remaining Time This bit is used to indicate the current remaining time of frame. The initial value is the value of OTG_FS_HFIVL, and every time passing one PHY clock, the value of this bit will decrease by 1, and when reaching 0, this bit will reload the value of frame interval.

23.5.4 Full-speed OTG host periodic transmission state register (OTG_FS_HPTXSTS)

Offset address: 0x410

Reset value: 0x0008 0200

Field	Name	R/W	Description
15:0	FSPACE	R/W	Periodic Transmit Data FIFO Available Space This bit indicates the idle space of periodic TXFIFO (in 32-bit word). 0x0: TXFIFO is full 0x1: 1 word 0x2: 2 words 0xn: n words are available (0<n<512) Others: Reserved
23:16	QSPACE	R	Periodic Transmit Request Queue Available Space This bit indicates the available space of periodic transmit request queue. 0x0: The queue is full 0x1: 1 position 0x2: 2 positions 0xn: n positions are available (0<n<8) Others: Reserved
31:24	QTOP	R	Top of the Periodic Transmit Request Queue This bit indicates the transaction being processed in periodic transmit request queue. [24]: End [26:25]: Type 00：IN/OUT 01: Zero-length data packet 11: Disable channel command [30:27]: Channel/endpoint number [31]: Odd/even frame 0: Even frame 1: Odd frame

23.5.5 Full-speed OTG host all-channel interrupt register (OTG_FS_HACHINT)

Offset address: 0x414

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	ACHINT	R	All Channels Interrupts No. X bit represents interrupt of Channel X. Up 16 channels.
31:16	Reserved		

23.5.6 Full-speed OTG host all-channel interrupt mask register (OTG_FS_HACHIMASK)

Offset address: 0x418

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	ACHIMASK	R/W	All Channels Interrupts Mask No. X bit represents interrupt mask of Channel X. Up 16 channels. 0: Mask 1: Not mask
31:16	Reserved		

23.5.7 Full-speed OTG host port control state register (OTG_FS_HPORTCSTS)

Offset address: 0x440

Reset value: 0x0000 0C00

Field	Name	R/W	Description
0	PCNNTFLG	R	Port Connect Flag 0: The port is not connected 1: Port connected
1	PCINTFLG	RC_W1	Port Connect Interrupt Flag This bit will be set to 1 when the port is connected to the device.
2	PEN	RC_W0	Port Enable After the port resets the sequence, the program cannot write to this bit, and can only enable the port through the module. If this bit is cleared to zero, the port will be disabled. 0: Disable 1: Enable
3	PENCHG	RC_W1	PEN Bit Change This bit will be set to 1 when PEN bit of this register changes.
4	POVC	R	Port Overcurrent This bit indicates whether this port is overloaded. 0: No overload 1: Overload
5	POVCCHG	RC_W1	POVC Bit Change This bit will be set to 1 when POVC bit changes.
6	PRS	R/W	Port Resume 0: Resume signal is not driven 1: Resume signal is driven
7	PSUS	R/S	Port Suspend 0: Port is not suspended 1: Port is suspended
8	PRST	R/W	Port Reset The prot can start reset only when this bit is set to 1 for over 10ms. 0: Not in reset state 1: In reset state
9	Reserved		

Field	Name	R/W	Description
11:10	PDLSTS	R	Port Data Line Status This bit indicates the logic level of the USB data line at this time. [10] bit means OTG_FS_FS_DP [11] bit means OTG_FS_FS_DM
12	PP	R/W	Port Power This bit controls the power-on of the port. If there is overload, the port will power down (clear 0). 0: Power down 1: Power on
16:13	PTSEL	R/W	Port Test Mode Select 0000: Test is disabled 0001：Test_J 0010：Test_K 0011：Test_SE0_NAK 0100：Test_Packet 0101：Test_Force_Enable Others: Reserved
18:17	PSPDSEL	R	Port Speed Select 01: Full speed 10: Low speed 11: Reserved
31:19	Reserved		

23.5.8 Full-speed OTG host channel -X characteristics register (OTG_FS_HCHX) (X=0…7)

Offset address: 0x500+20*X

Reset value: 0x0000 0000

Field	Name	R/W	Description
10:0	MAXPSIZE	R/W	Maximum Data Packet Size This bit indicates the maximum data packet size of the device endpoint connected to the host.
14:11	EDPNUM	R/W	Endpoint Number This bit indicates the number of the device endpoint connected to the host.
15	EDPDRT	R/W	Endpoint Direction 0：OUT 1：IN
16	Reserved		
17	LSDV	R/W	Low-speed Device This bit indicates the low-seed device is connected.
19:18	EDPTYP	R/W	Endpoint Type This bit is used to select the transmission type of endpoint. 00: Control 01: Synchronous 10: Batch

Field	Name	R/W	Description
			11: Interrupt
21:20	CNTSEL	R/W	Count Function Select In this register, this bit is only used to indicate the number of transactions that must be executed by the periodic endpoint per frame. 00: Reserved 01: 1 10: 2 11: 3
28:22	DVADDR	R/W	Device Address This bit indicates the device address connected to the host.
29	ODDF	R/W	Odd Frame This bit controls whether the OTG host transmits in odd frame. 0: Even frame 1: Odd frame Note: It applies only to periodic transactions.
30	CHINT	R/S	Channel Interrupt 0: Not interrupt 1: Stop transmitting data through the channel
31	CHEN	R/S	Channel Enable 0: Disable 1: Enable

23.5.9 Full-speed OTG host channel -X interrupt register (OTG_FS_HCHINTX) (X=0…7)

Offset address: 0x508+20*X

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TSFCMPN	RC_W1	Transfer Complete Normally
1	TSFCMPAN	RC_W1	Transfer Complete Abnormally
2	Reserved		
3	RXSTALL	RC_W1	STALL Response Received Interrupt
4	RXNAK	RC_W1	NAK Response Received Interrupt
5	RXTXACK	RC_W1	ACK Response Received/Transmitted Interrupt
6	Reserved		
7	TERR	RC_W1	Transaction Error Indicate that one of the following error occurs: CRC failure Timeout Bit stuffing error EOP error
8	BABBLE	RC_W1	Babble Error

Field	Name	R/W	Description
9	FOVR	RC_W1	Frame Overrun Error
10	DTOG	RC_W1	Data Toggle Error
31:11	Reserved		

23.5.10 Full-speed OTG host channel -X interrupt mask register (OTG_FS_HCHIMASKX) (X=0…7)

Offset address: 0x50C+20*X

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TSFCMPNM	R/W	Transfer Complete Normally Mask 0: Mask 1: Not mask
1	TSFCMPANM	R/W	Transfer Complete Abnormally Mask 0: Mask 1: Not mask
2	Reserved		
3	RXSTALLM	R/W	STALL Response Received Interrupt Mask 0: Mask 1: Not mask
4	RXNAKM	R/W	NAK Response Received Interrupt Mask 0: Mask 1: Not mask
5	RXTXACKM	R/W	ACK Response Received/Transmitted Interrupt 0: Mask 1: Not mask
6	RXNYETM	R/W	NYET Response Received Interrupt Mask 0: Mask 1: Not mask
7	TERRM	R/W	Transaction Error Mask 0: Mask 1: Not mask
8	BABBLEM	R/W	Babble Error Mask 0: Mask 1: Not mask
9	FOVRM	R/W	Frame Overrun Error Mask 0: Mask 1: Not mask
10	DTOGM	R/W	Data Toggle Error Mask 0: Mask 1: Not mask
31:11	Reserved		

23.5.11 Full-speed OTG host channel -X transmission size register (OTG_FS_HCHTSIZEX) (X=0…7)

Offset address: 0x510+20*X

Reset value: 0x0000 0000

Field	Name	R/W	Description
18:0	TSFSIZE	R/W	Transfer Size For IN: The value of this bit is the size reserved for the transmission buffer, which is generally an integer multiple of the maximum data packet. For OUT: The value of this bit determines the number of bytes to be transmitted by the host.
28:19	PCKTCNT	R/W	Packet Count This bit indicates the value of the transmitted or received data packet. For each data packet transmitted, the value of this bit decreases by 1. When it decreases to 0, it means that the transmission is completed.
30:29	DATAPID	R/W	Data PID This bit is initial PID of data communication. 00：DATA0 01：DATA2 10：DATA1 11: MDATA (controlled transmission)/SETUP (uncontrolled transmission)
31	Reserved		

23.6 OTG_FS device mode register address mapping

Table 76 OTG_FS Device Mode Register Address Mapping

Register name	Description	Offset address
OTG_FS_DCFG	Full-speed OTG device configuration register	0x800
OTG_FS_DCTRL	Full-speed OTG device control register	0x804
OTG_FS_DSTS	Full-speed OTG device state register	0x808
OTG_FS_DINIMASK	Full-speed OTG device IN endpoint interrupt mask register	0x810
OTG_FS_DOUTIMASK	Full-speed OTG device OUT endpoint interrupt mask register	0x814
OTG_FS_DAEPINT	Full-speed OTG device all-endpoint interrupt register	0x818
OTG_FS_DAEPIMASK	Full-speed OTG device all-endpoint interrupt mask register	0x81C
OTG_FS_DVBUSDTIM	Full-speed OTG device VBUS release time register	0x828
OTG_FS_DVBUSPTIM	Full-speed OTG device VBUS pulse time register	0x82C
OTG_FS_DIEIMASK	Full-speed OTG device IN endpoint FIFO empty interrupt mask register	0x834

Register name	Description	Offset address
OTG_FS_DIEPCTRL0	Full-speed OTG device IN endpoint 0 control register	0x900
OTG_FS_DIEPCTRLx	Full-speed OTG device IN endpoint x control register	0x900+20x
OTG_FS_DIEPINTx	Full-speed OTG device IN endpoint x interrupt register (x=0...3)	0x908+20x
OTG_FS_DIEPTRS0	Full-speed OTG device IN endpoint 0 transmission size register	0x910
OTG_FS_DIEPTRSx	Full-speed OTG device IN endpoint x transmission size register (x=1…3)	0x910+20x
OTG_FS_DITXFSTSx	Full-speed OTG device IN endpoint x TXFIFO state register (x=0...3)	0x918+20x
OTG_FS_DOEPCTRL0	Full-speed OTG device OUT endpoint 0 control register	0xB00
OTG_FS_DOEPCTRLx	Full-speed OTG device OUT endpoint x control register (x=1…3)	0xB00+20x
OTG_FS_DOEPINTx	Full-speed OTG device OUT endpoint x interrupt register (x=0...3)	0xB08+20x
OTG_FS_DOEPTRS0	Full-speed OTG device OUT endpoint 0 transmission size register	0xB10
OTG_FS_DOEPTRSx	Full-speed OTG device OUT endpoint x transmission size register (x=1…3)	0xB10+20x

23.7 OTG_FS device mode register functional description

23.7.1 Full-speed OTG device configuration register (OTG_FS_DCFG)

Offset address: 0x800

Reset value: 0x0020 0000

Field	Name	R/W	Description
1:0	DSPDSEL	R/W	Device Speed Select This bit selects the maximum enumeration speed of the device connected to the host, 11：FS（48MHz） Others: Reserved
2	SENDOUT	R/W	Send the Received OUT Packet on Nonzero-length Status 0: After receiving the OUT data packet, transmit the data packet to the application program, and reply the handshake signal according to the NAK and STALL bits of the endpoint 1: After receiving the OUT data packet (non-zero length), reply the STALL handshake signal
3	Reserved		
10:4	DADDR	R/W	Device Address This bit is the address of storage device, and the parameters are from SetAddress command.

Field	Name	R/W	Description
12:11	PFITV	R/W	Periodic (Micro) Frame Interval This bit is configured to determine the time point of the periodic frame interrupt program, and can determine whether the synchronous communication of the frame is completed. 00: 80% of frame interval 01: 85% of frame interval 10: 90% of frame interval 11: 95% of frame interval
31:13	Reserved		

23.7.2 Full-speed OTG device control register (OTG_FS_DCTRL)

Offset address: 0x804

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	RWKUPS	R/W	Remote Wakeup Signaling The program wakes up the USB host by setting this bit to 1 to make the module exit the suspended state. Note: According to the agreement, after this bit is set to 1, it should be cleared to 0 within 1~15ms.
1	SDCNNT	R/W	Soft Disconnect Soft disconnect means that the host cannot receive the signal of "Device connected", and the device cannot receive the signal. 0: Normal. The host can receive device connection event 1: Soft disconnection
2	GINAKSTS	R	Global IN NAK Status This bit determines whether to reply the handshake signal according to the data availability in TXFIFO. 0: Yes 1: No, all non-periodic IN endpoints reply handshake signal
3	GONAKSTS	R	Global OUT NAK Status 0: Transmit the handshake signal according to FIFO state and NAK and STALL bit state 1: No data is received, and all data packets except the SETUP transaction reply the NAK signal
6:4	TESTSEL	R/W	Test Mode Select 000: Disable the test 001：Test_J 010：Test_K 011：Test_SE0_NAK 100：Test_Packet 101：Test_Force_Enable Others: Reserved
7	GINAKSET	W	Global IN NAK Setup Set the global non-periodic IN NAK to 1 to make the non-periodic IN endpoint transmit NAK signal. This bit can be set to 1 only when GINNPNAKE bit of OTG_FS_GCINT register is cleared to 0.

Field	Name	R/W	Description
8	GINAKCLR	W	Global IN NAK Clear Clear the global non-periodic IN NAK to 0.
9	GONAKSET	W	Global OUT NAK Setup Set the global OUT NAK to 1 to make OUT endpoint transmit NAK signal. This bit can be set to 1 only when GONAKE bit of OTG_FS_GCINT register is cleared to 0.
10	GONAKCLR	W	Global OUT NAK Clear Clear the global OUT NAK to 0.
11	POPROGCMP	R/W	Power-on Programming Complete This bit indicates that the programming operation is completed after the register is awakened.
31:12	Reserved		

23.7.3 Full-speed OTG device state register (OTG_FS_DSTS)

Offset address: 0x808

Reset value: 0x0000 0002

Field	Name	R/W	Description
0	SUSSTS	R	Suspend Status When the USB bus has been idle for more than 3ms, the module will enter the suspended state, and this bit will be set to 1. When there is an activity on the USB line or the module receives a remote wake-up signal, the module will exit the suspended state.
2:1	ENUMSPD	R	Enumerated Speed Enumeration speed of full-speed OTG after chirp sequence detection. 11: Full speed (48MHz) Others: Reserved
3	ERTERR	R	Erratic Error If any irregular error occurs, this bit will be set to 1. At this time, communication can be resumed only by performing soft disconnection.
7:4	Reserved		
21:8	SOFNUM	R	Frame Number of the Received SOF
31:22	Reserved		

23.7.4 Full-speed OTG device IN endpoint interrupt mask register (OTG_FS_DINIMASK)

Offset address: 0x810

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TSFCMPM	R/W	Transfer Completed Interrupt Mask 0: Mask 1: Not mask

Field	Name	R/W	Description
1	EPDISM	R/W	Endpoint Disable Interrupt Mask 0: Mask 1: Not mask
2	Reserved		
3	TOM	R/W	Timeout Interrupt Mask 0: Mask 1: Not mask
4	ITXEMPM	R/W	IN Token Received when TxFIFO Empty Mask 0: Mask 1: Not mask
5	IEPMMM	R/W	IN Token Received with Endpoint Mismatch Mask 0: Mask 1: Not mask
6	IEPNAKEM	R/W	IN Endpoint NAK Effective Mask 0: Mask 1: Not mask
31:7	Reserved		

23.7.5 Full-speed OTG device OUT endpoint interrupt mask register (OTG_FS_DOUTIMASK)

Offset address: 0x814

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TSFCMPM	R/W	Transfer Completed Interrupt Mask 0: Mask 1: Not mask
1	EPDISM	R/W	Endpoint Disable Interrupt Mask 0: Mask 1: Not mask
2	Reserved		
3	SETPCMPM	R/W	SETUP Phase Complete Mask 0: Mask 1: Not mask
4	OTXEMPM	R/W	OUT Token Received when Endpoint Disabled Mask 0: Mask 1: Not mask
31:5	Reserved		

23.7.6 Full-speed OTG device all-endpoint interrupt register (OTG_FS_DAEPINT)

Offset address: 0x818

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	INEPINT	R	All IN Endpoint Interrupts No. X bit indicates interrupt of IN endpoint X. Up to 16 IN endpoints.
31:16	OUTEPINT	R	All OUT Endpoint Interrupts No. X bit indicates interrupt of OUT endpoint (X-16). Up to 16 OUT endpoints.

23.7.7 Full-speed OTG device all-endpoint interrupt mask register (OTG_FS_DAEPIMASK)

Offset address: 0x81C

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	AINM	R/W	All IN Endpoint Interrupts Mask No. X bit indicates interrupt mask of IN endpoint X. Up to 16 IN endpoints. 0: Mask 1: Not mask
31:16	AOUTM	R/W	All OUT Endpoint Interrupts Mask No. X bit indicates interrupt mask of OUT endpoint (X-16). Up to 16 OUT endpoints. 0: Mask 1: Not mask

23.7.8 Full-speed OTG device V_{BUS} release time register (OTG_FS_DVBUSDTIM)

Offset address: 0x828

Reset value: 0x0000 17D7

Field	Name	R/W	Description
15:0	VBUSDTIM	R/W	Device V_{BUS} Discharge Time Discharge time after V_{BUS} impulses during SRP period. Value=Discharge time (number of PHY clock)/1024
31:16	Reserved		

23.7.9 Full-speed OTG device V_{BUS} pulse time register (OTG_FS_DVBUSPTIM)

Offset address: 0x82C

Reset value: 0x0000 05B8

Field	Name	R/W	Description
11:0	VBUSPTIM	R/W	Device V_{BUS} Pulsing Time V_{BUS} pulse time during SRP. Value=Pulse time (number of PHY clock)/1024
31:12	Reserved		

23.7.10 Full-speed OTG device IN endpoint FIFO empty interrupt mask register (OTG_FS_DIEIMASK)

Offset address: 0x834

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	INEM	R/W	IN Endpoint Tx FIFO Empty Interrupt Mask No. X bit indicates TXFE interrupt mask of IN endpoint X. Up to 16 IN endpoints. 0: Mask 1: Not mask
31:16	Reserved		

23.7.11 Full-speed OTG device IN endpoint 0 control register (OTG_FS_DIEPCTRL0)

Offset address: 0x900

Reset value: 0x0000 8000

Field	Name	R/W	Description
1:0	MAXPS	R/W	Maximum Packet Size This bit configures the maximum data packet size of endpoint. 00: 64 bytes 01: 32 bytes 10: 16 bytes 11: 8 bytes
14:2	Reserved		
15	USBAEP	R	USB Active Endpoint This bit indicates whether the endpoint is activated in the current configuration and interface. This bit is always set to 1.
16	Reserved		
17	NAKSTS	R	NAK Status 0: The module replies non-NAK handshake signal according to the FIFO state 1: The module replies the NAK handshake signal on this endpoint. At this time, even if there is space in TXFIFO, the module will still stop transmitting data.
19:18	EPTYPE	R	Endpoint Type This bit is set to 00 by hardware, indicating control type of the endpoint.
20	Reserved		
21	STALLH	R/S	STALL Handshake The program can only set this bit to 1 and when the endpoint receives the SETUP token, this bit will be cleared to 0. The priority of STALL is higher than that of NAK.
25:22	TXFNUM	R/W	TXFIFO Number Set a separate FIFO number for IN endpoint 0.

Field	Name	R/W	Description
26	NAKCLR	W	NAK Clear When performing write operation to this bit, the NAK bit of the endpoint 0 will be cleared to 0.
27	NAKSET	W	NAK Set When performing write operation to this bit, the NAK bit will be set to 1.
29:28	Reserved		
30	EPDIS	R	Endpoint Disable Data transmission on the endpoint can be stopped by setting this bit to 1. This bit needs to be cleared to 0 before the endpoint disable interrupt bit is set to 1; this bit can only be set to 1 after EPEN is set to 1.
31	EPEN	R	Endpoint Enable After this bit is set to 1, the endpoint will start to transmit data. When any of the following interrupts is triggered, this bit will be cleared to 0: SETUP completed Disable endpoint Transmission completed

23.7.12 Full-speed OTG device IN endpoint x control register (OTG_FS_DIEPCTRLx) (x=1~3, endpoint number)

Offset address: 0x900+0x20x

Reset value: 0x0000 0000

Field	Name	R/W	Description
10:0	MAXPS	R/W	Maximum Packet Size This bit configures the maximum data packet size of endpoint. (in byte).
14:11	Reserved		
15	USBAEP	R/W	USB Active Endpoint This bit indicates whether the endpoint is activated in the current configuration and interface. After USB is reset, this bit will be cleared to 0 (except endpoint 0).
16	EOF	R	Even Odd Frame This bit is used to indicate the frame number transmitted/received by the endpoint (for synchronization IN) or the PID of data packet (for interrupt/batch IN). Used for synchronous IN endpoints: 0: Even frame 1: Odd frame Endpoint Data PID Used for interrupt/batch IN endpoints: 0：DATA0 1：DATA1

Field	Name	R/W	Description
17	NAKSTS	R	NAK Status 0: The module replies non-NAK handshake signal according to the FIFO state 1: The module replies to the NAK handshake signal on this endpoint; at this time, for asynchronous IN: even if there is data available in TXFIFO, the module will still stop transmitting data; for synchronous IN, the module will transmit zero-length data packet even if there is data available in TXFIFO Note: The module always responds to the SETUP data packet through ACK handshake.
19:18	EPTYPE	R/W	Endpoint Type 00: Control 01: Synchronous 10: Batch 11: Interrupt
20	Reserved		
21	STALLH	RW/RS	STALL Handshake For uncontrolled and non-synchronous IN endpoints (read/write mode is R/W): When this bit is set to 1, the device will reply STALL to all tokens from the USB host. This bit can only be cleared to 0 by software. Used for control endpoints (read/write mode is R/W): When this bit is set to 1, it means that the module receives SETUP token.
25:22	TXFNUM	R/W	TXFIFO Number These bits indicate the FIFO number associated with the endpoint, and a separate FIFO number needs to be set for each valid IN endpoint
26	NAKCLR	W	NAK Clear When performing write operation to this bit, the NAK bit of the endpoint will be cleared to 0.
27	NAKSET	W	NAK Set When performing write operation to this bit, the NAK bit of the endpoint will be set to 1. This bit can control the transmission of NAK handshake signal.
28	DPIDSET	W	DATA0 PID Set Used for interrupt/batch IN endpoints: When performing write operation to this bit, PID will be set to DATA0. Even Frame Set Used for synchronous IN endpoints: When performing write operation to this bit, EOF will be set to even frame.
29	OFSET	W	Odd Frame Set It is used for synchronous IN endpoints. When performing write operation to this bit, EOF will be set to odd frame.

Field	Name	R/W	Description
30	EPDIS	R/S	Endpoint Disable Data transmission on the endpoint can be stopped by setting this bit to 1. This bit needs to be cleared to 0 before the endpoint disable interrupt bit is set to 1; this bit can only be set to 1 after EPEN is set to 1.
31	EPEN	R/S	Endpoint Enable After this bit is set to 1, the endpoint will start to transmit data. When any of the following interrupts is triggered, this bit will be cleared to 0: SETUP completed Disable endpoint Transmission completed

23.7.13 Full-speed OTG device IN endpoint x interrupt register (OTG_FS_DIEPINTx) (x=0~3, endpoint number)

Offset address: 0x908+0x20x; m=0~3

Reset value: 0x0000 0080

Read this register when ONEP bit of OTG_FS_GCINT register is set to 1; Read OTG_FS_DAEPINT register to obtain the accurate endpoint number of the device endpoint x interrupt register, and then read the register; only when the corresponding bit of the register is cleared to 0, can the corresponding bit of OTG_FS_DAEPINT register and OTG_FS_GCINT register be cleared to 0.

Field	Name	R/W	Description
0	TSFCMP	RC_W1	Transfer Complete Interrupt This bit indicates that the transmission on the endpoint has been completed.
1	EPDIS	RC_W1	Endpoint Interrupt Disable This bit means that the endpoint is disabled.
2	Reserved		
3	TO	RC_W1	Timeout Interrupt This bit is only applicable to the control IN endpoints, indicating that the response to the recently received IN token has timed out.
4	ITXEMP	RC_W1	Receive IN Token Interrupt when FIFO is empty This bit is only applicable to non-periodic IN endpoints, indicating that IN token is received when the corresponding TXFIFO of the endpoint is empty.
5	Reserved		
6	IEPNAKE	RC_W1	IN Endpoint NAK Effective This bit indicates that the module samples NAK, namely, the NAK bit of the IN endpoint has taken effect. This bit will be cleared to 0 when NAKCLR bit of OTG_FS_DIEPCTRLx register is written.
7	TXFE	R	TXFIFO Empty Interrupt The interrupt will be generated when TXFIFO of this endpoint is empty.

Field	Name	R/W	Description
31:8	Reserved		

23.7.14 Full-speed OTG device IN endpoint 0 transmission size register (OTG_FS_DIEPTRS0)

Offset address: 0x910

Reset value: 0x0000 0000

This register can be modified only after EPEN bit of OTG_FS_DIEPCTRLx register is set to 1; this register can be read only when EPEN bit of OTG_FS_DIEPCTRLx register is cleared to 0

Field	Name	R/W	Description
6:0	EPTRS	R/W	Endpoint Transfer Size This bit indicates the data size contained by endpoint 0 in one data transmission.
18:7	Reserved		
20:19	EPPCNT	R/W	Endpoint Packet Count This bit indicates the number of data packets contained by endpoint 0 in one data transmission.
31:21	Reserved		

23.7.15 Full-speed OTG device IN endpoint x transmission size register (OTG_FS_DIEPTRSx) (x=1~3, endpoint number)

Offset address: 0x910+0x20x; x=1~3

Reset value: 0x0000 0000

This register can be modified only after EPEN bit of OTG_FS_DIEPCTRLx register is set to 1; this register can be read only when EPEN bit of OTG_FS_DIEPCTRLx register is cleared to 0

Field	Name	R/W	Description
18:0	EPTRS	R/W	Endpoint Transfer Size This bit indicates the data size contained by endpoint x in one data transmission (in byte).
28:19	EPPCNT	R/W	Endpoint Packet Count This bit indicates the number of data packets contained by endpoint x in one data transmission.
30:29	TXDCNT	R/W	Transmit Packet Count For periodic IN endpoints, this bit indicates the number of data packets that must be transmitted per frame on USB. For the calculation synchronization IN endpoint, this bit calculates the data PID of the endpoint. 01: 1 10: 2 11: 3
31	Reserved		

23.7.16 Full-speed OTG device IN endpoint x TXFIFO state register (OTG_FS_DITXFSTSx) (x=0~3, endpoint number)

Offset address: 0x918+0x20m; m=0~3

Reset value: 0x0000 0200

Field	Name	R/W	Description
15:0	INEPTXFSA	R	IN Endpoint TXFIFO Space Available This bit indicates the available space of the IN endpoint TXFIFO (in word). 0x0: IN endpoint TXFIFO is full 0x1: 1 byte 0x2: 2 bytes 0xn: n bytes are available (0<n<512) Other value: Reserved
31:16	Reserved		

23.7.17 Full-speed OTG device OUT endpoint 0 control register (OTG_FS_DOEPCTRL0)

Offset address: 0xB00

Reset value: 0x0000 8000

Field	Name	R/W	Description
1:0	MAXPS	R	Maximum Packet Size This bit configures the maximum data packet size of endpoint. 00: 64 bytes 01: 32 bytes 10: 16 bytes 11: 8 bytes
14:2	Reserved		
15	USBAEP	R	USB Active Endpoint This bit indicates whether the endpoint is activated in the current configuration and interface. This bit is always set to 1.
16	Reserved		
17	NAKSTS	R	NAK Status 0: The module replies non-NAK handshake signal according to the FIFO state 1: The module replies the NAK handshake signal on this endpoint. At this time, even if there is space in RXFIFO, the module will still stop receiving data.
19:18	EPTYPE	R	Endpoint Type This bit is set to 00 by hardware, indicating control type of the endpoint.
20	SNMEN	R/W	Snoop Mode Enable In snoop mode, the correctness of OUT data packets is not checked before they are transmitted to the storage area.

Field	Name	R/W	Description
21	STALLH	R/S	STALL Handshake The program can only set this bit to 1 and when the endpoint receives the SETUP token, this bit will be cleared to 0. The priority of STALL is higher than that of NAK.
25:22	Reserved		
26	NAKCLR	W	NAK Clear When performing write operation to this bit, the NAK bit of the endpoint 0 will be cleared to 0.
27	NAKSET	W	NAK Set When performing write operation to this bit, the NAK bit will be set to 1.
29:28	Reserved		
30	EPDIS	R	Endpoint Disable Data transmission on the endpoint can be stopped by setting this bit to 1. This bit needs to be cleared to 0 before the endpoint disable interrupt bit is set to 1; this bit can only be set to 1 after EPEN is set to 1.
31	EPEN	W	Endpoint Enable After this bit is set to 1, the endpoint will start to transmit data. When any of the following interrupts is triggered, this bit will be cleared to 0: SETUP completed Disable endpoint Transmission completed

23.7.18 Full-speed OTG device OUT endpoint x control register (OTG_FS_DOEPCTRLx) (x=1~3, endpoint number)

Offset address: 0xB00+0x20x

Reset value: 0x0000 0000

Field	Name	R/W	Description
10:0	MAXPS	R/W	Maximum Packet Size This bit configures the maximum data packet size of endpoint. (in byte).
14:11	Reserved		
15	USBAEP	R/W	USB Active Endpoint This bit indicates whether the endpoint is activated in the current configuration and interface. After USB is reset, this bit will be cleared to 0 (except endpoint 0).

Field	Name	R/W	Description
16	EOF	R	Even Odd Frame This bit is used to indicate the frame number transmitted/received by the endpoint (for synchronization IN) or the PID of data packet (for interrupt/batch IN). Used for synchronous IN endpoints: 0: Even frame 1: Odd frame Endpoint Data PID Used for interrupt/batch IN endpoints: 0：DATA0 1：DATA1
17	NAKSTS	R	NAK Status 0: The module replies non-NAK handshake signal according to the FIFO state 1: The module replies the NAK handshake signal on this endpoint. At this time, for OUT endpoint, even if there is remaining space in RXFIFO, the module will still stop receiving data Note: The module always responds to the SETUP data packet through ACK handshake.
19:18	EPTYPE	R/W	Endpoint Type 00: Control 01: Synchronous 10: Batch 11: Interrupt
20	SNMEN	R/W	Snoop Mode Enable In snoop mode, the correctness of OUT data packets is not checked before they are transmitted to the storage area.
21	STALLH	RW/RS	STALL Handshake For uncontrolled and non-synchronous IN endpoints (read/write mode is R/W): When this bit is set to 1, the device will reply STALL to all tokens from the USB host. This bit can only be cleared to 0 by software. Used for control endpoints (read/write mode is R/S): When this bit is set to 1, it means that the module receives SETUP token.
25:22	Reserved		
26	NAKCLR	W	NAK Clear When performing write operation to this bit, the NAK bit of the endpoint will be cleared to 0.
27	NAKSET	W	NAK Set When performing write operation to this bit, the NAK bit of the endpoint will be set to 1. This bit can control the transmission of NAK handshake signal.

Field	Name	R/W	Description
28	DPIDSET	W	DATA0 PID Set Used for interrupt/batch IN endpoints: When performing write operation to this bit, PID will be set to DATA0. Even Frame Set Used for synchronous IN endpoints: When performing write operation to this bit, EOF will be set to even frame.
29	OFSET	W	Odd Frame Set Used for synchronous OUT endpoints: When performing write operation to this bit, EOF will be set to odd frame. Used for interrupt/batch OUT endpoints: When performing write operation to this bit, PID will be set to DATA1.
30	EPDIS	R/S	Endpoint Disable Data transmission on the endpoint can be stopped by setting this bit to 1. This bit needs to be cleared to 0 before the endpoint disable interrupt bit is set to 1; this bit can only be set to 1 after EPEN is set to 1.
31	EPEN	R/S	Endpoint Enable After this bit is set to 1, the endpoint will start to transmit data. When any of the following interrupts is triggered, this bit will be cleared to 0: SETUP completed Disable endpoint Transmission completed

23.7.19 Full-speed OTG device OUT endpoint x interrupt register (OTG_FS_DOEPINTx) (x=0~3, endpoint number)

Offset address: 0xB08+0x20m; m=0~3

Reset value: 0x0000 0080

Read this register when ONEP bit of OTG_FS_GCINT register is set to 1; Read OTG_FS_DAEPINTx register to obtain the accurate endpoint number of the device endpoint x interrupt register, and then read the register; only when the corresponding bit of the register is cleared to 0, can the corresponding bit of OTG_FS_DAEPINT register and OTG_FS_GCINT register be cleared to 0.

Field	Name	R/W	Description
0	TSFCMP	RC_W1	Transfer Complete Interrupt This bit indicates that the transmission on the endpoint has been completed.
1	EPDIS	RC_W1	Endpoint Interrupt Disable This bit means that the endpoint is disabled.
2	Reserved		

Field	Name	R/W	Description
3	SETPCMP	RC_W1	SETUP Phase Complete Interrupt This bit is only applicable to the control OUT endpoint, indicating that the SETUP phase has been completed. After an interrupt is generated, the received SETUP data can be decoded.
4	RXOTDIS	RC_W1	Receive OUT Token When Disable Interrupt This bit is only applicable to the control OUT endpoint, indicating that the OUT token is received without enabling the endpoint.
5	Reserved		
6	RXBSP	RC_W1	Receive Back-to-Back SETUP Packet Interrupt This bit is only applicable to the control OUT endpoint, indicating that the endpoint has received more than three consecutive SETUP data packets.
31:7	Reserved		

23.7.20 Full-speed OTG device OUT endpoint 0 transmission size register (OTG_FS_DOEPTRS0)

Offset address: 0xB10

Reset value: 0x0000 0000

This register can be modified only after EPEN bit of OTG_FS_DOEPCTRLx register is set to 1; this register can be read only after EPEN bit of OTG_FS_DOEPCTRLx register is cleared to 0

Field	Name	R/W	Description
6:0	EPTRS	R/W	Endpoint Transfer Size This bit indicates the data size contained by endpoint 0 in one data transmission (in byte).
18:7	Reserved		
19	EPPCNT	R/W	Endpoint Packet Count This bit will decrease to 0 after RXFIFO is written to a data packet.
28:20	Reserved		
30:29	SPCNT	R/W	SETUP Packet Count These bits indicate the number of SETUP dat packets that can be received continuously 01: 1 10: 2 11: 3
31	Reserved		

23.7.21 Full-speed OTG device OUT endpoint x transmission size register (OTG_FS_DOEPTRS) (x=1~3, endpoint number)

Offset address: 0xB10+0x20m; m=1~3

Reset value: 0x0000 0000

This register can be modified only after EPEN bit of OTG_FS_DOEPCTRLx register is set to 1; this register can be read only after EPEN bit of OTG_FS_DOEPCTRLx register is cleared to 0

Field	Name	R/W	Description
18:0	EPTRS	R/W	Endpoint Transfer Size This bit indicates the data size contained by endpoint x in one data transmission (in byte).
28:19	EPPCNT	R/W	Endpoint Packet Count This bit indicates the number of data packets contained by endpoint x in one data transmission.
30:29	PID_SPCNT	R/W	Receive Data PID or SETUP Packet Count For synchronous OUT endpoints, this bit indicates the PID of the last received data packet. 00：DATA0 01：DATA2 10：DATA1 11：MDATA For the control OUT endpoint, this bit indicates the number of SETUP data packets that the endpoint can continuously receive. 01: 1 10: 2 11: 3
31	Reserved		

23.8 Full-speed OTG power and clock gating control register (OTG_FS_PCGCTRL)

Offset address: 0xE00

Reset value: 0x0000 0000

This register is applicable to both master mode and device mode.

Field	Name	R/W	Description
0	PCLKSTOP	R/W	PHY Clock Stop 0: The PHY clock is enabled to start when the USB communication is restored or the session is restarted 1: Stop the PHY clock when USB communication is suspended, the session is invalid, or the device is disconnected
1	GCLK	R/W	Gate HCLK 0: When the USB communication is restored or the session is restarted, it is allowed to stop providing the clock to modules other than AHB bus slave interface, main interface and wake-up 1: When the USB communication is suspended or the session is invalid, stop providing the clock for the modules other than AHB bus slave interface, main interface and wake-up

Field	Name	R/W	Description
3:2	Reserved		
4	PHYSUS	R/W	PHY Suspend This bit means that PHY is suspended.
31:5	Reserved		

24 Ethernet

24.1 Introduction

Ethernet provides configurable and flexible peripherals to meet various application requirements of customers. It supports two industry standard interfaces connected to the external physical layer: MII and Reduced Media Independent Interface RMII used by default, where MII is only defined in the IEEE 802.3 specification. It has many application fields, such as switch, network interface card and so on. Ethernet can transmit and receive data according to IEEE 802.3-2002 standard with the help of peripherals.

Ethernet complies with the following standards:

- IEEE802.3-2002 for Ethernet MAC
- IEEE1588-2002 standards which specify synchronization precision of networked clock
- AMBA 2.0 for AHB master/slave ports
- RMII specification of RMII Alliance

24.2 Main characteristics of Ethernet

24.2.1 Main characteristics of MAC

（1） Communicates with an external high-speed Ethernet PHY through the MII interface conforming to the IEEE802.3 specification

（2） Support 10/100Mbp data transmission rate when external PHY interface

（3） Half-duplex operation

- Support CSMA/CD protocol
- Provide back pressure flow control

（4） Full-duplex operation

- Support IEEE 802.3x flow control
- If the flow control input signal disappears, the zero-range pause frame will be automatically transmitted
- The received pause frame can be forwarded to the user application program

（5） Insert header and start-of-frame data in the transmit path, delete header and start-of-frame data in the receive path

（6） Automatically generate CRC and pad, which can be automtically cleared when receiving frames

（7） Programmable frame interval (In 8-bit units, 40-96 bits)

（8） Programmable frame length; it supports up to 16KB jumbo frame

（9） Address filter mode
- Four 48-bit DA address registers; each byte can be masked
- Three 48-bit SA address registers; each byte can be masked
- 64-bit Hash filter, applicable to multicast and unicast addresses
- Can transmit multi-cast address frames
- Support mixed mode, and can transmit all frames, with network monitoring not filtered
- A state report will be attached when transmitting incoming data packets

（10） Independent transmitting, receiving and control interface

（11） 32-bit data transmitting interface and receiving interface

（12） Conduct IEEE 802.1Q VLAN variable detection for received frames

（13） MDIO main interface (optional), used for PHY device configuration and management

（14） Conduct forced network statistics through RMON/MIB counter

（15） Detect LAN wake-up frame and AMD Magic Packet™ frame

（16） Support Ethernet frame timestamp, and each frame gives 64-bit timestamp

（17） 2KB transmit FIFO of programmable threshold function and 2KB receive FIFO of configurabe threshold function

（18） During multi-frame storage of the receive FIFO, the receiving state vector is inserted into the receive FIFO after EOF transmission, so that the receiving state of these frames will not be stored by the receive FIFO

（19） In storage and forwarding mode, all error frames will be filtered in receiving process and not be forwarded to the application program

（20） Generate pulses for lost or damaged frames in the receive FIFO to support data statistics

（21） Select to forward good frames of small size

（22） In enhanced receiving, IPv4 header checksum and TCP, UDP or ICMP checksum encapsulated in IPv4 or IPv6 data packets can be checked

（23） The checksum unloads the received IPv4 and TCP data packets encapsulated by Ethernet frames

（24） Storage and forwarding mechanism transmitted to MAC

（25） The pause frame control or back pressure signal to be transmitted to the MAC core is automatically generated according to the receive FIFO filling level

（26） Handle automatic retransmission of conflict frames during transmission

（27） Discard frames under excessive collision, delay collision, excessive delay and underflow conditions

（28） Control and refresh Tx FIFO through software

（29） Calculate IPv4 header checksum and TCP, UDP or ICMP checksum and insert the frames transmitted in storage and forwarding mode

（30） Internal loopback through MII during debugging

24.2.2 Main characteristics of PTP

（1） Timestamp of transmitting and receiving frames

（2） Coarse calibration and precision calibration

（3） An interrupt will be triggered when the system time is greater than the target time

（4） Output second pulse

24.2.3 Main characteristics of DMA

（1） AHB burst type can be selected at the AHB main interface

（2） Select address alignment burst from AHB master port

（3） AHB slave interface supports all AHB burst types

（4） Double-buffer (buffering ring) or linked list (chain) descriptor link

（5） Byte aligned addressing supported by data buffer

（6） Optimize packet-oriented DMA transmission

（7） Descriptor architecture, which allows transmission of large data blocks with minimal CPU intervention (each descriptor can transmit up to 8KB data)

（8） Comprehensive state when reporting normal operation and transmission errors

（9） Size of single programmable burst for transmitting and receiving DMA engine, for optimal host bus

（10） Programmable interrupt option

（11） Control transmitting/receiving completion interrupt

（12） Loop scheduling arbitration or fixed priority arbitration is adopted between the transmitting engine and the receiving engine

（13） The current Tx/RX descriptor pointer and buffer pointer are used as state registers

24.3 Functional description

24.3.1 Multiplexing function mapping

The following table displays MAC signal and corresponding MII/RMII signal mapping.

Table 77 Multiplexing Function Mapping

Port	AF11
	ETH
PA0-WKUP	ETH_MII_CRS
PA1	ETH_MII_RX_CLK/ETH_RMII_REF_CLK
PA2	ETH_MDIO
PA3	ETH_MII_COL
PA7	ETH_MII_RX_DV/ETH_RMII_CRS_DV
PB0	ETH_MII_RXD2
PB1	ETH_MII_RXD3
PB5	ETH_PPS_OUT
PB8	ETH_MII_TXD3
PB10	ETH_MII_RX_ER
PB11	ETH_MII_TX_EN/ETH_RMII_TX_EN
PB12	ETH_MII_TXD0/ETH_RMII_TXD0
PB13	ETH_MII_TXD1/ETH_RMII_TXD1
PC1	ETH_MDC
PC2	ETH_MII_TXD2
PC3	ETH_MII_TX_CLK
PC4	ETH_MII_RXD0/ETH_RMII_RXD0
PC5	ETH_MII_RXD1/ETH_RMII_RXD1
PE2	ETH_MII_TXD3
PG8	ETH_PPS_OUT
PG11	ETH_MII_TX_EN/ETH_RMII_TX_EN
PG13	ETH_MII_TXD0/ETH_RMII_TXD0
PG14	ETH_MII_TXD1/ETH_RMII_TXD1
PH2	ETH_MII_CRS
PH3	ETH_MII_COL
PH6	ETH_MII_RXD2

Port	AF11
	ETH
PH7	ETH_MII_RXD3
PI10	ETH_MII_RX_ER

24.3.2 SMI, MII and RMII

Ethernet peripherals include MAC 802.3 with dedicated DMA controller. It supports MII and RMII used by default and switches them through select bit. It also includes SMI for communicating with external PHY. The mode and function of MAC controller and DMA controller can be selected through a configuration register.

When transmitting data, first transmit the data from the system memory to the TX FIFO buffer through DMA, and then transmit it through the MAC core. The Ethernet frame received through the line is stored by RX FIFO before it is transmitted to the system memory through DMA.

Note: When using Ethernet, the clock frequency of AHB shall be at least 25MHz.

24.3.2.1 Station management interface (SMI)

SMI supports accessing 32 PHY. The application program selects one PHY among the 32 PHY through the 2-wire clock and data line, and then accesses any PHY register. Only one register in one PHY can be addressed at any given time.

Both MDC clock line and MDIO data line are used as multiplexing function I/O in the microcontroller:

- MDC: Periodic clock, which provides reference timing when transmitting data at 2.5MHz. The minimum high/low-level time of MDC is 160ns. The minimum cycle of MDC is 400ns. In idle state, the SMI management interface drives the MDC clock signal to low level.
- MDIO: Data input/output bit stream, which is used to synchronize the transmission state with PHY device through MDC clock signal.

SMI frame format

Table 78Frame Format

Management frame format	
Header	Each operation can be started through the header field, and the header field is used to establish synchronization with the PHY device and corresponds to 32 consecutive logical “1” bits on the MDIO line and 32 cycles on the MDC.
Start	It is defined by the <01> mode, and used to verify transition of the state of the line from the default logic "1" - logic "0" - logic "1".
Operation	Define the type of ongoing operation.

Management frame format	
PADDR	The PHY address has 5 bits, allowing 32 unique PHY addresses. The MSB bit of the address is the first to transmit and receive.
RADDR	The register address has 5 bits, and 32 different registers can be addressed in the selected PHY device. The MSB bit of the address is the first to transmit and receive.
TA	A 2-bit mode is defined between RADDR and DATA to avoid competition during read operation. When performing read operation, the MAC controller drives two bits of the TA to the high-impedance state on MDIO line. PHY device will drive the first bit of TA to high-impedance state and the second bit to "0". When write operation is performed, the MAC controller will drive the <10> mode for the TA. The PHY device drives two bits of TA to the high-impedance state.
Data	The data field is 16 bits. Bit 15 of the MAC_DATA register is the first bit.
Idle	MDIO line is driven to the high-impedance state. The three-state driver is disabled, and the pull-up resistance of PHY keeps the line in the logic "1" state.

SMI clock selection

Mac starts management read/write operation. SMI clock is a frequency division clock with AHB clock as clock source. The frequency division factor depends on the clock range set in MAC_ADDR register.

Table 79 Clock Range

CR bit	HCLK clock	MDC clock
000	60-72MHz	AHB clock/42
001	Reserved	-
010	20-35MHz	AHB clock/16
011	35-60MHz	AHB clock/26
100、101、110、111	Reserved	-

SMI write operation

When MB bit and MW bit of MAC_ADDR are set to 1 by application program, SMI will trigger write operation of PHY register by transmitting PHY address, and register address in PHY, and writing data. When performing write operation, the application program cannot modify MAC_ADDR and MAC_DATA registers. After write operation is completed, SMI will reset MB bit.

SMI read operation

When MB bit of MAC_ADDR is set and MW bit is cleared to zero, SMI will trigger read operation of PHY register by transmitting PHY address, and register address in PHY. When performing read operation, the application program cannot modify MAC_ADDR and MAC_DATA registers. After read operation is completed, SMI will reset MB bit, and update the read data from PHY to MAC_DATA register.

24.3.2.2 Media independent interface (MII)

MII defines the interconnection between MAC sublayer and PHY at data transmission rate of 10 Mbit/s and 100 Mbit/s.

The signals are as follows:

（1） MII_TX_EN: Transmit enable signal; MAC is currently transmitting half byte for MII

（2） MII_RX_DV: Data receiving effective signal; PHY is currently receiving recovered and decoded half byte of MII

（3） MII_TXD [3:0]: Data transmitting signal

（4） MII_RXD [3:0]: Data receiving signal

（5） MII_RX_ER: Receiving error signal

（6） MII_TX_CLK: Continuous clock signal, providing reference timing for TX data transmission

（7） MII_RX_CLK: Continuous clock signal, providing reference timing for RX data transmission

（8） MII_CRS: Carrier sense signal

（9） MII_COL: Conflict detection signal

Table 80 TX Interface Signal Encoding

MII_TX_EN	MII_TXD [3:0]	Description
0	0000-1111	Normal frame internal
1	0000-1111	Normal data transmission

Table 81 RX Interface Signal Encoding

MII_RX_DV	MII_RX_ER	MII_RXD [3:0]	Description
0	0	0000-1111	Normal frame internal
0	1	0000	Normal frame internal
0	1	0001-1101	Reserved
0	1	1110	Error carrier detection
0	1	1111	Reserved
1	0	0000-1111	Normal data receiving
1	1	0000-1111	Data receiving error

MII clock source

TX_CLK and RX_CLK clock signal can take effect only when 25MHz clock is provided to external PHY, and this signal can be output through MCO pin. The

required frequency can be obtained on MCO pin through 25 MHz external quartz crystal only when PLL frequency doubling is configured.

24.3.2.3 Reduced media independent interface (RMII)

RMII reduces the number of pins of MCU of Ethernet peripherals and external PHY at 10/100Mbit/s. According to IEEE 802.3u standard, MII has 16 data and control signal pins. RMII reduces the number of pins to 7.

RMII is instantiated between MAC and PHY. It is conductive to converting MII of MAC to RMII. RMII has the following characteristics:

（1） Separate 2-bit wide transmitting and receiving data path

（2） 10-Mbit/s and 100-Mbit/s running speed

（3） The reference clock is 50MHz

（4） Provide the same reference clock to MAC and external Ethernet PHY from the outside

RMII clock source

Use external 50MHz clock or embedded PLL to generate 50MHz-frequency signal to drive PHY.

24.3.2.4 MII/RMII selection

When the Ethernet controller is not in reset mode or the clock is enabled, the application program needs to set MII/RMII mode.

24.3.3 Media access control (MAC 802.3)

The access method of IEEE 802.3 international standard applicable to LAN is CSMA/CD. The Ethernet peripheral consists of one MAC 802.3 controller with MII and a dedicated DMA controller.

（1） The following system uses LAN CSMA/CD sublayer
- Support half-duplex and full-duplex
- The conflict detection access method is applicable only to half-duplex
- The data rate of baseband system and broadband system is 10 Mbit/s and 100Mbit/s
- Support MAC to control frame sublayer

（2） Functions of MAC sublayer
- Data encapsulation
  - Framing
  - Addressing
  - Error detection
- Media access management
  - Media distribution

- Contention resolution

（3） Working mode of MAC sublayer

- Half-duplex: Contention for physical media with CSMA/CD algorithm
- Full duplex: When the physical media supports synchronous transmission and receiving, and two full-duplex stations are connected to the LAN, data can be transmitted and received at the same time without solving the contention problem.

24.3.3.1 MAC 802.3 frame format

IEEE 802.3-2002 standard specifies MAC uses MAC sublayer and optional MAC control sublayer (10/100 Mbit/s).

（1） Two frame formats are specified for data communication system using CSMA/CD MAC

- Basic MAC frame format
- Tagged MAC frame format

（2） Frame structure of field

- Header: 7 bytes, used for synchronization
- Start frame delimiter: 1 byte, indicating the start of the frame
- Destination address and source address: MAC address field (6 bytes), indicating the address of destination station and source station

（3） Address assignment is based on the following types

- Single address: The physical address related to THE special station in the network.
- Group address: A multi-destination address related to one or more stations in a given network. There are two kinds of multicast addresses, namely, multicast group address and broadcast address.
- QTag prefix: A 4-byte field inserted in the source address and MAC client length/type field. This field is an extension of the basic frame (untagged) to obtain the tagged MAC frame. There is no untagged MAC frame.
- Data and PAD: n bytes; the data are completely transparent, which means that any number of bytes may appear in data field. If PAD exists, its size is decided by the data size.
- MAC client length/type: 2 bytes, which have different meanings.
- Frame inspection sequence: 4 bytes including CRC value. CRC calculation is based on the following fields: source address, destination address, QTag prefix, length/type, LLC data and PAD.

24.3.3.2 MAC frame transmission

All operations when DMA controls transmission. DMA pushes the data read from system memory into FIFO. Then the frame will pop up and be transmitted to MAC core. When frame transmission is over, the transmission state will be

obtained from MAC core and sent back to DMA. The FIFO fill level is indicated to the DMA to initiate data acquisition in the required system memory burst by using the AHB interface. The data from AHB main interface will be pushed to FIFO. The depth of transmit FIFO is 2KB

Transmit protocol

MAC controls transmission of Ethernet frame. The following functions are implemented to meet IEEE 802.3/802.3z specification:

- Generate header and SFD
- Generate transmitted frame state
- Generate blocking signals in half-duplex mode
- Control the flow (back pressure) in half-duplex mode
- Control Jabber timeout
- Including timestamp snapshot logic that conforms to IEEE 1588

Transmit CRC: Automatic generation of CRC and pad

In order to meet the minimum data field requirements of IEEE 802.3, when the number of bytes received from the application program is less than 60, zero will be attached to the transmitted frame to make the data length become 46 bytes. MAC can set not adding filling value. Calculate the CRC of the FCS field and attach it to the data being transmitted. If MAC is set to not attach the CRC value to the end of the Ethernet frame, the CRC will not be transmitted. However, when MAC is set to attach filling to the frame less than 60 bytes, CRC will be attached to the end of the filling frame.

Transmit data packets

Transmission of data packets contains transmission of single data packet and multiple data packets, and their operation mode is different.

Transmit scheduler

MAC is responsible for scheduling the frame transmission on MII. The interval between two transmitted frames can be maintained, and the truncated binary exponential rollback algorithm can be observed in half-duplex mode. MAC enables transmission after meeting IFG counter and rollback delay conditions.

Transmit flow control

In full-duplex mode, when MAC_FCTRL[TXFCTRLEN]=1, MAC will generate pause frame and transmit it when needed. The pause frame and CRC are transmitted together. Generation of the pause frame can be enabled in two ways. When the application program sets FCTRLB bit to 1 or the receive FIFO is full, the pause frame will be transmitted.

Transmit FIFO refresh

FTXF bit of ETH_DMAOPMOD register controls to clear the transmit FIFO. Even if Tx FIFO is transmitting the frame to MAC core, Tx FIFO and the corresponding pointer will be immediately cleared to the initial state, as a result, an underrun event will be generated to MAC transmitter, and the frame transmission will be terminated. The state of the frame will mark both the underrun event and the frame emptying event.

Transmit status word

After the Ethernet frame is transmitted to the MAC core and the core completes the transmission of the frame, the transmission state will be provided to the application program.

Transmit checksum offload

The communication protocol realizes the checksum field, which helps understanding the integrity of data transmitted through the network. Because encapsulating TCP and UDP on IP datagrams is the most widely application of the Ethernet, the Ethernet controller has the function of transmitting checksum offload, and this function supports checksum calculation and insertion in the transmitting path, and error detection in the receiving path.

Retransmitting during conflict

In half-duplex mode, when transmitting frames to MAC, collision event may occur on the MAC line interface. The MAC may even indicate retrying before finishing receiving the frame. Then the frame will be retransmitted and pop up from the FIFO again.

MII/RMII

Each half byte from MII is transmitted on RMII, double bits are transmitted at one time, and the transmitting order is from low to high.

24.3.3.3 MAC frame receiving

The MAC pushes the received frame into the Rx FIFO. Once the state of this FIFO exceeds the configured receiving threshold, it will be indicated to DMA so that DMA can initiate preconfigured burst transmission to AHB interface.

Receive protocol

When a frame is received, the header and SFD of the frame will be removed. When SFD is detected, MAC will transmit Ethernet frame data to RX FIFO, which starts from the first byte after SFD. After the IEEE 1588 timestamp function is enabled, once an SFD is detected on the MII, a snapshot of the

system time will be obtained. This timestamp will be transmitted to the application program, unless the MAC filters and discards the frame.

Receive multiple frames

Since the state is available immediately after receiving the data, the frames can be stored as long as the FIFO is not full.

Receive CRC: Automatic CRC and pad removal

The MAC will check the CRC error in the received frame and calculate the 32-bit CRC in it. No matter whether the pad/CRC is automatically removed, the Mac will receive the whole frame to calculate the CRC check of the received frame.

Received frame controller

When MAC_FRAF[RXA]=0, MAC will perform frame filtering according to the destination address and source address. If filtering fails, the frame will be discarded and not be transmitted to the application program. When the filtering parameters change dynamically, the filtering fails, the remaining frames will be discarded and the receive status word will be updated immediately. In Ethernet power-down mode, all received frames will be discarded and not be forwarded to the application program.

Receive checksum offload

The IPC bit in the MAC_CFG register controls the receive checksum offload. This function is to detect and process IPv4 and IPv6 frames in received Ethernet frame to ensure data integrity. The MAC identifies IPv4 or IPv6 frames by checking the type field of the received Ethernet frame. This identification method is also applicable to frames with VLAN tag.

Receive flow control

MAC_FCTRL[RXFCTRLEN] controls the detection function of pause frame. When this bit is set, the MAC will detect the receiving pause frame and the frame transmission will pause. The specific time is determined by the delay set in the received pause frame. After the flow control is enabled, start to monitor whether the destination address of the received frame matches the multicast address of the control frame. If they match, the MAC will determine whether to transmit the received control frame to the application program according to the MAC_FRAF[PCTRLF] bit.

Error processing

Table 97 Error Handling Situation

Occurrence	Processing results
Rx FIFO has been full before EOF data is received from MAC.	Discard the entire frame, and the overrun counter in the ETH_DMAMFABOCNT register increses.
Use FERRF and FUF bits in the ETH_DMAOPMOD register to enable the corresponding functions.	Rx FIFO can filter error frames and too small frames.
Configure the receive FIFO to work in storage and forwarding mode.	Filter and discard all error frames.
In pass-through mode, if the SOF of the frame is read from Rx FIFO, the state and length of the frame are available.	The whole error frame can be discarded. DMA can empty the error frame being read from FIFO. Then stop the data transmission to DMA, read from the inside and discard the remaining frames. If available, transmission of next frame can be started.

Receive status word

At the end of Ethernet frame receiving, MAC will output the receiving state to DMA. The detailed description of receiving state is the same as RXDES0[31:0].

Frame length interface

The data transmission and receiving between the application and the MAC are conducted in the form of transmitting a complete frame. The application layer needs to know the length of the frame received from the inbound port in order to transmit the frame to the outbound port. The MAC core provides the length of each received frame at the end of receiving of each frame.

MII/RMII receive bit sequence

Each half byte is transmitted from the two bits received on RMII to MII, and the transmitting order is from low to high.

24.3.3.4 MAC interrupt

Various events can generate an interrupt to the MAC core, and the MAC_ISTS register describes various event interrupts. Setting the corresponding mask bit in the interrupt mask register can prevent event interrupts from being generated. The interrupt can be cleared by reading the corresponding state register and other registers.

24.3.3.5 MAC filtering

Address filtering

Check the destination address and source address of all received frames and report the corresponding address filtering state. The address check depends on the setting of the frame filter register. The filtered frames can be identified:

multicast frames or broadcast frames. Address filtering uses the MAC address of the station and the multi-broadcast list for address check.

Unicast destination address filtering

MAC supports 4 MAC addresses for unicast perfect filtering. If MAC_FRAF[HUC]=0, MAC will compare whether all 48 bits of the received unicast address match the set MAC address.

Multicast destination address filtering

The PM of MAC_FRAF register controls whether to set the MAC to pass all multicast frames. When the PM bit is reset, the HMC bit of the MAC_FRAF register controls the multicast address filtering.

Hash or perfect address filtering

When setting HPF bit, HUC bit ad HMC bit of MAC_FRAF register, DA filter is configured to allow frames to pass when its DA matches hash filter or perfect filter. This configuration is applicable to unicast and multicast frames. If the HPF bit is reset, there is only one filtering method.

Broadcast address filtering

In the default mode, the MAC does not filter broadcast frames. However, if MAC_FRAF[DISBF]=1, all broadcast frames will be discarded.

Unicast source address filtering

The MAC performs perfect filtering according to the source address of the received frame. By default, the MAC compares the SA field with the value in the SA register. When Bit 30 in the corresponding register is set, the MAC address register will be configured to contain SA for comparison. If MAC_FRAF[SAFEN]=0, the result of SA filtering will be presented in the status bit of the received status word. Otherwise, the MAC will discard the frames that do not pass SA filtering.

Reverse filtering

In the final output, the DAIF and SAIF bits of MAC_FRAF control the filtering of destination address and source address respectively. The DAIF bit is applicable to unicast and multicast Da frames. When this bit is set, the result of unicast/multicast destination address filtering will be reversed. When the SAIF bit is set, the result of unicast SA filtering will be reversed.

Table 98 Destination Address Filtering

Frame type	PR	HUC	HMC	DAIF	PM	DISBF	HPF	DA filtering operation
Broadcast	1	X	X	X	X	X	X	Pass
	0	X	X	X	X	0	X	Pass
	0	X	X	X	X	1	X	Fail
Unicast	1	X	X	X	X	X	X	All frames pass
	0	0	X	0	X	X	X	Pass when perfect/group filter matches
	0	0	X	1	X	X	X	Fail when perfect/group filter matches
	0	1	X	0	X	X	0	Pass when hash filter matches
	0	1	X	1	X	X	0	Fail when hash filter matches
	0	1	X	0	X	X	1	Pass when hash or perfect/group filter matches
	0	1	X	1	X	X	1	Fail when hash or perfect/group filter matches
Multicast	1	X	X	X	X	X	X	All frames pass
	X	X	X	X	1	X	X	All frames pass
	0	X	0	0	0	X	X	If PCTRLF=0x, pass when perfect/group filter matches, and discard the pause control frame
	0	X	1	0	0	X	0	If PCTRLF=0x, pass when hash filter matches, and discard the pause control frame
	0	X	1	0	0	X	1	If PCTRLF=0x, pass when hash or perfect/group filter matches, and discard the pause control frame
	0	X	0	1	0	X	X	If PCTRLF=0x, fail when perfect/group filter matches, and discard the pause control frame
	0	X	1	1	0	X	0	If PCTRLF=0x, fail when hash filter matches, and discard the pause control frame
	0	X	1	1	0	X	1	If PCTRLF=0x, fail when hash or perfect/group filter matches, and discard the pause control frame

Table 99 Source Address Filtering

Frame type	PR	SAIF	SAFEN	SA filtering operation
Unicast	1	X	X	All frames pass

Frame type	PR	SAIF	SAFEN	SA filtering operation
	0	0	0	Pass when perfect/group filter matches, but the pause control frame is not discarded
	0	1	0	Fail when perfect/group filter matches, but the frame is not discarded
	0	0	1	Pass when perfect/group filter matches, and discard the failed frames
	0	1	1	Fail when perfect/group filter matches, but the failed frames are not discarded

24.3.3.6 MAC loopback mode

MAC can loop back the received frames. This function is controlled by LBM bit of MAC_CFG register, and it is disabled by default.

24.3.3.7 MAC management counter (MMC)

MMC has a control register, two interrupt state registers, and two mask interrupt registers to collect information about received frames and transmitted frames. These registers are accessible from the application program.

Receive the MMC counter and update the frames that have passed address filtering. The discarded frame will not be updated unless the discarded frame is a short frame less than 6 bytes.

Good frame

（1） If there are no following errors during transmission, the transmitted frame is a “good frame”:

- Frame underrun
- No carrier/lost carrier
- Jabber timeout
- Delay conflict
- Excessive delay
- Excessive conflict

（2） If there are no following errors during receiving, the received frame is a “good frame”:

- Short frame
- CRC error
- MII_RXER input error
- Alignment error (for 10/100Mb/s only)
- Length error (for non-type frames only)
- Out of range (for non-type frames only, exceeding the maximum size)

（3） The frame type determines the maximum frame size as follows:

- Maximum size of untagged frame=1518
- Maximum size of VLAN frame=1522

24.3.3.8 Power management (PMT)

PMT supports receiving network remote wake-up frame and magic data packet frame. Interrupts can be generated for wake-up frames and magic data packet frames received by MAC. PMT module can be enabled by WKUPFEN bit and MPEN bit of MAC_PMTCTRLSTS register. When the power-down mode is enabled in the PMT, the MAC will discard all received frames and will not forward them to the application. The power-down mode will exit only when the remote wake-up frame or magic data packet frame is received and the corresponding detection is enabled.

Detect remote wake-up frame

When MAC is in sleep mode and MAC_PMTCTRLSTS[WKUPFEN]=1 is enabled, the MAC can resume normal work after receiving the remote wake-up frame.

Detect magic data packet

AMD Company's technology can be used to power on the devices which are in sleep mode on the network. MAC receives a specific information packet called magic data packet, and its address is the node on the network. Only the magic data packets that are transmitted to the device or multicast address are checked to determine whether they meet the wake-up requirements.

System precautions during power-down

When the EINT 19 interrupt line is enabled, the Ethernet PMT module can detect frames when the system is in stop mode. The MAC receiver state machine shall remain enabled in power-down mode.

24.3.3.9 Precision time protocol (IEEE 1588PTP)

The IEEE 1588 standard defines a protocol. It is suitable for systems that communicate through LAN supporting multicast message transmission and synchronous heterogeneous systems, including clocks with different fixing accuracy, resolution and stability. It supports precision clock synchronization in measurement and control systems which are realized by technologies such as network communication, LAN computing and distributed objects. It supports system-level synchronization accuracy within the subsecond range, and requires minimal network and local clock computing resources. This protocol, called precision time protocol, is transmitted through UDP/IP. The system or network is divided into master node and slave node, which are used to allocate timing/clock information. The protocol synchronizes the slave node to the master node by exchanging PTP messages.

Use PTP to transmit frames

The timestamp is captured when the SFD of the frame is output on the MII. Each transmitted frame may be tagged to indicate whether there is need to capture the timestamp of this frame. PTP frames can be identified without processing the transmitted frame. Transmit the control bit control frame in the descriptor. The captured timestamp is returned to the application in a manner of providing the frame state. The timestamp will be transmitted back to the corresponding transmit descriptor along with the transmission state of the frame, so that the timestamp can be connected with the specific PTP frame. The 64-bit timestamp information is written back to the TXDES2 and TXDES3 fields, wherein TXDES2 maintains the 32 least significant bits of the timestamp.

Use PTP to receive frames

When the IEEE 1588 timestamp function is enabled, the timestamps of all frames received on the MII will be captured by the Ethernet MAC. The MAC provides the timestamp when the frame receiving is completed. The captured timestamp is returned to the application in a manner of providing the frame state. The timestamp will be transmitted back to the corresponding receive descriptor along with the receiving state of the frame. The 64-bit timestamp information is written back to the RXDES2 and RXDES3 fields, wherein RXDES2 maintains the 32 least significant bits of the timestamp.

Reference timing source

To take a time snapshot, the core needs a 64-bit reference time. PTP reference clock input is used to generate reference time and capture timestamp internally. The frequency of the generated reference clock cannot be less than the resolution of the timestamp counter. The synchronization precision target between the master node and each slave node is about 100ns.

Calibration method

Synchronizing or updating the system time in a process is the coarse calibration method, and synchronizing or updating the system time in order to reduce the system time jitter is the precision calibration method.

System time calibration method

The 64-bit PTP time is refreshed by the PTP input reference clock HCLK. In order to obtain the timestamp of the Ethernet frame transmitted or received on the MII, this time is used as the clock source. The system time timer can be initialized or calibrated in coarse calibration or precision calibration method.

System time initialization

The timestamp function is controlled by TSEN bit of PTP_TSCTRL register. After setting, the timestamp can be enabled only by initializing the timestamp

counter.

PTP trigger connected internally to TMR2

In order to avoid the uncertainty of command execution time caused by use of interrupt when the system time is greater than the target time, the PTP trigger output signal internally connected to TMR2 input trigger can be set to high level when the system time is greater than the target time.

PTP pulse per second output signal

PTP pulse is used to check the synchronization of all nodes in the network. Two clocks can be provided with pulses per second (PPS) output signals to test the difference between the local slave clock and the master reference clock. The pulse width of PPS output is 125ms.

24.3.4 DMA controller

DMA is used for packet data transmission. The controller can be set to generate CPU interrupt under normal/error conditions such as completion of transmitting frames and receiving frames. DMA has separate transmitter and receiver and corresponding control and state registers. The transmitter transmits the data in the system memory to Tx FIFO, and the receiver transmits the data received by Rx FIFO to the system memory. DMA descriptor can transmit data from the source address to the destination address with minimal CPU intervention. The communication mode between DMA and CPU falls into the following two data structures:

- Control and state register
- Descriptor list and data buffer

24.3.4.1 Host bus burst access

DMA attempts fixed-length burst transmission on the AHB main interface. The maximum length of the burst depends on the PBL bit of ETH_DMABMOD register. The receive and transmit descriptors access the 16 bytes to be read with the maximum possible burst size.

24.3.4.2 Host data buffer alignment

The transmit and receive data buffers do not limit the start address alignment. In our system, the start address of the buffer can be aligned with any of the four bytes. DMA always starts transmission when the address is aligned with the bus width, and uses unnecessary byte channels to transmit empty data at the beginning or end of Ethernet frame transmission.

24.3.4.3 Calculate buffer size

DMA only updates the status of transmit and receive descriptors, not the size. The size needs to be calculated by the driver. Transmit DMA will transmit the

correct number of bytes to the MAC core.

24.3.4.4 DMA arbiter

The arbiter in DMA arbitrates between the transmitting channel and the receiving channel accessing the AHB main interface respectively. Circular scheduling and fixed priority arbitration can be used.

24.3.4.5 Error response to DMA

If the slave gives an error response to the data transmission initiated by the DMA channel, the corresponding DMA will stop all operations and update the FBERRFLG bit and ERRB bit in ETH_DMASTS register.

24.3.4.6 Tx DMA

Tx DMA contains two modes: default mode and OSF mode

Process transmitted frames

The expected data buffer of transmit DMA contains a complete Ethernet frame, excluding header, pad and FCS. The DA, SA, and type/length fields contain valid data. When the transmit descriptor indicates that the MAC core disables the insertion of CRC or pad, the buffer must have a complete Ethernet frame containing CRC bytes. The frame is bounded by the first descriptor and the last descriptor, which can be a data link or across multiple buffers.

Pause transmission polling

When DMA detects all descriptors and the TXBU bit of ETH_DMASTS register is set, the transmission polling will be suspended. Or when a transmission error caused by underrun is detected, the frame transmission will be aborted. The corresponding transmit descriptor 0 bit will be set to 1. If the second condition occurs, AINTS bit and TXUNF bit of ETH_DMASTS register will be set, and if the information is written to the transmission descriptor 0, the transmission polling will also be suspended.

24.3.4.7 Functional description of general transmit descriptor

The general transmit descriptor structure consists of four 32-bit words. If the timestamp is activated or IPv4 checksum offload is activated, the enhanced descriptor must be used.

Transmit descriptor word 0 (TXDES0)

Field	Name	R/W	Description
0	DEF	R/W	Deferred When this bit is set, it indicates that the MAC is delayed before transmission due to the existence of carrier. This bit is valid only in half-duplex mode. 0: No delay 1: Delay
1	UFERR	R/W	Underflow Error When this bit is set, it indicates the MAC terminates the frame because the data arrives late from the host memory. The underflow error indicates that the DMA encountered an empty transmit buffer while transmitting frames. The transmitting process enters the pending state.
2	EDEF	R/W	Excessive Deferral If MAC_CFG[4] is set to 1, this bit indicates that transmission has been over.
6:3	CCNT	R/W	Collision Count The value of this bit field indicates the number of collision that occurs before frame transmission. Invalid when TXDES0[8] is set to 1.
7	VLANF	R/W	VLAN Frame When this bit is set, it indicates that the transmitted frame is a frame of VLAN type.
8	EC	R/W	Excessive Collision When this bit is set, it indicates that the transmission is terminated after 16 consecutive collisions when trying to transmit the current frame. If MAC_CFG[9] is set, this bit will be set after the first collision, and the transmission of the frame will be terminated.
9	LC	R/W	Late Collision When this bit is set, it indicates that the frame transmission is terminated due to a collision after the collision window. This bit is invalid if underflow error is set.
10	NC	R/W	No Carrier When this bit is set, it indicates that the carrier detection signal of PHY is continuously formed during transmission.
11	LSC	R/W	Loss of Carrier When this bit is set, it indicates that the carrier is lost during frame transmission. Only when the MAC works in half-duplex mode, it is valid for frames transmitted without conflict.
12	IPERR	R/W	IP Payload Error When this bit is set to 1, it indicates that the MAC transmitter detects an error in the TCP, UDP, or ICMP IP packet payload. The transmitter will check the payload length received in the IPv4 or IPv6 header according to the actual number of bytes of TCP, UDP or ICMP IP packets received from the application program. If there is mismatch, the error status will be displayed.
13	FF	R/W	Frame Flushed When this bit is set, it indicates that DMA or MTL refreshes the frame due to the software refresh command given by the CPU.

Field	Name	R/W	Description
14	JTO	R/W	Jabber Timeout When this bit is set, it indicates that the MAC transmitter has experienced a jabber timeout. This bit can be set only when JDIS bit of MAC_CFG register is not set.
15	ERRS	R/W	Error Summary The value is OR operation result of the following bits: TXDES0[1]：UFERR TXDES0[2]：EDEF TXDES0[8]：EC TXDES0[9]：LC TXDES0[10]：NC TXDES0[11]：LSC TXDES0[12]：IPERR TXDES0[13]：FF TXDES0[14]：JTO TXDES0[16]：IHERR
16	IHERR	R/W	IP Header Error When this bit is set to 1, it indicates that the MAC transmitter has detected an error in the IP data header. The transmitter will check the header length of IPv4 packets according to the number of header bytes received from the application program. If there is a mismatch, it indicates the error status. If the main header length of IPv6 frame is not 40 bytes, a header error will be reported. If the value of the header length field of IPv4 frame is less than 0x5, a header error will also be reported. Besides, the Ethernet length/type field value of IPv4 or IPv6 frame must match the IP header version received along with the data packet.
17	TXTSS	R/W	TX Timestamp Status This status bit indicates that the timestamp of the corresponding transmitted frame has been captured. When this bit is set, TXDES2 and TXDES3 have the timestamp values captured for the transmitted frames. This bit field is valid only when the last control bit (TXDES0[29]) in the descriptor is set. When the enhanced descriptor is enabled, TXTSS=1 indicates that there is timestamp value in TXDES6 and TXDES7.
19:18	Reserved		
20	TXCH	R/W	Second Address Chained When this bit is set to 1, the second address in the descriptor is the address of the next descriptor, not the address of the second buffer, and TXDES1[28:16] is "irrelevant" value. The priority of TXDES0[21] is higher than TXDES0[20].
21	TXENDR	R/W	Transmit End of Ring When this bit is set to 1, the descriptor list has reached the last descriptor. DMA will return the base address of the descriptor list and form a descriptor ring.

Field	Name	R/W	Description
23:22	CHINS	R/W	Checksum Insertion Control These bits control the calculation and insertion of checksum. The bit codes are as follows: 00: Disable checksum insertion 01: Enable calculation and insertion of IP header checksum 10: Enable the calculation and insertion of payload checksum and IP header checksum, but the pseudo header checksum will not be calculated in hardware 11: Enable the calculation and insertion of payload checksum and IP header checksum, and the pseudo header checksum will be calculated in hardware.
24	Reserved		
25	TXTSEN	R/W	Transmit Timestamp Enable When this bit is set to 1 and TSEN is set to 1, the IEEE1588 hardware timestamp function will be activated for the transmitted frame described in the descriptor. This bit is valid only when TXDES0[28]=1.
26	DISP	R/W	Disable Pad 0: DMA will automatically add complementary bit item and CRC for frames less than 64 bytes. Whether to add CRC field has nothing to do with TXDES0[27] 1: MAC will not automatically add complementary bit item for frames less than 64 bytes This bit is valid only when TXDES0[28]=1.
27	DISC	R/W	Disable CRC When this bit is set to 1, MAC will not attach the CRC to the end of the transmitted frame. This bit is valid only when TXDES0[28]=1.
28	FS	R/W	First Segment When this bit is set to 1, it indicates that the buffer includes the first segment of the frame.
29	LS	R/W	Last Segment When this bit is set to 1, it indicates that the buffer includes the last segment of the frame.
30	INTC	R/W	Interrupt on Completion When this bit is set to 1, after transmission of current frame is completed, an interrupt will be transmitted.
31	OWN	R/W	Own 0: This describer belongs to CPU 1: This describer belongs to DMA DMA will clear this bit when the frame transmission is completed or the buffer allocated in the descriptor is empty. All bits of the first descriptor of this frame should be set after all subsequent descriptors belonging to the same frame are set.

Transmit descriptor word 1 (TXDES1)

Field	Name	R/W	Description
12:0	TXBS1	R/W	Transmit Buffer 1 Size These bits indicate the size of the first data buffer. If the bit is 0, DMA will ignore this buffer and use the buffer 2 or the next descriptor, depending on the value of TXDES0[20].
15:13	Reserved		
28:16	TXBS2	R/W	Transmit Buffer 2 Size These bits indicate the size of the second data buffer in bytes. If TXDES0[20]=1, this field will be invalid.
31:29	Reserved		

Transmit descriptor word 2 (TXDES2)

Field	Name	R/W	Description
31:0	TXADDR1_TXFTSL	R/W	Transmit Buffer 1 Address Pointer / Transmit frame timestamp low It indicates the location of the data in the memory to the DMA. When all data have been transmitted, the DMA can use these bits to return the timestamp data. TXADDR1: When TXDES0[31]=1, these bits indicate the physical address of buffer 1. There are no restrictions on buffer address alignment. TXFTSL: Before TXDES0[31] is cleared to zero, the DMA will update this field with the 32 least significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when the timestamp function of this frame is activated and LS=1.

Transmit descriptor word 3 (TXDES3)

Field	Name	R/W	Description
31:0	TXADDR2_TXFTSH	R/W	Transmit Buffer 2 Address Pointer (Next descriptor address) / Transmit frame timestamp high It indicates the location of the data in the memory to the DMA. When all data have been transmitted, the DMA can use these bits to return the timestamp data. TXADDR2: When TXDES0[31]=1 and the descriptor ring structure is used, these bits indicate the physical address of buffer 2. If TXDES1[24]=1, this address contains the pointer of the physical register where the next descriptor is located. The buffer address pointer matches the bus width only when TXDES1[24]=1. TXFTSH: Before TXDES0[31] is cleared to zero, the DMA will update this field with the 32 most significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when the timestamp function of this frame is activated and LS=1.

24.3.4.8 Rx DMA

Obtain receiving descriptor

The receiver always tries to get an additional descriptor to add to the frame to be received. It will attempt to obtain the descriptor when any of the following operations occurs:

（1） The command of receiving polling requirements has been issued

（2） After DMA runs, the STRX bit of ETH_DMAOPMOD register is immediately set

（3） The descriptor data buffer is full before the end of the currently transmitted frame

（4） The receiving process is suspended because RDES0[OWN]=0, and a new frame is received

（5） The receive data frame is completed, but the receive descriptor is not disabled

Process received frames

The MAC will transmit the received frames to the memory only when the frame whose size is not less than the threshold number of bytes set for the receive FIFO passes the address filtering, or when the whole frame is written to the FIFO in the storage and forwarding mode.

Stop when receiving

If a new received frame is detected when the receiving process is suspended, the DMA will obtain the current descriptor in memory again. If the descriptor is owned by DMA, the frame will be received again. If it is owned by the host, by default, the DMA will discard the current frame at the top of Rx FIFO and the lost frame counter will increase. If multiple frames are stored in Rx FIFO, the above process will be repeated. After DISFRXF bit of ETH_DMAOPMOD register is set, it can avoid discarding or refreshing the frame at the top of the Rx FIFO. At this time, RXBU bit is set to 1 and the receiving process returns to the suspended state.

24.3.4.9 Functional description of general receive descriptor

The general receive descriptor structure consists of four 32-bit words. If the timestamp function or IPv4 checksum offload is activated, the enhanced descriptor must be used.

Receive descriptor word 0 (RXDES0)

Field	Name	R/W	Description
0	PERR_ESA	R/W	Payload Checksum Error / extended status available When this bit is set, the TCP, UDP or ICMP checksum calculated by the core does not match the checksum field of the received encapsulated TCP, UDP or ICMP segment. This bit will also be set when the number of payload bytes received does not match the value of the length field of the IPv4 or IPv6 datagram encapsulated in the received Ethernet frame. After the enhanced descriptor format is enabled, this bit has ESA functions. When ESA is set to 1, it indicates that there is an extended state in RXDES4. ESA is valid only when RXDES0[8]=1.
1	CERR	R/W	CRC Error When this bit is set, a CRC error will occur on the received frame. This bit is valid only when RXDES0[8]=1
2	DERR	R/W	Dribble Error When this bit is set, the received frame has a multiple of non-integer bytes. This bit is valid only in MII mode.
3	RERR	R/W	Receive Error When this bit is set and RX_DV signal is transmitted during frame receiving, RX_ERR signal will be generated.
4	RXWDTTO	R/W	Receive Watchdog Timeout When this bit is set, the receive watchdog timer has timed out when receiving the current frame, and the current frame will be truncated when the watchdog times out.
5	FT	R/W	Frame Type 0: The received frame is an Ethernet type frame 1: The received frame is an IEEE802.3 frame When this bit is set. When this bit is reset, it indicates that this bit is invalid for short frames less than 14 bytes.
6	LC	R/W	Late Collision When this bit is set, a delay collision occurs when a frame is received in half-duplex mode.
7	IPCERR_TSV	R/W	IPv header Checksum Error / Time Stamp Valid When this bit is set, there is an error in the IPv4 or IPv6 header. The reasons may be: the Ethernet type field is inconsistent with the IP header version field, and does not match the checksum of the header in IPv4, or the Ethernet frame lacks the required number of IP header bytes. After the enhanced descriptor format is enabled, this bit has TSV functions. When TSV=1, it indicates that the timestamp snapshot will be written in RXDES6 and RXDES7. TSV is valid only when RXDES0[8]=1.
8	LDES	R/W	Last Descriptor When this bit is set, the buffer pointed to by the descriptor is the last buffer of the frame.
9	FDES	R/W	First Descriptor When this bit is set, the descriptor contains the first buffer of the frame. If the size of the first buffer is 0, the second buffer contains the beginning of the frame. If the size of the second buffer is also 0, the next descriptor contains the beginning of the frame.

Field	Name	R/W	Description
10	VLANF	R/W	VLAN Frame When this bit is set, the frame referred to by this descriptor is a VLAN frame with MAC tag.
11	OFERR	R/W	Overflow Error When this bit is set, the received frame is damaged due to buffer overflow in Rx FIFO.
12	LERR	R/W	Length Error When this bit is set, the actual length of the received frame does not match the length/type field. This bit is valid only when RXDES0[5]=0.
13	SADDRF	R/W	Source Address Filter Fail When this bit is set, the SA field of the frame does not pass the SA filter in the MAC.
14	DESERR	R/W	Descriptor Error When this bit is set, it indicates that the frame is truncated because the frame is not suitable for the current descriptor buffer, and DMA has no next descriptor. The frame is truncated. Note: This field is valid only when the last descriptor (RXDES0[8]) is set.
15	ERRS	R/W	Error Summary The value is OR operation result of the following bits: RXDES0[0]：PERR_ESA RXDES0[1]：CERR RXDES0[3]：RERR RXDES0[4]：RXWDTTO RXDES0[6]：LC RXDES0[7]：IPCERR_TSV RXDES0[11]：OFERR RXDES0[14]：DESERR
29:16	FL	R/W	Frame Length This bit field indicates the byte length of the received frame transmitted to the host memory. This bit is valid only only when RXDES0[8] =1 and RXDES0[14])=0. When RXDES0[8]=0 and ERRS=0, it indicates the cumulative number of bytes that have been transmitted to the current frame.
30	ADDRF	R/W	Destination Address Filter Fail When this bit is set, it indicates the frame that fails DA filtering in MAC.
31	OWN	R/W	Own 0: This describer belongs to CPU 1: This describer belongs to DMA This bit will be cleared when DMA completes frame receiving or the allocated buffer in the descriptor is full.

Table 82 Configuration in Normal Descriptor Format

Bit 0 (PERRC_ESA)	Bit 5 (FT)	Bit 7 (IPCERR_TSV)	Frame state
0	0	0	IEEE 802.3 type frame

Bit 0 (PERRC_ESA)	Bit 5 (FT)	Bit 7 (IPCERR_TSV)	Frame state
1	0	1	Type frame which is neither IPv4 nor IPv6
0	1	0	IPv4/IPv6 type frame; checksum error is not detected
1	1	0	IPv4/IPv6 type frame; payload checksum error is detected
0	1	1	IPv4/IPv6 type frame; IP header checksum error is detected
1	1	1	IPv4/IPv6 type frame; IP header and payload checksum error are detected
1	0	0	IPv4/IPv6 type frame; there is no IP header checksum error, and the payload check bypasses because the payload is not supported
0	0	1	Reserved

Receive descriptor word 1 (RXDES1)

Field	Name	R/W	Description
12:0	RXBS1	R/W	Receive Buffer 1 Size 0: DMA will ignore this buffer and use the buffer 2 or the next descriptor according to the value of RXCH bit. Other: It indicates the size of the first data buffer. The buffer size must be a multiple of 4, 8, or 16, depending on the bus width, even if the value of the buffer 2 address pointer is not aligned. When the buffer size is not a multiple of 4, 8, or 16, the generated behavior is undefined.
13	Reserved		
14	RXCH	R/W	Second Address Chained When this bit is set, the second address in the descriptor is the address of the next descriptor, not the address of the second buffer. Ignore the value of RXBS2. RXER has priority over RXCH.
15	RXER	R/W	Receive End of Ring When this bit is set, it indicates that the descriptor list has reached the final descriptor. DMA will return the base address of the descriptor list and create a descriptor ring.
28:16	RXBS2	R/W	Receive Buffer 2 Size It indicates the size of the second data buffer. The buffer size must be a multiple of 4, 8, or 16, depending on the bus width, even if the value of the buffer 1 address pointer is not aligned. When the buffer size is not a multiple of 4, 8, or 16, the generated behavior is undefined. This bit field will be invalid if RXCH bit is set.
30:29	Reserved		
31	DINTC	R/W	Interrupt on Completion Disable When this bit is set, it will prevent the setting of RXFLG bit and make the received frame end in the buffer indicated by the descriptor, so as to disable causing the host interrupt.

Receive descriptor word 2 (RXDES2)

Field	Name	R/W	Description
31:0	RXADDR1_RXFTSL	R/W	Receive Buffer 1 Address Pointer / Receive Frame Timestamp Low It indicates the location of the data in the memory to the DMA. When all data have been transmitted, the DMA can use these bits to return the timestamp data. RXADDR1: When RXDES0[OWN]=1, these bits indicate physical address of the buffer 1. Except when the starting point of the frame is stored by using the value of RXDES2, the address is generated by DMA by using the configured value. During the start of transmitted frame, the DMA will perform write operation when RXDES2[3:0]=0, but the frame data will be shifted according to the actual buffer address pointer. When the address pointer points to the buffer where the middle or last part of the frame is stored, the DMA will ignore RXDES2[3:0]. There are no restrictions on buffer address alignment. RXFTSL: Before RXDES0[OWN] is cleared to zero, the DMA will update this field with the 32 least significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when the timestamp function of this frame is activated and LS=1.

Receive descriptor word 3 (RXDES3)

Field	Name	R/W	Description
31:0	RXADDR2_RXFTSH	R/W	Receive Buffer 2 Address Pointer (Next Descriptor Address) / Receive Frame Timestamp High It indicates the location of the data in the memory to the DMA. When all data have been transmitted, the DMA can use these bits to return the timestamp data. RXADDR1: When RXDES0[OWN]=1 and the descriptor ring structure is used, these bits indicate the physical address of buffer 2. If RXDES[24]=1, this address contains the pointer of the physical register where the next descriptor is located. The buffer address pointer matches the bus width only when RXDES1[24]=1. When RXDES[24]=0, except when the starting point of the frame is stored by using the value of RXDES2, the address is generated by DMA by using the configured value. When the address pointer points to the buffer where the middle or last part of the frame is stored, the DMA will ignore RXDES2[3:0], and there are no restrictions on buffer address alignment. RXFTSH: Before RXDES0[OWN] is cleared to zero, the DMA will update this field with the 32 least significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when the timestamp function of this frame is activated and LS=1.

24.3.4.10 DMA interrupt

There are two groups of interrupts: normal interrupt and abnormal interrupt. The

interrupt can be cleared by writing to the corresponding bit of ETH_DMASTS register. When all enabled interrupts in the group are cleared, the summary bit will also be cleared to zero. If the interrupt is caused by the MAC core, the PMTFLG or TSTFLG bits in the ETH_DMASTS register will be set to high level.

24.3.5 Ethernet interrupt

The Ethernet controller has two interrupt vectors: one for normal Ethernet operation and one for Ethernet wake-up events only when mapped to EINT 19. The first Ethernet vector is reserved for interrupts generated by MAC and DMA. The second is reserved for interrupts generated by PMT when a wake-up event occurs. The mapping of the wake-up event to EINT 19 makes the core exit the low-power mode and generate an interrupt.

When the Ethernet wake-up event mapped to EINT 19 occurs and both MAC PMT interrupt and EINT 19 interrupt with rising edge detection are enabled, two interrupts will be generated.

24.4 MAC register address mapping

Table 83 Register Address Mapping

Register name	Description	Offset address
MAC_CFG	Configuration register	0x00
MAC_FRAF	Frame filter register	0x04
MAC_HTH	Hash table high-bit register	0x08
MAC_HTL	Hash table low-bit register	0x0C
MAC_ADDR	MII address register	0x10
MAC_DATA	MII data regisster	0x14
MAC_FCTRL	Receive flow control register	0x18
MAC_VLANT	VLAN tag register	0x1C
MAC_REMWKUPFFL	Remote wake-up frame filter register	0x28
MAC_PMTCTRLSTS	PMT control and state register	0x2C
MAC_ISTS	Interrupt state register	0x38
MAC_IMASK	Interrupt mask register	0x3C
MAC_ADDR0H	MAC address 0 high register	0x40
MAC_ADDR0L	MAC address 0 low register	0x44
MAC_ADDR1H	MAC address 1 high register	0x48
MAC_ADDR1L	MAC address 1 low register	0x4C
MAC_ADDR2H	MAC address 2 high register	0x50

Register name	Description	Offset address
MAC_ADDR2L	MAC address 2 low register	0x54
MAC_ADDR3H	MAC address 3 high register	0x58
MAC_ADDR3L	MAC address 3 low register	0x5C

24.5 MAC register functional description

24.5.1 Configuration register (MAC_CFG)

Offset address: 0x00

Reset value: 0x0000 8000

Field	Name	R/W	Description
1:0	Reserved		
2	RXEN	R/W	Receiver Enable The receiving state machine of MAC can receive frames from MII. After this bit is set, the receiving state machine of MAC will be turned off after the current frame is received, and will receive no frame from the MII.
3	TXEN	R/W	Transmitter Enable The transmitting state machine of MAC can transmit on MII. After this bit is set, the transmitting state machine of MAC will be turned off after the current frame is transmitted, and will transmit no frame.
4	DC	R/W	Deferral Check The deferral check function enables MAC. When the delay of the transmitting state machine exceeds the mode of 24288 bits multiplied by 10 or 100 Mbps, the MAC will identify the frame aborted state, and set the excessive delay error in the transmitted frame state. When the bit is reset, the bit will disable the deferral check function until the CRS signal becomes an invalid signal, and the MAC will be delayed. This bit is applicable only in half-duplex mode.
6:5	BL	R/W	Back off Limit This bit determines the random integer (r) of the time delay (4096-bit time for 1000Mbps and 512-bit time for 10/100Mbps) that the MAC waits before retransmission attempt when retrying after collision. This bit is applicable only in half-duplex mode. 00：k=min(n，10) 01：k=min(n，8) 10：k=min(n，4) 11：k= min(n，1) Wherein, n=the number of retransmission attempts. The value range of random integer r is $0 \le r < 2^k$
7	ACS	R/W	Automatic Pad or CRC Stripping Only when the bit length of MAC is less than 1536 bytes, will Pad or FCS be removed when the frame comes in. All received frames with bit length greater than or equal to 1536 bytes are passed to the application program without removing Pad or FCS. When this bit is reset, the MAC will transmit all incoming frames to the host without modification.
8	Reserved		

Field	Name	R/W	Description
9	DISR	R/W	Disable Retry MAC will try to transmit once only. When a collision occurs to the MII interface, the MAC will ignore transmission of the current frame and report the abortion of a frame with a large collision error in the transmitted frame state. When this bit is reset, retry the MAC according to the setting of BL bit. This bit is applicable only in half-duplex mode.
10	IPC	R/W	IPv4 Checksum Offload The MAC calculates all 16-bit 1 complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 header checksum of the received Ethernet frame is correct, and gives the state in the receiving state word. This function is disabled when this bit is reset.
11	DM	R/W	Duplex Mode MAC works in full-duplex mode and can transmit and receive at the same time.
12	LBM	R/W	Loopback Mode When this bit is set, the MAC will run in loopback mode on the MII. The MII receive clock input (RX_CLK) needs to work in loopback mode normally, because there is no loopback in the transmit clock.
13	DISRXO	R/W	Disable Receive Own When it is confirmed that phy_txen_o is in half-duplex mode, MAC will disable receiving frames. When this bit is reset, MAC will receive all packets transmitted by PHY. This bit is not applicable if the MAC is working in full-duplex mode.
14	SSEL	R/W	Speed select 0：10Mbps 1：100Mbps
15	Reserved		
16	DISCRS	R/W	Disable Carrier Sense During Transmission When it is set to high, the MAC transmitter will ignore the MII CRS signal during frame transmission in half-duplex mode. This request results in no error due to carrier loss or no carrier in such transmission process. When it is set to low, the MAC transmitter will generate a carrier sense error and can even abort the transmission.
19:17	IFG	R/W	Inter-Frame Gap These bits are used to control the minimum gap between frames during transmission. 000: 96-bit time 001: 88-bit time 010: 80-bit time … 111: 40-bit time In half-duplex mode, the minimum IFG can only be configured as 64 bits (IFG=100), and lower value will not be considered.
21:20	Reserved		

Field	Name	R/W	Description
22	JDIS	R/W	Jabber Disable The MAC disables the Jabber timer on transmitting end. MAC can transmit up to 16384 bytes frames. When this bit is reset, if the application program transmits more than 2048 bytes of data during transmission, the MAC will cut off the transmitter.
23	WDTDIS	R/W	Watchdog Disable The MAC disables the watchdog timer on the receiving end. The MAC can receive up to 16384 bytes of frames. When this bit is reset, the MAC does not allow the received frame to exceed 2048 bytes or the watchdog timeout register. After the watchdog limits the number of bytes, the MAC will disable receiving any bytes.
31:24	Reserved		

24.5.2 Frame filter register (MAC_FRAF)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	PR	R/W	Promiscuous Mode The address filtering module will pass all incoming frames, regardless of destination address or source address. The SA or DA state bits of the receiving state word are always cleared.
1	HUC	R/W	Hash Unicast The MAC filters the destination address of unicast frames according to the hash table. After reset, the MAC performs perfect destination address filtering on unicast frames, which compares the DA field with the value programmed in the DA register.
2	HMC	R/W	Hash Multicast The MAC filters the destination address of received multicast frames according to the hash table. After reset, the MAC performs perfect destination address filtering on multicast frames, which compares the DA field with the value programmed in the DA register.
3	DAIF	R/W	DA Inverse Filtering The address check block compares the DA addresses of unicast and multicast frames in inverse filtering method. After reset, normal frame filtering will be performed.
4	PM	R/W	Pass All Multicast All received frames whose destination address is multicast address (the first field of the destination address fields is 1) will be delivered. The filtering of multicast frames after reset depends on HMC bit.
5	DISBF	R/W	Disable Broadcast Frames The address filter will filter all incoming broadcast frames. After reset, the address filter will transmit all received broadcast frames.
7:6	PCTRLF	R/W	Pass Control Frames These bits control the forwarding of all control frames (including unicast and multicast pause frames). 0x: MAC filters all control frames arriving at the application program. 10: Even if the control frames do not pass the address filter, the MAC will also forward them to the application program.

Field	Name	R/W	Description
			11: MAC forwards the control frames that pass the address filtering. Note: MAC is enabled to full-duplex mode when RXFCTRLEN bit of MAC_FCTRL is set.
8	SAIF	R/W	SA Inverse Filtering The address check block compares the addresses of SA in inverse filtering method. SA frames that match the SA register will be marked as SA address filter failure. After reset, the SA frames that do not match the SA register will be marked as SA address filter failure.
9	SAFEN	R/W	Source Address Filter Enable The MAC compares the SA field of the received frame with the value programmed in the enabled SA register. If the comparison fails, the MAC will discard the frame. After reset, the MAC will forward the received frames to the application program of receiving state for updating SAFEN bit.
10	HPF	R/W	Hash or Perfect Filter If it matches the perfect filter or Hash filter set for the HMC or HUC bit, it will configure the address filter to pass the frame. When this bit is low and the HUC or HMC bit is set, the frame will be passed only when the Hash filter matches.
30:11	Reserved		
31	RXA	R/W	Receive All The MAC receiving module will transmit all received frames, regardless of whether they pass the address filter. The result of SA or Da filtering is updated in the corresponding bit of the receiving state word. When this bit is reset, the receiving module will only pass these frames to the application program that passes the SA or DA address filter.

24.5.3 Hash table high-bit register (MAC_HTH)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	HTH	R/W	Hash Table High High 32 bits of Hash table.

24.5.4 Hash table low-bit register (MAC_HTL)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	HTL	R/W	Hash Table Low Low 32 bits of Hash table.

24.5.5 MII address register (MAC_ADDR)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	MB	R/W	MII Busy Write to MAC_HT register and this bit will be valid. During PHY register access period, the software sets this bit to 1, indicating that read or write access is in progress. Therefore, MII data should remain valid in a PHY write operation until the MAC clears this bit. For read operation, MAC_HT is valid after this bit is cleared. Subsequent read and write operation can be performed only after the previous operation is completed.
1	MW	R/W	MII Write For PHY, this bit indicates that this is a write operation using the MII data register. If this bit is not set, it indicates that this is a read operation and the data will be put in the MII data register.
4:2	CR	R/W	Clock Range The selection of CR clock range determines the frequency of HCLK and is used to determine the frequency of MDC clock: Select HCLK MDC clock 000：60-100 MHz-HCLK/42 001：Reserved 010：20-35 MHz-HCLK/16 011：35-60 MHz-HCLK/26 100, 101, 110, 111: Reserved
5	Reserved		
10:6	MR	R/W	MII Register These bits select the required register in the selected PHY devices.
15:11	PA	R/W	Physical Layer Address It indicates which of the 32 possible PHY devices are being accessed.
31:16	Reserved		

24.5.6 MII data register (MAC_DATA)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	MD	R/W	MII Data The 16-bit data value read from PHY after performing the management of read operation, or the 16-bit data value written to PHY before performing the management of write operation.
31:16	Reserved		

24.5.7 Receive flow control register (MAC_FCTRL)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	FCTRLB/BPA	R/W	Flow Control Busy/Back Pressure Activate When a pause control frame is initiated in full-duplex mode, this bit should be read as 0 before it is written to the flow control register. Only when the application program sets this bit to 1, can a pause control frame be initialized. During the transmission of the control frame, this bit continues to be set to indicate that the frame transmission is in progress. After the transmission of the pause control frame is completed, the MAC will reset this bit to 0. It cannot be written to the flow control register before this bit is cleared. In half-duplex mode, if the TXFCTRLEN bit is set, the back pressure function will be activated. When this bit is set (and TXFCTRLEN is set), the back pressure will be declared by the MAC core. During back pressure period, when the MAC receives a new frame, the transmitter starts to transmit JAM mode, which causes collision. When MAC is configured as full-duplex mode, BPA will be automatically disabled.
1	TXFCTRLEN	R/W	Transmit Flow Control Enable In full-duplex mode, when this bit is set, MAC will enable the flow control operation to transmit the pause frame. When this bit is reset, the flow control operation of MAC will be disabled, and MAC will not transmit any pause frame. In half-duplex mode, when this bit is set, the MAC will enable back pressure operation. When this bit is reset, the back pressure characteristic will be disabled.
2	RXFCTRLEN	R/W	Receive Flow Control Enable When this bit is set, the MAC will decode the received pause frame and disable its transmitter within the specified pause time. When this bit is reset, the decoding function of the pause frame will be disabled.
3	UNPFDETE	R/W	Unicast Pause Frame Detect When this bit is set, the MAC uses the unique multicast address to detect the pause frames, and also uses the specified unicast address in the MAC_ADDR0H and MAC_ADDR0L registers to detect the pause frame. When this bit is reset, the MAC only detects the pause frame of the unique multicast address specified in the 802.3x standard.
5:4	PTSEL	R/W	Pause Threshold Select Set the threshold of Pause timer for automatic retransmission of pause frames. The threshold should always be less than the pause time configured by bit [31:16]. For example, if PT = 100H (256 slot time) and PTSEL =01, and the second PAUSE frame is initiated at 228 (256-28) slot time after the first PAUSE frame is transmitted, the second Pause frame will be automatically transmitted. Select the threshold 00: Pause time - 4-slot time 01: Pause time - 28-slot time 10: Pause time - 144-slot time 11: Pause time - 256-slot time The slot time is defined as the time that the MII interface takes to transmit 512 bits (64 bytes)

Field	Name	R/W	Description
6	Reserved		
7	ZQPDIS	R/W	Zero-quanta Pause Disable When this bit is set, it is disabled to automatically generate zero-range pause control frame when the flow control signal of FIFO layer fails. When this bit is reset, normal operation of automatic zero-range pause control frame generation is enabled.
15:8	Reserved		
31:16	PT	R/W	Pause Time This bit saves the value used in the transmission of control frame. If this bit is configured to be double synchronized to the MII clock domain, continuous write operations should be performed on the register only after at least 4 clock cycles in the target clock domain.

24.5.8 VLAN tag register (MAC_VLANT)

Offset address: 0x1C

Reset value: 0x0000 0000

This register contains the IEEE 802.1Q VLAN tag, used to identify the VLAN frame. The MAC compares No. 13 and No. 14 bytes of the received frame (length/type) with 0x8100, and compares the next 2 bytes with VLAN tag; if the match is successful, set the receive VLAN bit of the received frame state. The legal length of the frame increases from 1518 bytes to 1522 bytes.

Field	Name	R/W	Description
15:0	VLANTID	R/W	VLAN Tag Identifier It contains 802.1Q VLAN tag, which is used to identify VLAN frames and compare them with No. 15 byte and No. 16 byte of the received frame. Bit [15:13] is the user priority, bit [12] is the canonical format indicator, and bit [11:0] is the VLAN identifier of the VLAN tag. When the VLANTCOMP bit is set, only bit [11:0] is used for comparison. If VLANTID is all 0, the MAC does not check the VLAN tag comparison of No. 15 byte and No. 16 byte, and declares all frames with Type value of 0x8100 as VLAN frames.
16	VLANTCOMP	R/W	12-bit VLAN Tag Comparison When this bit is set, the VLAN identifier of bit 12 instead of the complete 16-bit VLAN tag will be used for comparison and filtering. The VLAN tag bit [11:0] is compared with the corresponding bit in the received VLAN tag frame. When this bit is reset, all 16 bits of No. 15 and No. 16 bytes of the received VLAN frame will be used for comparison.
31:17	Reserved		

24.5.9 Remote wake-up frame filter register (MAC_REMWKUPFFL)

Offset address: 0x28

Reset value: 0x0000 0000

The application program will write/read the remote wake-up frame filter register through this address. In fact, the wake-up frame filter register is eight (opaque) wake-up frame filter registers. Eight continuous write operations to this address

of the offset (0x0028) will write/read all wake-up frame filter registers. This register contains the high 16 bits of the seventh MAC address.

Wake-up frame filter register x (MAC_WKUPFFLx) (x=0-3)

Field	Name	R/W	Description
31:0	FLXBMASK	R/W	Filter x Byte Mask This register defines which bytes of the frame are detected by the filter x to determine whether the frame is a wake-up frame. MSB[31] must be zero. Bit y[30:0] is byte mask. If the bit y (the number of bytes) of byte mask is set to 1, the filter x offset + y of the incoming frame will be processed by the CRC module; otherwise, the filter x offset + y will be ignored.

Wake-up frame filter register 4 (MAC_WKUPFFL4)

Field	Name	R/W	Description
3:0	FL0COM	R/W	Filter 0 Command This 4-bit command controls filter x operation. Bit 3 specifies the address type and defines the destination address type of the mode. When this bit is set to 1, the mode is applicable only to multicast frames. When this bit is reset, the mode is applicable only to unicast frames. Bit 2 and Bit 1 are reserved bits. Bit 0 is the enable bit of filter X; if bit 0 is set to 1, filter x will be enabled.
7:4	Reserved		
11:8	FL1COM	R/W	Filter 1 Command This 4-bit command controls filter x operation. Bit 3 specifies the address type and defines the destination address type of the mode. When this bit is set to 1, the mode is applicable only to multicast frames. When this bit is reset, the mode is applicable only to unicast frames. Bit 2 and Bit 1 are reserved bits. Bit 0 is the enable bit of filter X; if bit 0 is set to 1, filter x will be enabled.
15:12	Reserved		
19:16	FL2COM	R/W	Filter 2 Command This 4-bit command controls filter x operation. Bit 3 specifies the address type and defines the destination address type of the mode. When this bit is set to 1, the mode is applicable only to multicast frames. When this bit is reset, the mode is applicable only to unicast frames. Bit 2 and Bit 1 are reserved bits. Bit 0 is the enable bit of filter X; if bit 0 is set to 1, filter x will be enabled.
23:20	Reserved		
27:24	FL3COM	R/W	Filter 3 Command This 4-bit command controls filter x operation. Bit 3 specifies the address type and defines the destination address type of the mode. When this bit is set to 1, the mode is applicable only to multicast frames. When this bit is reset, the mode is applicable only to unicast frames. Bit 2 and Bit 1 are reserved bits. Bit 0 is the enable bit of filter X; if bit 0 is set to 1, filter x will be enabled.
31:28	Reserved		

Wake-up frame filter register 5 (MAC_WKUPFFL5)

Field	Name	R/W	Description
7:0	FL0OFF	R/W	Filter 0 Offset This register defines the offset (within the frame range) of the frame to be detected by the filter x. This 8-bit mode offset is the offset of the first byte of the filter x to be detected. The minimum allowable value is 12, which indicates the 13th byte of the frame (the offset value 0 indicates the first byte of the frame).
15:8	FL1OFF	R/W	Filter 1 Offset This register defines the offset (within the frame range) of the frame to be detected by the filter x. This 8-bit mode offset is the offset of the first byte of the filter x to be detected. The minimum allowable value is 12, which indicates the 13th byte of the frame (the offset value 0 indicates the first byte of the frame).
23:16	FL2OFF	R/W	Filter 2 Offset This register defines the offset (within the frame range) of the frame to be detected by the filter x. This 8-bit mode offset is the offset of the first byte of the filter x to be detected. The minimum allowable value is 12, which indicates the 13th byte of the frame (the offset value 0 indicates the first byte of the frame).
31:24	FL3OFF	R/W	Filter 3 Offset This register defines the offset (within the frame range) of the frame to be detected by the filter x. This 8-bit mode offset is the offset of the first byte of the filter x to be detected. The minimum allowable value is 12, which indicates the 13th byte of the frame (the offset value 0 indicates the first byte of the frame).

Wake-up frame filter register 6 (MAC_WKUPFFL6)

Field	Name	R/W	Description
15:0	FL0CRC16	R/W	Filter 0 CRC-16 This register contains the CRC_16 value calculated according to the mode, and the byte mask programmed for wake-up filter register module.
31:16	FL1CRC16	R/W	Filter 1 CRC-16 This register contains the CRC_16 value calculated according to the mode, and the byte mask programmed for wake-up filter register module.

Wake-up frame filter register 7 (MAC_WKUPFFL7)

Field	Name	R/W	Description
15:0	FL2CRC16	R/W	Filter 2 CRC-16 This register contains the CRC_16 value calculated according to the mode, and the byte mask programmed for wake-up filter register module.
31:16	FL3CRC16	R/W	Filter 3 CRC-16 This register contains the CRC_16 value calculated according to the mode, and the byte mask programmed for wake-up filter register module.

24.5.10 PMT control and state register (MAC_PMTCTRLSTS)

Offset address: 0x2C

Reset value: 0x0000 0000

This register will configure the wake-up time request and monitor the wake-up event.

Field	Name	R/W	Description
0	PD	R/S	Power Down When this bit is set to 1, all received frames will be discarded. When receiving the magic packet or wake-up frame, this bit will be automatically cleared to zero and the power-down mode will be disabled. After this bit is cleared to zero, the received frame will be forwarded to the application program. This bit can be set to 1 only when the magic packet is enabled or the wake-up frame bit is set to 1.
1	MPEN	R/W	Magic Packet Enable When this bit is set to 1, this bit will enable the power management event generated due to receiving of a magic packet.
2	WKUPFEN	R/W	Wakeup Frame Enable When this bit is set to 1, this bit will enable the power management event generated due to receiving of a wake-up frame.
4:3	Reserved		
5	MPRX	RC_R	Magic Packet Received When this bit is set to 1, it indicates that the power management event is generated due to receiving of a magic packet. This bit can be cleared to zero by reading the register.
6	WKUPFRX	RC_R	Wakeup Frame Received When this bit is set to 1, it indicates that the power management event is generated due to receiving of a wake-up frame. This bit can be cleared to zero by reading the register.
8:7	Reserved		
9	GUN	R/W	Global Unicast When this bit is set to 1, it will enable any filtered unicast packet confirmed by MAC address to a wake-up frame.
30:10	Reserved		
31	WKUPFRST	R/S	Wakeup Frame Filter Register Pointer Reset When this bit is set to 1, it will reset the remote wake-up frame filter register pointer to 000b. It will be automatically cleared to zero after 1 clock cycle.

24.5.11 Interrupt state register (MAC_ISTS)

Offset address: 0x38

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	Reserved		

Field	Name	R/W	Description
3	PMTIS	R	PMT Interrupt Status This bit is set when a magic packet or remote wake-up frame is received in power-off mode. When bit [6:5] is cleared due to read operation of PMT control and state register, this bit will be cleared.
4	MMCIS	R	MMC Interrupt Status When any bit [6:5] is set to high, this bit will be set to high and it can be cleared only when all these bits are low.
5	MMCRXIS	R	MMC Receive Interrupt Status When an interrupt is generated in the MMC receive interrupt register, this bit will be set to high. When all bits in the interrupt register are cleared, this bit will also be cleared.
6	MMCTXIS	R	MMC Transmit Interrupt Status When an interrupt is generated in the MMC transmit interrupt register, this bit will be set to high. When all bits in the interrupt register are cleared, this bit will also be cleared.
8:7	Reserved		
9	TSIS	R	Timestamp Interrupt Status When the system time value is equal to or exceeds the value specified in the target time register, this bit will be set to 1. It will be cleared to zero when reading this register.
15:10	Reserved		

24.5.12 Interrupt mask register (MAC_IMASK)

Offset address: 0x3C

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	Reserved		
3	PMTIM	R/W	PMT Interrupt Mask When this bit is set, the PMT interrupt status bit is set in the register "interrupt state register", so this bit disables generation of interrupt signal.
8:4	Reserved		
9	TSTIM	R/W	Time Stamp Trigger Interrupt Mask If this bit is set to 1, generation of timestamp interrupts will be disabled.
15:10	Reserved		

24.5.13 MAC address 0 high register (MAC_ADDR0H)

Offset address: 0x40

Reset value: 0x0010 FFFF

Field	Name	R/W	Description
15:0	ADDR0H	R/W	MAC address 0 high bit [47:32] It contains the first 16 bits (47:32) of the first 6 bytes of MAC address 0. The MAC uses this field to filter the received frames and inserts the MAC address in the transmission flow control (pause) frame.

Field	Name	R/W	Description
30:16	Reserved		
31	AL1	R	Always 1

24.5.14 MAC address 0 low register (MAC_ADDR0L)

Offset address: 0x44

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	ADDR0L	R/W	MAC Address 0 low bit [31:0] (MAC Address 1) This bit field contains the low 32 bits of the first 6-byte MAC address 0. This is the frame used by MAC to filter the received frames and insert the MAC address in the transmission flow control (pause) frame.

24.5.15 MAC address 1 high register (MAC_ADDR1H)

Offset address: 0x48

Reset value: 0x0000 FFFF

Field	Name	R/W	Description
15:0	ADDR1H	R/W	MAC address 1 high bit [47:32] It contains the first 16 bits (47:32) of the first 6-byte MAC address 1. The MAC uses this field to filter the received frames and inserts the MAC address in the transmission flow control (pause) frame.
23:16	Reserved		
29:24	MASKBCTRL	R/W	Mask Byte Control These bits are used to compare the mask control bits of 1 byte of each MAC address. When they are set to high level, the MAC core will not compare the corresponding bytes of the received DA/SA with the contents of the MAC address 1 register. Each bit is used to control the mask of bytes, as follows: Bit 29: ADDR1H [15:8] Bit 28: ADDR1H [7:0] Bit 27: ADDR1L [31:24] … Bit 24: ADDR1L [7:0]
30	ADDRSEL	R/W	Address Select 0: Compare the MAC address 1 [47:0] with the DA field of the received frame 1: Compare the MAC address 1 [47:0] with the SA field of the received frame
31	ADDREN	R/W	Address Enable 0: The address filter will ignore the address used for filtering 1: The address filter uses the MAC address 1 for filtering

24.5.16 MAC address 1 low register (MAC_ADDR1L)

Offset address: 0x4C

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	ADDR1L	R/W	MAC Address 1 low bit [31:0] (MAC Address1) This bit field contains the low 32 bits of the first 6-byte MAC address 1. If the application does not load the content of this bit field after initialization, the content will not be defined.

24.5.17 MAC address 2 high register (MAC_ADDR2H)

Offset address: 0x50

Reset value: 0x0000 FFFF

Field	Name	R/W	Description
15:0	ADDR2H	R/W	MAC address 2 high bit [47:32] (MAC Address 2) It contains the first 16 bits (47:32) of the first 6 bytes of MAC address 2.
23:16	Reserved		
29:24	MASKBCTRL	R/W	Mask Byte Control These bits are used to compare the mask control bits of 2 bytes of each MAC address. When they are set to high level, the MAC core will not compare the corresponding bytes of the received DA/SA with the contents of the MAC address 2 register. Each bit is used to control the mask of bytes, as follows: Bit 29: ADDR2H [15:8] Bit 28: ADDR2H [7:0] Bit 27: ADDR2L [31:24] … Bit 24: ADDR2L [7:0]
30	ADDRSEL	R/W	Address Select 0: Compare the MAC address 2 [47:0] with the DA field of the received frame 1: Compare the MAC address 2 [47:0] with the SA field of the received frame
31	ADDREN	R/W	Address Enable 0: The address filter will ignore the address used for filtering 1: The address filter uses the MAC address 2 for filtering

24.5.18 MAC address 2 low register (MAC_ADDR2L)

Offset address: 0x54

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	ADDR2L	R/W	MAC Address 2 low bit [31:0] (MAC Address 2) This bit field contains the low 32 bits of the first 6-byte MAC address 2. If the application does not load the content of this bit field after initialization, the content will not be defined.

24.5.19 MAC address 3 high register (MAC_ADDR3H)

Offset address: 0x58

Reset value: 0x0000 FFFF

Field	Name	R/W	Description
15:0	ADDR3H	R/W	MAC address 3 high bit [47:32] (MAC Address 3) It contains the first 16 bits (47:32) of the first 6-byte MAC address 3.
23:16	Reserved		
29:24	MASKBCTRL	R/W	Mask Byte Control These bits are used to compare the mask control bits of 3 bytes of each MAC address. When they are set to high level, the MAC core will not compare the corresponding bytes of the received DA/SA with the contents of the MAC address 3 register. Each bit is used to control the mask of bytes, as follows: Bit 29: ADDR3H [15:8] Bit 28: ADDR3H [7:0] Bit 27: ADDR3L [31:24] … Bit 24: ADDR3L [7:0]
30	ADDRSEL	R/W	Address Select 0: Compare the MAC address 3 [47:0] with the DA field of the received frame 1: Compare the MAC address 3 [47:0] with the SA field of the received frame
31	ADDREN	R/W	Address Enable 0: The address filter will ignore the address used for filtering 1: The address filter uses the MAC address 3 for filtering

24.5.20 MAC address 3 low register (MAC_ADDR3L)

Offset address: 0x5C

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	ADDR3L	R/W	MAC Address 3 low bit [31:0] (MAC Address 3) This bit field contains the low 32 bits of the first 6-byte MAC address 3. If the application does not load the content of this bit field after initialization, the content will not be defined.

24.6 MMC register address mapping

Table 84 MMC Register Address Mapping

Register name	Description	Offset address
MMC_CTRL	Control register	0x100
MMC_RXINT	Receive interrupt register	0x104
MMC_TXINT	Transmit interrupt register	0x108
MMC_RXINTMASK	Mask receive interrupt register	0x10C
MMC_TXINTMASK	Mask transmit interrupt register	0x110
MMC_TXGFSCCNT	Transmitted good frames single collision counter register	0x14C

Register name	Description	Offset address
MMC_TXGFMCCNT	Transmitted good frames more collision counter register	0x150
MMC_TXGFCNT	Transmitted good frames counter register	0x168
MMC_RXFCECNT	Received Frames CRC Error Counter register	0x194
MMC_RXFAECNT	Received frame alignment error counter register	0x198
MMC_RXGUNCNT	Received good unicast frame counter register	0x1C4

24.7 MMC register functional description

24.7.1 Control register (MMC_CTRL)

Offset address: 0x100

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CNTRST	R/W	Counter Reset When this bit is set, all counters will be reset. This bit will be automatically cleared to zero after 1 clock cycle
1	CNTSTOPRO	R/W	Counter Stop Rollover When this bit is set, the counter will not return to zero when it reaches its maximum value.
2	RSTOR	R/W	Reset on read When this bit is set, after reading the MMC counter, this counter will be reset. The counter will be cleared to zero after reading the least significant byte channel.
3	MCNTF	R/W	MMC Counter Freeze When this bit is set, all MMC counters will be frozen so that they remain at the current value. (Only after this bit is cleared to zero, will the MMC counter be updated due to the existence of transmitted or received frames)
31:4	Reserved		

24.7.2 Receive interrupt register (MMC_RXINT)

Offset address: 0x104

Reset value: 0x0000 0000

Field	Name	R/W	Description
4:0	Reserved		
5	RXFCE	RC_R	Received Frames CRC Error This bit will be set when the received frame counter has a CRC error and reaches half of its maximum value.
6	RXFAE	RC_R	Received Frames Alignment Error This bit will be set when the received frame counter has an alignment error and reaches half of its maximum value.

Field	Name	R/W	Description
16:7	Reserved		
17	RXGUNF	RC_R	Received Good Unicast Frames This bit will be set when the received good unicast frame counter reaches half of its maximum value.
31:18	Reserved		

24.7.3 Transmit interrupt register (MMC_TXINT)

Offset address: 0x108

Reset value: 0x0000 0000

Field	Name	R/W	Description
13:0	Reserved		
14	TXGFSCOL	RC_R	Transmitted Good Frames Single Collision This bit will be set when the good frame counter transmitted after a single collision reaches half of its maximum value.
15	TXGFMCOL	RC_R	Transmitted Good Frames More Single Collision This bit will be set when the good frame counter transmitted after multiple collisions reach half of its maximum value.
20:16	Reserved		
21	TXGF	RC_R	Transmitted Good Frames This bit will be set when the transmitted good frame counter reaches half of its maximum value.
31:22	Reserved		

24.7.4 Mask receive interrupt register (MMC_RXINTMASK)

Offset address: 0x10C

Reset value: 0x0000 0000

Field	Name	R/W	Description
4:0	Reserved		
5	RXFCEM	R/W	Received Frames CRC Error Mask When this bit is set, the interrupt will be masked when the received frame counter has a CRC error and reaches half of its maximum value.
6	RXFAEM	R/W	Received Frames Alignment Error Mask When this bit is set, the interrupt will be masked when the received frame counter has an alignment error and reaches half of its maximum value.
16:7	Reserved		
17	RXGUNFM	R/W	Received Good Unicast Frames Mask When this bit is set, the interrupt will be masked when the received good unicast frame counter reaches half of its maximum value.
31:18	Reserved		

24.7.5 Mask transmit interrupt register (MMC_TXINTMASK)

Offset address: 0x110

Reset value: 0x0000 0000

Field	Name	R/W	Description
13:0	Reserved		
14	TXGFSCOLM	R/W	Transmitted Good Frames Single Collision Mask When this bit is set, the interrupt will be masked when the good frame counter transmitted after single collision reaches half of its maximum value.
15	TXGFMCOLM	R/W	Transmitted Good Frames More Single Collision Mask When this bit is set, the interrupt will be masked when the good frame counter transmitted after multiple collisions reaches half of its maximum value.
20:16	Reserved		
21	TXGFM	R/W	Transmitted Good Frames Mask When this bit is set, the interrupt will be masked when the transmitted good frame counter reaches half of its maximum value.
31:22	Reserved		

24.7.6 Transmitted good frames single collision counter register (MMC_TXGFSCCNT)

Offset address: 0x14C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TXGFSCCNT	R	Transmitted Good Frames Single Collision Counter Transmitted good frames single collision counter.

24.7.7 Transmitted good frames more collision counter register (MMC_TXGFMCCNT)

Offset address: 0x150

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TXGFMCCNT	R	Transmitted Good Frames More Collision Counter Transmitted good frames more collision counter .

24.7.8 Transmitted good frames counter register (MMC_TXGFCNT)

Offset address: 0x168

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TXGFCNT	R	Transmitted Good Frames Counter Transmitted good frames counter.

24.7.9 Received Frames CRC Error Counter register (MMC_RXFCECNT)

Offset address: 0x194

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RXFCECNT	R	Received Frames CRC Error Counter Received Frames CRC Error Counter.

24.7.10 Received frame alignment error counter register (MMC_RXFAECNT)

Offset address: 0x198

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RXFAECNT	R	Received Frames Alignment Error Counter Received Frames Alignment Error Counter.

24.7.11 Received good unicast frame counter register (MMC_RXGUNCNT)

Offset address: 0x1C4

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RXGUNCNT	R	Received Good Unicast Frames Counter Received Good Unicast Frames Counter.

24.8 PTP register address mapping

Used to support the register of precision network clock synchronization which is in accordance with IEEE 1588 standard.

Table 85 PTP Register Address Mapping

Register name	Description	Offset address
PTP_TSCTRL	Timestamp control register	0x700
PTP_SUBSECI	Subsecond increment register	0x704
PTP_TSH	Timestamp high bit register	0x708
PTP_TSL	Timestamp low bit register	0x70C
PTP_TSHUD	Timestamp high bit update register	0x710
PTP_TSLUD	Timestamp low bit update register	0x714
PTP_TSA	Timestamp addend register	0x718
PTP_TTSH	Target timestamp high bit register	0x71C
PTP_TTSL	Target timestamp low bit register	0x720

24.9 PTP register functional description

24.9.1 Timestamp control register (PTP_TSCTRL)

Offset address: 0x700

Reset value: 0x0000 2000

Field	Name	R/W	Description
0	TSEN	R/W	Time Stamp Enable 0: Disable 1: Enable Since the maintained system time is suspended, after this bit is set to high level, it will be always necessary to initialize the timestamp function (system time).
1	TSUDSEL	R/W	Time Stamp Update Mode Select Select the method of updating the system timestamp 0: Rough update 1: Precision update
2	TSSTINIT	R/W	Time Stamp System Time Initialize When this bit is set, the system time will be initialized with the value specified in the timestamp high-bit update register and timestamp low-bit update register. Before this bit is set, it must be read as zero. After initialization, this bit will be cleared to zero.
3	TSSTUD	R/W	Time Stamp System Time Update When this bit is set, the system time will be updated with the value specified in the timestamp high-bit update register and timestamp low-bit update register. TSSTINIT and TSSTUD must be read as zero before this bit is set. After the update is completed, this bit will be cleared to zero.
4	TSTRGIEN	R/W	Time Stamp Trigger Interrupt Enable When this bit is set, if the value written in the target time register is less than the system time, a timestamp interrupt will be generated. This bit will be cleared to zero when a timestamp interrupt is triggered.
5	TSADDUD	R/W	Time Stamp Addend Register Update When this bit is set, the contents of the timestamp addend register will be updated to PTP for precision calibration. After the update is completed, this bit will be cleared to zero. Before this bit is set, it must be read as zero.
31:6	Reserved		

Table 86 Timestamp Snapshot Message

TSCLKNSEL	TSSMNSEL	TSSMESEL	Snapshot message
0X	Irrelevant	0	SYNC, Follow_Up, Delay_Req, Delay_Resp
	1	1	Delay_Req
	0	1	SYNC
10	×	0	SYNC，Follow_Up，Delay_Req，Delay_Resp
		1	SYNC，Follow_Up
11		0	SYNC，Follow_Up，Delay_Req，Delay_Resp，Pdelay_Req，Pdelay_Resp
		1	SYNC，Pdelay_Req，Pdelay_Resp

Note: ×=not applicable

24.9.2 Subsecond increment register (PTP_SUBSECI)

Offset address: 0x704

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	STSUBSECI	R/W	System Time Subseconds Increment It will be added to the system time subsecond value at the time of each update.
31:8	Reserved		

24.9.3 Timestamp high bit register (PTP_TSH)

Offset address: 0x708

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	STSEC	R	System Time Second Value System second time.

24.9.4 Timestamp low bit register (PTP_TSL)

Offset address: 0x70C

Reset value: 0x0000 0000

Field	Name	R/W	Description
30:0	STSUBSEC	R	System Time Subseconds Value System subsecond time, with precision of 0.46ns.
31	STSEL	R	System Time Select This bit indicates positive and negative values of the system time. 0: Positive 1: Negative Since the system time should always be positive, this bit is generally zero.

24.9.5 Timestamp high bit update register (PTP_TSHUD)

Offset address: 0x710

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TSUDSEC	R/W	Time Stamp Update Second Value The second time to be initialized or added to the system time.

24.9.6 Timestamp low bit update register (PTP_TSLUD)

Offset address: 0x714

Reset value: 0x0000 0000

Field	Name	R/W	Description
30:0	TSUDSUBSEC	R/W	Time Stamp Update Subseconds Value The subsecond time to be initialized or added to the system time. The precision is 0.46ns.
31	TSUDSEL	R/W	Time Stamp Update Select This bit indicates positive and negative values of the system time.

Field	Name	R/W	Description
			0: Positive 1: Negative When TSSTINIT bit is set, this bit is 0. When TSSTUD bit and this bit are set to 1 at the same time, the value of the timestamp update register shall be subtracted from the system time. Otherwise, it will be added to the system time.

24.9.7 Timestamp addend register (PTP_TSA)

Offset address: 0x718

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TSA	R/W	Time Stamp Addend Value The 32-bit time value to be added to the accumulator register, used for time synchronization.

24.9.8 Target timestamp high bit register (PTP_TTSH)

Offset address: 0x71C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TTSH	R/W	Target Time Stamp High Value Storage second time. When the value of the timestamp matches or exceeds two target timestamp registers at the same time, the MAC will generate an interrupt.

24.9.9 Target timestamp low bit register (PTP_TTSL)

Offset address: 0x720

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TTSL	R/W	Target Time Stamp Low Value Storage nanosecond time. When the value of the timestamp matches or exceeds two target timestamp registers at the same time, the MAC will generate an interrupt.

24.10 DMA register address mapping

Table 87 DMA Register Address Mapping

Register name	Description	Offset address
ETH_DMABMOD	DMA mode register	0x1000
ETH_DMATXPD	Transmit poll demand register	0x1004
ETH_DMARXPD	Receive poll demand register	0x1008
ETH_DMARXDLADDR	Receive descriptor list address register	0x100C
ETH_DMATXDLADDR	Transmit descriptor list address register	0x1010
ETH_DMASTS	State register	0x1014

Register name	Description	Offset address
ETH_DMAOPMOD	Operation mode register	0x1018
ETH_DMAINTEN	Interrupt enable register	0x101C
ETH_DMAMFABOCNT	Missed frame and buffer overflow counter register	0x1020
ETH_DMAHTXD	Current host transmit descriptor register	0x1048
ETH_DMAHRXD	Current host receive descriptor register	0x104C
ETH_DMAHTXBADDR	Current host transmit buffer address register	0x1050
ETH_DMAHRXBADDR	Current host receive buffer address register	0x1054

24.11 DMA register functional description

24.11.1 DMA bus mode register (ETH_DMABMOD)

Offset address: 0x1000

Reset value: 0x0000 2101

Field	Name	R/W	Description
0	SWR	R/W	Software Reset When this bit is set, the MAC DMA controller will reset the MAC logic and all internal registers. It will be cleared automatically after all clock domains are reset. You should read a 0 value in this bit before reprogramming any registers.
1	DAS	R/W	DMA Arbitration Scheme It specifies the arbitration scheme between the transmitting and receiving paths of channel 0. 0: Weighted round robin scheduling of Rx:Tx is used, given in [15:14] 1: The priority of Rx is higher than that of Tx
6:2	DSL	R/W	Descriptor Skip Length This bit specifies the number of Word, Dword, or Lword skipped between two unlinked descriptors Address skip starts from the end of the current descriptor to the beginning of the next descriptor. When the DSL value is equal to 0, DMA will regard the descriptor table as continuous in ring mode.
7	Reserved		
13:8	PBL	R/W	Programmable Burst Length These bits indicate the maximum number of beats to be transmitted in a DMA transaction. This is the maximum value used in a single block read and write. Each time the burst transmission is started on the host bus, DMA will always attempt to follow the burst specified in PBL. PBL can be programmed with allowable value 1, 2, 4, 8, 16 and 32. Any other value may result in undefined behaviors. When USP is set to high level, the PBL value is only applicable to Tx DMA transactions. The PBL value has the following limitations: the maximum number of possible beats is limited by the size of Tx FIFO and Rx FIFO of MTL layer and the width of data bus on DMA. FIFO has a limitation, namely, the maximum beat supported is half the FIFO depth unless specified.
15:14	PR	R/W	Priority Ratio

Field	Name	R/W	Description
			These bits control the priority ratio of weighted round robin arbitration between Rx direct memory access and Tx direct memory access. These bits are valid only when bit [1] is reset. 00: Priority ratio is 1:1 01: Priority ratio is 2:1 10: Priority ratio is 3:1 11: Priority ratio is 4:1
16	FB	R/W	Fixed Burst This bit controls whether the AHB main interface performs fixed burst transmission. After it is set, at the beginning of normal burst transmission, the AHB interface only uses SINGLE, INCR4, INCR8 or INCR16. When it is reset, the AHB interface uses single and INCR burst transmission operations.
22:17	RPBL	R/W	Receive DMA programmable burst length (Rx DMA PBL) This bit field indicates the maximum number of beats to transmitted in a Rx DMA transaction. This is the maximum value used in a single block read and write. Each time the burst transmission is started on the host bus, Rx DMA will always attempt to follow the burst specified in RPBL. RPBL can be programmed with allowable value 1, 2, 4, 8, 16 and 32. Any other value may result in undefined behaviors. This field is valid only when USP is set to high level.
23	USP	R/W	Use Separate PBL When set to high level, this bit configures Rx DMA using the value configured in bit [22:17] as PBL. The PBL value in bit [13:8] is applicable only to Tx DMA operations. When reset to low level, the PBL value in bit [13:8] is applicable to two kinds of DMA engines.
24	PBLx4	R/W	PBLx4 Mode When set to high level, this bit will multiply the programmed PBL value by four times. Therefore, the DMA will transmit data at a maximum beam number of 4, 8, 16, 32, 64 and 128 according to the PBL value.
25	AAL	R/W	Address-Aligned Beats When this bit is set to high level and the FB bit is equal to 1, the AHB interface will generate all bursts aligned with the LS bit of the start address. If the FB bit is equal to 0, the first burst (the start address of the access data buffer) is misaligned, but the subsequent bursts are aligned to this address.
31:26	Reserved		

24.11.2 Transmit poll demand register (ETH_DMATXPD)

Offset address: 0x1004

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TXPD	R/W	Transmit Poll Demand When these bits are written with any value, DMA will read the current descriptor pointed to by the ETH_DMAHTXD register. If the descriptor is not available, the pending state will be transmitted and returned and the bit [2] of the ETH_DMASTS register will be set. If the descriptor is available, continue to transmit.

24.11.3 Receive poll demand register (ETH_DMARXPD)

Offset address: 0x1008

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RXPD	R/W	Receive Poll Demand When these bits are written with any value, DMA will read the current descriptor pointed to by the ETH_DMAHRXD register. If the descriptor is not available (owned by the host), the pending state will be transmitted and returned and the bit [7] of the ETH_DMASTS register will be set. If the descriptor is available, Rx DMA will return to active state.

24.11.4 Receive descriptor list address register (ETH_DMARXDLADDR)

Offset address: 0x100C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RXSTA	R/W	Start of Receive List This field contains the base address of the first descriptor in the receive descriptor list. LSB bits [1:0, 2:0, or 3:0] of 32-bit, 64-bit, or 128-bit bus width is ignored and is regarded as all zero by DMA. Therefore, these LSB bits are read-only.

24.11.5 Transmit descriptor list address register (ETH_DMATXDLADDR)

Offset address: 0x1010

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	TXSTA	R/W	Start of Transmit List This field contains the base address of the first descriptor in the receive descriptor list. LSB bits [1:0, 2:0, or 3:0] of 32-bit, 64-bit, or 128-bit bus width is ignored and is regarded as all zero by DMA. Therefore, these LSB bits are read-only.

24.11.6 State register (ETH_DMASTS)

Offset address: 0x1014

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TXFLG	RC_W1	Transmit Flag Frame transmission has been completed and TXDES1[31] bit in the first descriptor is set to 1.
1	TXSFLG	RC_W1	Transmit Stopped Flag

Field	Name	R/W	Description
			This bit is set when the transmission stops.
2	TXBU	RC_W1	Transmit Buffer Unavailable This bit indicates that the host owns the next descriptor in the transmit list and DMA cannot get it. Transmission pauses. Bit [22:20] explains the state conversion of the transmission process. To resume processing of the transmit descriptor, the host should change the ownership of the descriptor by setting TXDES0 [31], and then issue a transmit poll demand command.
3	TXJTO	RC_W1	Transmit Jabber Timeout This bit indicates that the transmit Jabber timer times out, and the transmission process will be terminated and in the stop state. This will cause Jabber timeout and the TXDES0 [14] flag bit to be set.
4	RXOVF	RC_W1	Receive Overflow This bit indicates that the receive buffer overflows during frame receiving. If part of the frame is transmitted to the application program, the overflow state will be set in RXDES0 [11].
5	TXUNF	RC_W1	Transmit Underflow This bit indicates that the transmit buffer underflows during frame transmission. Transmission is suspended and the underflow error TXDES0 [1] is set.
6	RXFLG	RC_W1	Receive Flag Frame receiving is completed, and the specific frame state information is updated in the descriptor. Receive and keep running.
7	RXBU	RC_W1	Receive Buffer Unavailable This bit indicates that the host owns the next descriptor in the receive list and DMA cannot get it. The receiving process is suspended. To resume processing of the receive descriptor, the host should change the ownership of the descriptor and issue a receive poll demand command. If no receive poll demand is issued, the receiving process will be resumed when the next confirmed incoming frame is received. This bit is set only when the current receive descriptor is owned by DMA.
8	RXSFLG	RC_W1	Receive Stopped Flag This bit will be set to 1 when the receiving process enters the stop state.
9	RXWTOFLG	RC_W1	Receive Watchdog Timeout Flag This bit is will be set to 1 when the length of the received frame is greater than 2048 bytes.
10	ETXFLG	RC_W1	Early Transmit Flag The frame to be transmitted has been completely transmitted to the transmit FIFO.
12:11	Reserved		
13	FBERRFLG	RC_W1	Fatal Bus Error Flag This bit indicates that a bus error has occurred, as described in bit [25:23]. When this bit is set, the corresponding DMA engine will disable all its bus access.
14	ERXFLG	RC_W1	Early Receive Flag

Field	Name	R/W	Description
			This bit indicates that DMA fills the first data buffer of the packet. When the software writes 1 to this bit or bit [6] of this register is set, this bit will be cleared.
15	AINTS	RC_W1	Abnormal Interrupt Summary When the corresponding interrupt bit is enabled in ETH_DMAINTEN register, the value of abnormal interrupt summary bit is the logic or operation result of the following bits: ETH_DMASTS[1]: Stop in transmission proces ETH_DMASTS[3]: Transmit Jabber timeout ETH_DMASTS[4]: Receive overflow ETH_DMASTS[5]: Transmit underflow ETH_DMASTS[7]: Receive buffer is unavailable ETH_DMASTS[8]: Stop in receiving proces ETH_DMASTS[9]: Receive watchdog timeout ETH_DMASTS[10]: Early transmit interrupt ETH_DMASTS[13]: Fatal bus error Only the unmasked bit affects the abnormal interrupt summary bit. This is a sticky bit and it must be cleared each time the corresponding bit that causes this bit to be set is cleared.
16	NINTS	RC_W1	Normal Interrupt Summary When the corresponding interrupt bit is enabled in ETH_DMAINTEN register, the value of normal interrupt summary bit is the logic or operation result of the following bits: ETH_DMASTS[0]: Transmit interrupt ETH_DMASTS[2]: Transmit buffer is unavailable ETH_DMASTS[6]: Receive interrupt ETH_DMASTS[14]: Early receive interrupt Only the unmasked bit affects the normal interrupt summary bit. This is a sticky bit and it must be cleared each time the corresponding bit that causes this bit to be set is cleared.
19:17	RXSTS	R	Receive Process State This field indicates the receive DMA FSM state. This field does not generate any interrupt. 000: Stop: Issue the reset or stop receiving command 001: Run: get the receive and transmit descriptors 010: Reserved 011: Run: wait for receiving message 100: Pending: the receive descriptor is unavailable 101: Run: disable the receive descriptor 110: Reserved 111: Run: in the progress of transmitting the received packet data from receive buffer to host memory
22:20	TXSTS	R	Transmit Process State This field indicates the transmit DMA FSM state. This field does not generate any interrupt. 000: Stop: issue the reset or stop transmission command 001: Run: get the transmit descriptor 010: Run: waiting state

Field	Name	R/W	Description
			011: Run: read data from host memory buffer and queue the transmit buffer (Tx FIFO) 100, 101: Reserved 110: Suspended: the transmit descriptor is unavailable or the transmit buffer underflows 111: Run: disable the transmit descriptor
25:23	ERRB	R	Error Bits This field indicates the type of error that causes the bus error, such as the error response of the AHB interface. This field is valid only when the bit [13] is set. This field does not generate any interrupt. 000: An error occurs in transmission process of Rx DMA write data 011: An error occurs in transmission process of Tx DMA read data 100: An error occurs in Rx DMA descriptor write access 101: An error occurs in Tx DMA descriptor write access 110: An error occurs in Rx DMA descriptor read access 111: An error occurs in Tx DMA descriptor read access
26	Reserved		
27	MMCFLG	R	MMC Flag This bit reflects an interrupt event in the MMC module of MAC. The software must read the corresponding register in the MAC to obtain the exact cause of the interrupt, and clear the interrupt source to clear this bit to 0. When this bit is high, an interrupt will be generated after it is enabled.
28	PMTFLG	R	PMT Flag This bit indicates an interrupt event in the PMT module of MAC. The software must read the PMT control and state register in the MAC to obtain the exact cause of the interrupt and clear its source to clear this bit to 0. When this bit is high, an interrupt will be generated after it is enabled.
29	TSTFLG	R	Timestamp Trigger Flag This bit indicates an interrupt event in the timestamp generator block of the MAC. The software must read the corresponding register in the MAC to obtain the exact cause of the interrupt, and clear its source to clear the bit to 0. When this bit is high, an interrupt will be generated after it is enabled.
31:30	Reserved		

24.11.7 Operation mode register (ETH_DMAOPMOD)

Offset address: 0x1018

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	Reserved		
1	STRX	R/W	Start or Stop Receive When this bit is set, the receiving process will be in running state. DMA attempts to obtain the descriptor from the receive list and process the incoming frames. Try to obtain the descriptor from the current location

Field	Name	R/W	Description
			in the list, and this location is the address set by the ETH_DMARXDLADDR register, or the location reserved when stopping before the receiving process. If DMA does not own this descriptor, receive will be suspended and ETH_DMASTS[7][will be set. The "Start receiving" command is valid only after receiving stops. If the command is issued before the ETH_DMARXDLADDR register is set, DMA behavior is unpredictable. When this bit is cleared, Rx DMA operation will stop after transmission of the current frame. The location of next descriptor in the receive list will be saved and become the current location after restarting the receiving process. The stop receiving command is valid only when the receiving process is in "running" or "suspended" state.
2	OSECF	R/W	Operate on Second Frame When this bit is set, it indicates that DMA is processing the second frame of transmitted data, even before obtaining the state of the first frame.
4:3	RXTHCTRL	R/W	Receive Threshold Control These two bits control the threshold level of the receive FIFO. When transmitting to the DMA starts, the frame size of receive FIFO is greater than the threshold. In addition, the complete frame with the length less than the threshold will be transmitted automatically. When the configured “receive FIFO size” is 128 bytes, 11 will not be used. These bits are valid only when the RXSF bit is 0 and will be ignored when the RXSF bit is 1 00：64 01：32 10：96 11：128
5	Reserved		
6	FUF	R/W	Forward Undersized Good Frames When it is set, Rx FIFO will forward small frames, including padding bytes and CRC. When it is reset, Rx FIFO will discard all frames less than 64 bytes unless a frame has been transmitted because the receiving threshold is low, such as RTC=01.
7	FERRF	R/W	Forward Error Frames When this bit is reset, Rx FIFO will discard the frames with error state. However, if the start byte pointer of the frame has been transferred to the read controller end (in threshold mode), the frame will not be discarded. If the start byte of the frame is not transmitted (output) on the ARI bus, Rx FIFO will discard the error frame.
12:8	Reserved		
13	STTX	R/W	Start or Stop Transmission Command When this bit is set, the transmission will be put in the running state, and DMA will check the transmit list of the current location to obtain the frame to be transmitted. The descriptor tries to obtain from the current location in the list or from the previous location reserved when the transmission stops. If the DMA does not own the current descriptor, the transmission will enter the suspended state and the ETH_DMASTS[2] will be set. This command will take effect only when the transmission

Field	Name	R/W	Description
			stops. If the command is issued before the ETH_DMATXDLADDR register is set, DMA behavior is unpredictable. When this bit is reset, the transmission process will stop after transmission of the current frame is completed. The location of next descriptor in the transmit list will be saved and when transmission is restarted, it will become the current location. The stop transmission command is valid only when transmission of the current frame is completed or the transmission is in the "suspended" state.
16:14	TXTHCTRL	R/W	Transmit Threshold Control These bits control the threshold level of the transmit FIFO. At the beginning of transmission, the frame size in the transmit FIFO is greater than the threshold. In addition, the complete frame with the length less than the threshold will also be transmitted. These bits are used only when the bit [21] is reset. 000：64 001：128 010：192 011：256 100：40 101：32 110：24 111：16
19:17	Reserved		
20	FTXF	R/W	Flush Transmit FIFO When this bit is set, the transmit FIFO controller logic will be reset to its default value, so all data in Tx FIFO will be lost or refreshed. This bit will be cleared internally when the refresh operation is completed. Before this bit is cleared, it should not be written into the operation mode register.
21	TXSF	R/W	Transmit Store and Forward When this bit is set, transmission will start if there is a complete frame in the transmit FIFO. When this bit is set, the TTC value specified in bit [16:14] will be ignored. This bit can be replaced only when transmission stops.
23:22	Reserved		
24	DISFRXF	R/W	Disable Flushing of Received Frames When this bit is set, Rx DMA will not refresh any frames because the receive descriptor or buffer is not available as it normally does when this bit is reset.
25	RXSF	R/W	Receive Store and Forward When this bit is set, the frame can be read after a complete frame is written to Rx FIFO, and the RTC bit will be ignored. When this bit is reset, Rx FIFO will run in pass-through mode, limited by the threshold specified by the RTC bit.
26	DISDT	R/W	Disable Dropping of TCP/IP Checksum Error Frames When this bit is set, the MAC will not discard the error frames detected only by the receive checksum offload engine. Such a frame has no error in the Ethernet frame received by the MAC, and only has errors in

Field	Name	R/W	Description
			the encapsulated load. When this bit is reset, if the FERRF bit is reset, all error frames will be discarded.
31:27	Reserved		

24.11.8 Interrupt enable register (ETH_DMAINTEN)

Offset address: 0x101C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TXIEN	R/W	Transmit Interrupt Enable When this bit is set to 1 through bit [16], the transmit interrupt will be enabled. When this bit is reset, the transmit interrupt will be disabled.
1	TXSEN	R/W	Transmit Stopped Enable When this bit is set to 1 through bit [15], the transmit stop interrupt will be enabled. When this bit is reset, the transmit stop interrupt will be disabled
2	TXBUEN	R/W	Transmit Buffer Unavailable Enable When this bit is set to 1 through bit [16], the transmit buffer unavailable interrupt will be enabled. When this bit is reset, the transmit buffer unavailable interrupt will be disabled.
3	TXJTOEN	R/W	Transmit Jabber Timeout Enable When this bit is set to 1 through bit [15], the transmit Jabber timeout interrupt will be enabled. When this bit is reset, the transmit Jabber timeout interrupt will be disabled.
4	RXOVFEN	R/W	Receive Overflow Interrupt Enable When this bit is set to 1 through bit [15], the receive overflow interrupt will be enabled. When this bit is reset, the overflow interrupt will be disabled.
5	TXUNFEN	R/W	Transmit Underflow Interrupt Enable When this bit is set to 1 through bit [15], the transmit underflow interrupt will be enabled. When this bit is reset, the underflow interrupt will be disabled.
6	RXIEN	R/W	Receive Interrupt Enable When this bit is set to 1 through bit [16], the receive interrupt will be enabled. When this bit is reset, the receive interrupt will be disabled.
7	RXBUEN	R/W	Receive Buffer Unavailable Enable When this bit is set to 1 through bit [15], the receive buffer unavailable interrupt will be enabled. When this bit is reset, the receive buffer unavailable interrupt will be disabled.
8	RXSEN	R/W	Receive Stopped Enable When this bit is set to 1 through bit [15], the receive stop interrupt will be enabled. When this bit is reset, the receive stop interrupt will be disabled.
9	RXWTOEN	R/W	Receive Watchdog Timeout Enable When this bit is set to 1 through bit [15], the receive watchdog timeout interrupt will be enabled. When this bit is reset, the receive watchdog timeout interrupt will be disabled.

Field	Name	R/W	Description
10	ETXIEN	R/W	Early Transmit Interrupt Enable When this bit is set to 1 through bit [15], the early transmit interrupt will be enabled. When this bit is reset, the early transmit interrupt will be disabled.
12:11	Reserved		
13	FBERREN	R/W	Fatal Bus Error Enable When this bit is set to 1 through bit [15], the fatal bus error interrupt will be enabled. When this bit is reset, the fatal bus error interrupt will be disabled.
14	ERXIEN	R/W	Early Receive Interrupt Enable When this bit is set to 1 through bit [16], the early receive interrupt will be enabled. When this bit is reset, the early receive interrupt will be disabled.
15	AINTSEN	R/W	Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary will be enabled. When this bit is reset, the abnormal interrupt summary will be disabled. This bit can enable the following interrupts: ETH_DMASTS[1]: Stop in transmission proces ETH_DMASTS[3]: Transmit Jabber timeout ETH_DMASTS[4]: Receive overflow ETH_DMASTS[5]: Transmit underflow ETH_DMASTS[7]: Receive buffer is unavailable ETH_DMASTS[8]: Stop in receiving proces ETH_DMASTS[9]: Receive watchdog timeout ETH_DMASTS[10]: Early transmit interrupt ETH_DMASTS[13]: Fatal bus error
16	NINTSEN	R/W	Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary will be enabled. When this bit is reset, the normal interrupt summary will be disabled. This bit can enable the following interrupts: ETH_DMASTS[0]: Transmit interrupt ETH_DMASTS[2]: Transmit buffer is unavailable ETH_DMASTS[6]: Receive interrupt ETH_DMASTS[14]: Early receive interrupt
31:17	Reserved		

24.11.9 Missed frame and buffer overflow counter register (ETH_DMAMFABOCNT)

Offset address: 0x1020

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	MISFCNT	RC_R	Controller Missed Frame Counter It indicates the number of frames lost by the controller because the host receive buffer is not available. This counter will increase each time the DMA discards an incoming frame.
16	MISFCNTOVF	RC_R	Overflow Bit for Missed Frame Counter

Field	Name	R/W	Description
27:17	AMISFCNT	RC_R	Application Missed Frame Counter It indicates the number of frames lost by application program.
28	OVFCNTOVF	RC_R	Overflow Bit for FIFO Overflow Counter
31:29	Reserved		

24.11.10 Current host transmit descriptor register (ETH_DMAHTXD)

Offset address: 0x1048

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	HTXDADDRP	R	Host Transmit Descriptor Address Pointer Pointer updaged by DMA during operation.

24.11.11 Current host receive descriptor register (ETH_DMAHRXD)

Offset address: 0x104C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	HRXDADDRP	R	Host Receive Descriptor Address Pointer Pointer updaged by DMA during operation.

24.11.12 Current host transmit buffer address register (ETH_DMAHTXBADDR)

Offset address: 0x1050

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	HTXBADDRP	R	Host Transmit Buffer Address Pointer Pointer updaged by DMA during operation.

24.11.13 Current host receive buffer address register (ETH_DMAHRXBADDR)

Offset address: 0x1054

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	HRXBADDRP	R	Host Receive Buffer Address Pointer Pointer updaged by DMA during operation.

25 Analog-to-digital Converter (ADC)

25.1 Full Name and Abbreviation Description of Terms

Table 88 Full Name and Abbreviation Description of ADC Terms

Full name in English	English abbreviation
Analog watchdog	AWD
Conversion	C
Injected	INJ
Regular	REG
Start	S
Scan	SCAN
Single	SINGLE
Automatic	A
Group	G
Discontinuous	DISC
Count	CNT
Dual	DUAL
Continuous	C
Calibration	CAL
Reset	RST
Alignment	ALIGN
External	EXT
Event	E
Trigger	TRG
Temperature	T
Sensor	S
Time	TIM
Sample	SMP
Offset	OF
High	H
Low	L
Threshold	T
Sequence	SEQ

Full name in English	English abbreviation
Length	LEN
Regular Channels	REG
Injected Channel	INJ
Injected Group	INJG
Automatic	A
Conversion	C
Analog Watchdog	AWD
Discontinuous Mode	DISC
Scan Mode	SCAN
Continuous Conversion	CONTC
Single Conversion	SINGLEC
External	EXT
External Trigger	EXTTRG
Sample Time	SMPTIM
Sequence	SEQ
Number	NUM

25.2 Introduction

Series products have two ADCs with 12-bit accuracy, and each ADC has up to 16 external channels and 2 internal channels. ADC1 and ADC2 have 16 external channels respectively, the A/D conversion mode of each channel has single, continuous, scan or discontinuous modes, and the ADC conversion results can be stored in 16-bit data register by left alignment or right alignment.

25.3 Main Characteristics

（1） ADC power supply requirements: From 2.4V to 3.6V; the general power supply voltage is 3.3V.

（2） ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$.

（3） 12-bit resolution

（4） ADC conversion time

- Formula: TCONV=sampling time+12.5 cycles
- The sampling time is controlled by SMPCYCCFGx[2:0] bit, and the minimum sampling cycle is 1.5; when ADCCLK=14MHz, the sampling time is 1.5 cycles: TCONV=1.5 cycles +12.5 cycles=14 cycles=1 μs.

（5） Mode input channel category

- External GPIO input channel
- One internal temperature sensor (V_{SENSE}) input channel
- One internal reference voltage (V_{REFINT}) input channel

（6） Channel conversion mode

- Single channel conversion mode: single conversion mode, continuous conversion mode
- Input channel classification: regular channel, injected channel
- One-group channel conversion mode: scan mode, discontinuous mode and injected channel management
- ADC mode: Independent ADC mode, and dual ADC mode

（7） Trigger mode

- On-chip timer signal trigger
- External pin signal trigger
- Software trigger

（8） Data register

- Regular data register
- Injected data register

（9） Interrupt

- End of conversion interrupt
- Analog watchdog interrupt

（10） DMA request supporting regular data conversion

（11） Data alignment

- Configurable data alignment of DALIGNCFG bit of data register ADC_CTRL2 is left or right alignment.

（12） Self-calibration

- Enable calibration by setting CAL bit of ADC_CTRL2 register. CAL bit is set to 1 during calibration and is cleared by hardware after calibration; calibration shall be performed every time before power-on.

25.4 Functional Description

25.4.1 ADC Pins

Table 89 ADC Pins

Name	Instruction	Signal type
V_{REF+}	High-end/Positive electrode reference voltage used by ADC, $2.4V \le V_{REF+} \le V_{DDA}$	Input, analog reference positive electrode
$V_{DDA}^{(1)}$	Equivalent to analog power supply of V_{DD} and: $2.4V \le V_{DDA} \le V_{DD}(3.6V)$	Input, analog power supply
V_{REF-}	Low-end/Negative electrode reference voltage used by ADC, $V_{REF-} = V_{SSA}$	Input, analog reference negative electrode
$V_{SSA}^{(1)}$	Equivalent to analog power supply of V_{ss}	Input, analog power ground
ADCx_IN[15:0]	16 analog input channels	Analog input signal

Note: 1. V_{DDA} and V_{SSA} should be connected to V_{DD} and V_{SS} respectively.

25.4.2 ADC Conversion Mode

The product has multiple built-in ADCs and channels (refer to the *Data Manual* for the specific number), which can be combined into a variety of conversion modes.

Multiple built-in ADCs; according to the number of ADCs, the conversion mode can be classified into independent ADC mode and dual ADC mode; multiple built-in channels, which can be classified into two groups, namely regular channel and injected channel. The internal conversion mode of each group can be divided into scan mode and discontinuous mode; for the internal channels of each group, the conversion mode is divided into single conversion mode and continuous conversion mode.

In the application, according to the actual application requirements, the number of ADC, the number of conversion channels and the conversion mode of each channel, the ADC conversion mode meeting the requirements can be designed.

25.4.2.1 Conversion mode of single ADC and single channel

Single ADC channel

Single ADC and single channel are not enabled by external trigger software. The conversion mode is single and continuous concurrent disabling of scan. The result of data conversion is right alignment. After the single ADC conversion is completed, the interrupt is triggered, and data is read in the interrupt service function, not using DMA transmission.

Single conversion mode

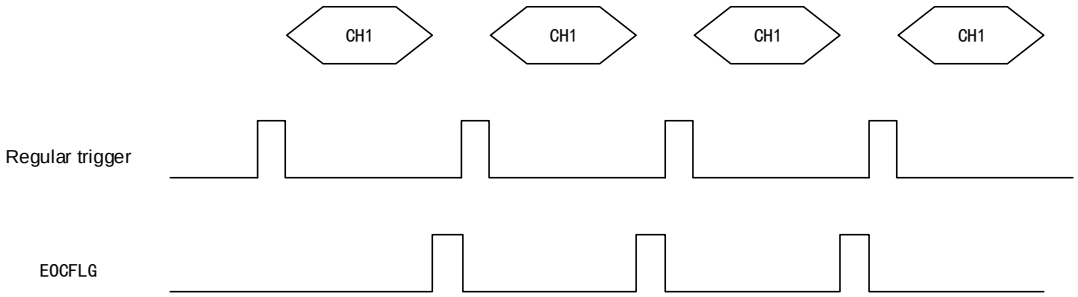
In this mode, for single channel, only one conversion is performed for this channel, and for multiple channels, only one conversion is performed for this group of channels.

This mode is started by the ADCEN bit of configuration register ADC_CTRL2 or is started by external trigger.

After one conversion of regular channel is over, the converted data will be stored in 16-bit ADC_REGDATA register, and EOCFLG bit will be set to 1. If configuration EOCIEN bit is set to 1, an interrupt will be generated.

After one conversion of injected channel is over, the converted data will be stored in 16-bit ADC_INJDATA1 register, and INJEOCFLG bit will be set to 1. If configuration INJEOCIEN bit is set to 1, an interrupt will be generated.

Figure 107 Single Conversion Mode Timing Diagram



Continuous conversion mode

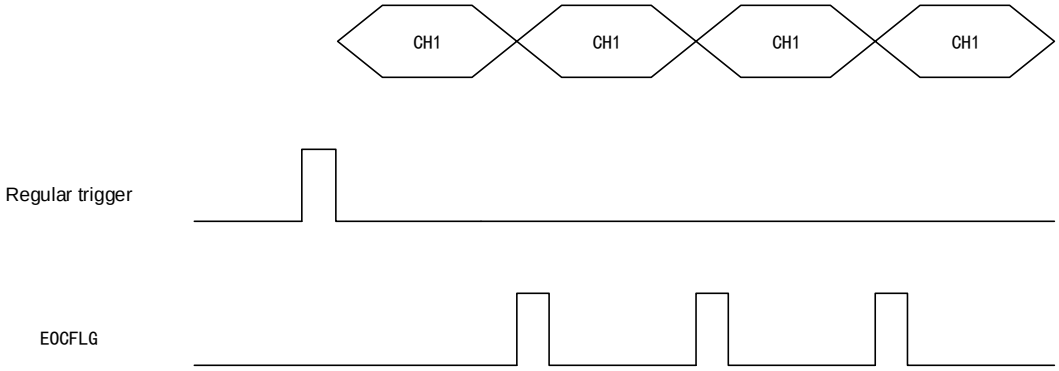
In this mode, for single channel, continuous conversion is conducted for this channel.

This mode is started by the ADCEN bit of configuration register ADC_CTRL2 or is started by external trigger.

After the conversion of one regular channel is over, the converted data will be stored in 16-bit ADC_REGDATA register, and EOCFLG bit will be set to 1. If configuration EOCIEN bit is set to 1, an interrupt will be generated.

After the conversion of one injected channel is over, the converted data will be stored in 16-bit ADC_INJDATA1 register, and INJEOCFLG bit will be set to 1. If configuration INJEOCIEN bit is set to 1, an interrupt will be generated.

Figure 108 Continuous Conversion Mode Timing Diagram



25.4.2.2 Conversion mode of single ADC and one group of channels

Single ADC and multiple channels

Turn on scan mode under single ADC multi-channel, do not use external trigger conversion, software trigger, data conversion result is right-aligned, ADC conversion result data is transferred to memory using DMA

Classification of analog input channels

Regular channel group

- The regular group consists of 16 channels
- Regular channel conversion sequence is determined by the register ADC_REGSEQx
- The total number of conversion channels of regular group is determined by REGSEQLEN[3:0] bit of configuration register ADC_REGSEQ1

Injected channel group

- The injected group consists of 4 channels
- Injected channel conversion sequence is determined by the register ADC_INJSEQ
- The total number of conversion channels of injected group is determined by INJSEQLEN[1:0 bit of configuration register ADC_INJSEQ

Internal input channel

Temperature sensor:

- The temperature sensor is used to measure the internal temperature of the chip
- The temperature sensor selects ADC1_IN16 input channel
- Start through TSVREFEN bit of the configuration register ADC_CTRL2

Internal reference voltage V_{REFINT}:

- The internal reference voltage is used to provide a stable voltage output for ADC
- Internal reference voltage V_{REFINT} is used to select ADC1_IN17 input channel

Channel conversion sequence

Configuration of regular sequence registers:

- Configure REGSEQC1[4:0]~REGSEQC6[4:0] bits of the register ADC_REGSEQ3 to set No. 1~6 conversion channels
- Configure REGSEQC7[4:0]~REGSEQC12[4:0] bits of the register ADC_REGSEQ2 to set No. 7~12 conversion channels
- Configure REGSEQC13[4:0]~REGSEQC16[4:0] bits of the register ADC_REGSEQ1 to set No. 13~16 conversion channels
- Configure REGSEQLEN[3:0] of the register ADC_REGSEQ1 to set the number of channels for conversion

Configuration of injected sequence register:

- Configure INJSEQC1[4:0]~INJSEQC4[4:0] bit of the register ADC_INJSEQ to set No. 1~4 conversion channels
- Configure INJSEQLEN[1:0] of the register ADC_INJSEQ to set the number of channels for conversion
- If the value of INJSEQLEN is less than 4, the conversion sequence will be different and start from (4-INJSEQLEN).

Channel conversion mode

Scan Mode

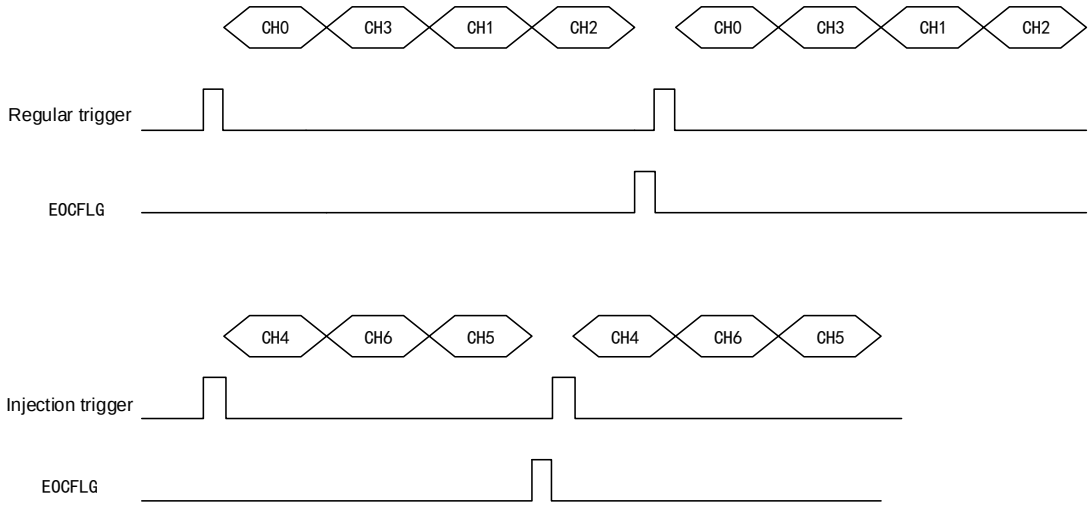
This mode is applicable to one group of channels, which is equivalent to a single conversion on each channel of one group of channels.

This mode is started by SCANEN bit of configuration register ADC_CTRL1, and after startup, ADC scans all channels which are arranged according to the sequence register ADC_REGSEQ or the ADC_INJSEQ, and after each channel conversion is completed, it will be automatically converted to the next channel of the group.

If the configuration CONTCEN bit is set to 1, the conversion will continue from the first channel of the group when the last channel of the group completes conversion.

If the configuration DMAEN bit is set to 1, the DMA controller will transmit the converted data of regular channel to SRAM every time the channel conversion is completed.

Figure 109 Scan Mode Timing Diagram



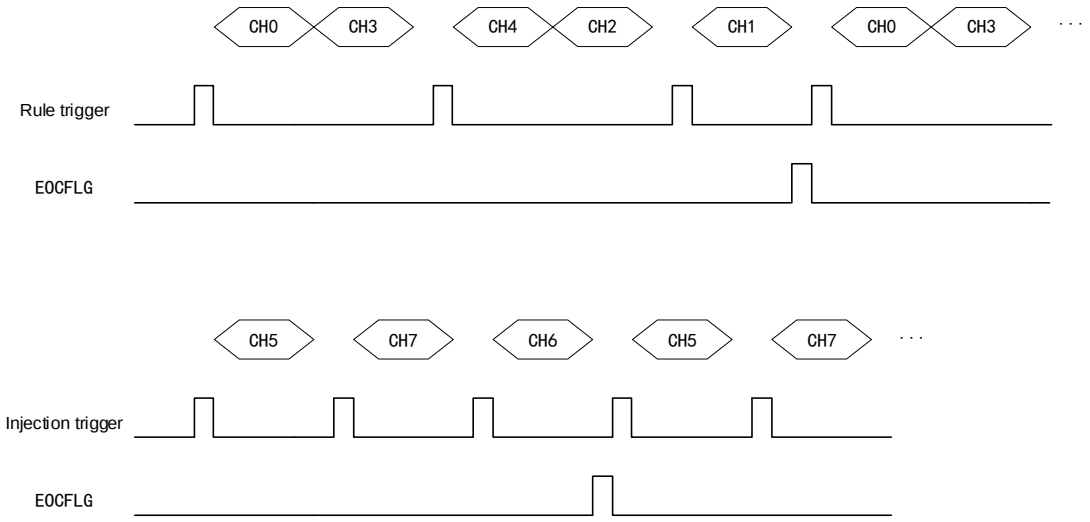
Discontinuous mode

This mode is suitable for a group of channels, which is equivalent to continuous conversion of multiple channels in a group of channels.

For regular groups, this mode is started by REGDISCEN bit of configuration register ADC_CTRL1; after startup, conduct short sequence conversion of n channels (n<=8), and n is determined by DISCNUMCFG[2:0] of configuration register ADC_CTRL1; next round of conversion of n channels can be started through software control or external trigger source and when the conversion of all channels of this group is completed, EOCFLG bit will be set to 1.

For injected groups, this mode is enabled by INJDISCEN bit of configuration register ADC_CTRL1; after startup, one channel will be converted according to the configuration sequence of the sequence register; conversion of next channels can be started by software control or external trigger source and when the conversion of all channels of this group is completed, EOCFLG bit and INJEOCFLG bit will be set to 1.

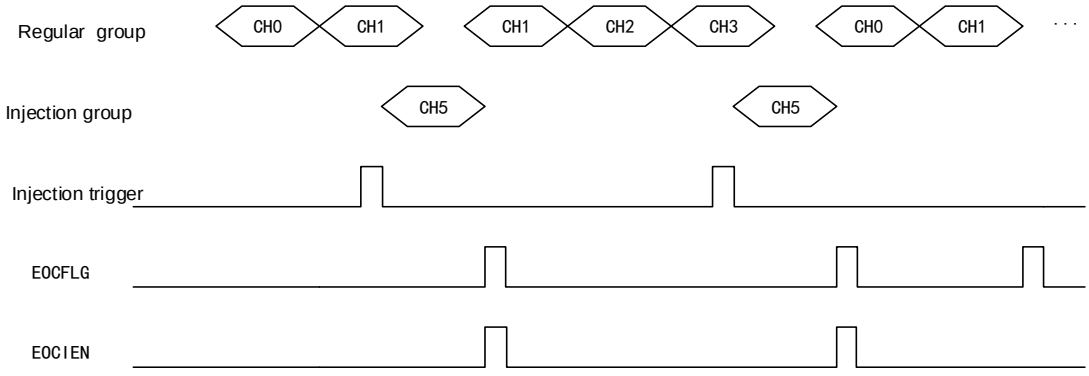
Figure 110 Discontinuous Mode Timing Diagram



Injected channel management

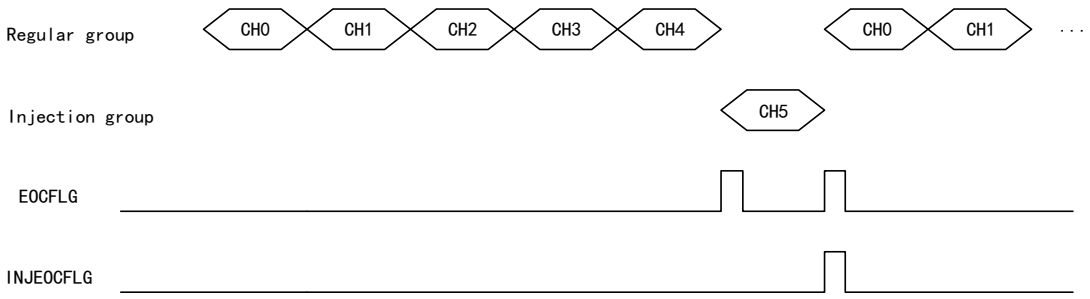
Trigger injection: Start by clearing INJGACEN bit of the register ADC_CTRL1 and configuring the SCANEN bit. If a software trigger or external trigger is generated during the conversion of regular group channels, the injected conversion will be triggered. At this time, the regular channel conversion will stop, the injected channel sequence will start conversion, and after the injected group channel conversion is completed, the regular group channel conversion will be recovered.

Figure 111Trigger Injection Timing Diagram



Automatic injection: Start by INJGACEN bit of configuration register ADC_CTRL1; after conversion of the regular group channels is completed, the injected group channels will start conversion automatically; in the automatic injection mode, external trigger of the injected group channels must be disabled; if the CONTCEN bit of the register ADC_CTRL2 is also configured, all channels of regular group and injection group will convert continuously.

Figure 112 Automatic Injection Timing Diagram



25.4.2.3 Conversion mode of dual-ADC and one group of channels

For products with two or more ADC modules, dual ADC mode is used. ADC1 is the master ADC by default, while others are the slave ADC by default, and dual ADC mode is set by configuring DUALMCFG[2:0] bit in ADC1_CTRL1 register.

When the configuration is triggered by external event, it is required to set it to trigger only the master ADC, and then configure the slave ADC to be triggered by software. (External trigger of master and slave must occur at the same time)

There are eight possible dual-ADC modes:

（1） Simultaneous regular mode

The simultaneous regular mode means ADC1 and ADC2 convert a regular channel group at the same time. Two ADCs cannot convert one channel at the same time.

The external trigger event is determined by REGEXTTRGSEL[2:0] of the register ADC1_CTRL2.

After ADC conversion, DMA transmission request will be generated, and converted data of ADC1 are stored in low 16 bits of the register ADC1_REGDATA, while ADC2 converted data are stored in high 16 bits of the register ADC1_REGDATA.

EOCFLG interrupt will be generated after all ADC regular channels are converted.

（2） Simultaneous injection mode

The simultaneous injection mode means ADC1 and ADC2 convert one injected channel group at the same time. Two ADCs cannot convert one channel at the same time.

The external trigger event is determined by INJGEXTTRGSEL[2:0] of the register ADC1_CTRL2.

After ADC conversion is over, the converted data will be stroed in the register ADC_INJDATAx.

INJEOCFLG interrupt will be generated after all ADC injected channels are converted.

（3） Fast cross mode

The fast cross mode means ADC1 and ADC2 collect a regular channel group alternately, with a short interval time.

The external trigger event is determined by REGEXTTRGSEL[2:0] of the register ADC_CTRL2; after the trigger is generated, ADC2 will be started, and ADC1 will be started after delay of seven ADC clock cycles.

The sampling time shall be less than seven ADC clock cycles.

（4） Slow cross mode

The slow cross mode means ADC1 and ADC2 collect a regular channel group alternately, with a long interval time.

The external trigger event is determined by REGEXTTRGSEL[2:0] of the register ADC_CTRL2; after the trigger is generated, ADC2 will be started, and ADC1 will be started after delay of 14 ADC clock cycles.

The sampling time shall be less than 14 ADC clock cycles.

（5） Alternate trigger mode

The alternate trigger mode means ADC1 and ADC2 collect the injected channel group by turns.

The external trigger event is determined by INJGEXTTRGSEL[2:0] of the register ADC1_CTRL2; after the trigger is generated, ADC1 will start conversion, and after all channels are converted, ADC2 will start conversion.

If discontinuous mode is enabled for ADC1 and ADC2, after triggered, ADC1 will start converting the first injected channel; after the second trigger is generated, ADC2 will start to convert the first injected channel and so on.

（6） Mixed simultaneous regular/injection mode

The mixed simultaneous regular/injection mode means after the simultaneous regular mode is interrupted, the simultaneous injection mode will be enabled.

In this mode, a sequence of the same length must be converted or a trigger interval time must be set to complete the conversion of a longer sequence.

（7） Mixed simultaneous regular + alternate trigger mode

The mixed simultaneous regular + alternate trigger mode means after the simultaneous regular mode is interrupted, the alternate trigger mode will be enabled.

In this mode, a sequence of the same length must be converted or a trigger

interval time must be set to complete the conversion of a longer sequence.

（8） **Mixed simultaneous injection + cross mode**

The mixed simultaneous injection + cross mode means after the cross mode is interrupted, the simultaneous injection mode will be enabled.

25.4.3 External Trigger

Register configuration of external trigger is as follows:

- The external event trigger of regular group channel is enabled by REGEXTTRGSEL[2:0] bit of configuration register ADC_CTRL2
- The external event trigger of injected group channel is started by INJGEXTTRGSEL[2:0] bit of configuration register ADC_CTRL2.

Table 90 External Trigger of Regular Channel of ADC1 and ADC2

Trigger source	REGEXTTRGSEL[2:0]	Trigger type
TMR1_CC1	000	Internal signal from on-chip timer
TMR1_CC2	001	
TMR1_CC3	010	
TMR2_CC2	011	
TMR3_TRGO	100	
TMR4_CC4	101	
EINT Line 11/TMR8_TRGO	110	External pin/internal signal from on-chip timer
REGSWSC	111	Software control bit

Table 109 External Trigger of Injected Channel of ADC1 and ADC2

Trigger source	INJGEXTTRGSEL[2:0]	Trigger type
TMR1_TRGO	000	Internal signal from on-chip timer
TMR1_CC4	001	
TMR2_TRGO	010	
TMR2_CC1	011	
TMR3_CC4	100	
TMR4_TRGO	101	
EINT Line 15/TMR8_CC4	110	External pin/internal signal from on-chip timer
INJSWSC	111	Software control bit

25.4.4 Data Register

25.4.4.1 Regular data register

ADC_REGDATA is a 32-bit ADC regular data register. In single-ADC mode, only

the lower 16 bits are used to store the converted data. In dual-ADC mode, the lower 16 bits are used to store the converted data of ADC1 while the higher 16 bits are used to store the converted data of ADC2. The data are left aligned or right aligned.

It is determined by DALIGNCFG bit of configuration register ADC_CTRL2 whether to use DMA transmission. There are at most 16 regular channels, but only one regular data register. Therefore, data coverage will occur in multi-channel conversion, and DMA transmission is needed at this time.

25.4.4.2 Injection data memory

ADC_INJDATAx (x=1,2,3,4) is ADC injected data register, and there are four 32-bit registers, of which the low 16 bits are effective and the high 16 bits are reserved. There are at most four injected channels and four injection data registers, so data coverage will not occur in multi-channel conversion. The data are left aligned or right aligned.

25.4.5 Interrupt

25.4.5.1 End of conversion interrupt

Interrupt of end of conversion of regular group channels

An interrupt will be generated by the end of conversion of regular channels; read the value of the regular data register in the interrupt function.

Determine by EOCFLG bit of configuration register ADC_STS.

Interrupt of end of conversion of injected group channels

An interrupt will be generated after the conversion of injected channels is completed; read the value of the regular data register in the interrupt function.

Determine by INJEOCFLG bit of configuration register ADC_STS.

25.4.5.2 Analog watchdog interrupt

If the input analog voltage is not within the threshold range, an analog watchdog interrupt will be generated.

Determine by configuring AWDFLG bit of the register ADC_STS.

25.4.6 DMA

DMA request will be generated after the conversion of regular channels is completed; the converted data result can be transmitted to the memory from the ADC_REGDATA register.

Only ADC1 can generate DMA request, and the conversion results of ADC2 are transmitted through the DMA function of ADC1.

25.5 Register Address Mapping

Table 91 ADC Register Address Mapping

Register name	Description	Offset address
ADC_STS	ADC state register	0x00
ADC_CTRL1	ADC control register 1	0x04
ADC_CTRL2	ADC control register 2	0x08
ADC_SMPTIM1	ADC sampling time register 1	0x0C
ADC_SMPTIM2	ADC sampling time register 2	0x10
ADC_INJDOFx	ADC injected channel data offset register x	0x14-0x20
ADC_AWDHT	Analog watchdog high-threshold register	0x24
ADC_AWDLT	Analog watchdog low-threshold register	0x28
ADC_REGSEQ1	ADC regular sequence register 1	0x2C
ADC_REGSEQ2	ADC regular sequence register 2	0x30
ADC_REGSEQ3	ADC regular sequence register 3	0x34
ADC_INJSEQ	ADC injected sequence register	0x38
ADC_INJDATAx	ADC injected data register X	0x3C–0x48
ADC_REGDATA	ADC regular data register	0x4C

25.6 Register Functional Description

25.6.1 ADC state register (ADC_STS)

Offset address: 0x00

Reset value: 0x0000 000

Field	Name	R/W	Description
0	AWDFLG	RC_W0	Analog Watchdog Occur Flag This bit is set to 1 by hardware and cleared by software, indicating whether an analog watchdog event occurs. 0: No occurrence 1: Occurred
1	EOCFLG	RC_W0	End of Conversion Flag 0: Not completed 1: Completed
2	INJEOCFLG	RC_W0	Injected Channel End of Conversion Flag 0: Not completed 1: Completed
3	INJCSFLG	RC_W0	Injected Channel Conversion Start Flag 0: Not start 1: Start

Field	Name	R/W	Description
4	REGCSFLG	RC_W0	Regular Channel Conversion Start Flag 0: Not start 1: Start
31:5	Reserved		

25.6.2 ADC control register 1 (ADC_CTRL1)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
4:0	AWDCHSEL	R/W	Analog Watchdog Channel Select 00000: ADC analog input channel 0 00001: ADC analog input channel 1 …… 01111: ADC analog input channel 15 10000: ADC analog input channel 16 10001: ADC analog input channel 17 Other value: Reserved For this register, pay attention to the followings: (1) The analog input channel 16 and channel 17 of ADC1 are connected to the temperature sensor and V_{REFINT} in the chip respectively (2) The analog input channel 16 and channel 17 of ADC2 are connected to V_{SS} in the chip
5	EOCIEN	R/W	EOC Interrupt Enable Used to enable the generation of interrupt after the conversion is completed. 0: Disable 1: Enable
6	AWDIEN	R/W	Analog Watchdog Interrupt Enable If the bit is set and in scan mode, when the watchdog detects that the value exceeds the threshold, an interrupt will be generated and the scan will be aborted. 0: Disable 1: Enable
7	INJEOCIEN	R/W	Interrupt Enable for Injected Channels End of Conversion Flag 0: Disable 1: Enable
8	SCANEN	R/W	Scan Mode Enable In the scan mode, convert the channel selected by ADC_REGSEQX or ADC_INJSEQX register. 0: Disable 1: Enable Note: If EOCINTEN or INJEOCINTEN bit is set respectively, EOC or INJEOC interrupt will be generated only after the last channel is converted.
9	AWDSGLEN	R/W	Enable The Watchdog On A Single Channel In Scan Mode This channel is specified by AWDCHSEL[4:0] bit.

Field	Name	R/W	Description
			0: Enable on all channels 1: Enable on a single channel;
10	INJGACEN	R/W	Automatic Injected Group Conversion Enable Used to enable automatic conversion of injected channels after the conversion of regular channel group is completed. 0: Disable 1: Enable
11	REGDISCEN	R/W	Discontinuous Mode On Regular Channels Enable 0: Disable 1: Enable
12	INJDISCEN	R/W	Discontinuous Mode On Injected Channels Enable 0: Disable 1: Enable
15:13	DISCNUMCFG	R/W	Discontinuous Mode Channel Number Configure 000: One channel 001: Two channels …… 111: Eight channels
19:16	DUALMCFG	R/W	Dual ADC Mode Configure 0000: Independent mode 0001: Mixed synchronous regular + injected synchronous mode 0010: Mixed simultaneous regular + alternate trigger mode 0011: Mixed simultaneous injection + fast cross mode 0100: Mixed simultaneous injection + slow cross mode 0101: Injected simultaneous mode 0110: Regular simultaneous mode 0111: Fast cross mode 1000: Slow cross mode 1001: Alternate trigger mode Others: Reserved In ADC2, these bits are reserved bits; in dual ADC mode, changing the channel configuration will result in a restart condition, which will result in loss of synchronization. It is recommended to turn off dual ADC mode (i.e. configure as independent mode) before making any configuration changes.
21:20	Reserved		
22	INJAWDEN	R/W	Enable the Analog Watchdog Function On the Injected Channels 0: Disable 1: Enable
23	REGAWDEN	R/W	Enable the Analog Watchdog Function On the Regular Channels 0: Disable 1: Enable
31:24	Reserved		

25.6.3 ADC control register 2 (ADC_CTRL2)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ADCEN	R/W	ADC Enable (1) If this bit is set to 0, write 1 to power on ADC and start ADC conversion (2) If this bit is set to 1, write 1 to start conversion 0: Disable ADC conversion and calibration and enter the power-down mode 1: Enable ADC and start conversion Note: To prevent triggering wrong conversion, if another bit and this bit in this register are changed, conversion will not be triggered.
1	CONTCEN	R/W	Continuous Conversion Mode Enable 0: Single conversion mode 1: Continuous conversion mode
2	CAL	R/W	A/D Calibration Calibration starts when this bit is set to 1 by software, and it is cleared by hardware when the calibration is completed. 0: Calibration is completed 1: Start calibration
3	CALRST	R/W	Calibration Reset This bit is set to 1 by software, and is cleared by hardware after the calibration register completes resetting. 0: It means resetting of calibration register is completed 1: Reset calibration register
7:4	Reserved		
8	DMAEN	R/W	DMA Mode Enable 0: Disable 1: Enable Note: Only ADC1 can generate DMA request.
10:9	Reserved		
11	DALIGNCFG	R/W	Data Alignment Mode Configure 0: Right alignment 1: Left alignment
14:12	INJGEXTTRGSEL	R/W	Select the External Trigger Event to Start the Injected Group Conversion Trigger configuration of ADC1 and ADC2 is as follows: 000: TRGO event of timer 1 001: CC4 event of timer 1 010: TRGO event of timer 2 011: CC1 event of timer 2 100: CC4 event of timer 3 101: TRGO event of timer 4 110: EINT Line 15 111：INJSWSC
15	INJEXTTRGEN	R/W	Enable the External Trigger Conversion Mode of the Injected Channels 0: Disable

Field	Name	R/W	Description
			1: Enable
16	Reserved		
19:17	REGEXTTRGSEL	R/W	Select the External Trigger Event to Start the Regular Group Conversion Trigger configuration of ADC1 and ADC2 is as follows: 000: CC1 event of timer 1 001: CC2 event of timer 1 010: CC3 event of timer 1 011: CC2 event of timer 2 100: TRGO event of timer 3 110: CC4 event of timer 4 110: EINT Line 11 111：REGSWSC
20	REGEXTTRGEN	R/W	Enable the External Trigger Conversion Mode of the Regular Channels 0: Disable 1: Enable
21	INJSWSC	R/W	Software Start Conversion Injected Channels If INJSWSC is selected as trigger event in INJEXESEL[2:0] bit, this bit wil be used to start conversion of a group of injected channel; this bit can be set to 1 and cleared by software, and be cleaered by hardware after the conversion is started. 0: Reset state 1: Start conversion of injected channels
22	REGSWSC	R/W	Software Start Conversion Regular Channels If REGSWSC is selected as trigger event in REGEXTSEL[2:0] bit, this bit will be used to start conversion of a group of regular channel; this bit can be set to 1 and cleared by software, and be cleared by hardware after the conversion is started. 0: Reset state 1: Start conversion of regular channels
23	TSVREFEN	R/W	Temperature Sensor and V_{REFINT} Channel Enable This bit is valid only in ADC1. This bit can be set to 1 and cleared by software; in the device with multiple ADCs, this bit only appears in ADC1. 0: Disable 1: Enable
31:24	Reserved		

25.6.4 ADC sampling time register 1 (ADC_SMPTIM1)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	SMPCYCCFG10	R/W	Channel 10 Sample Cycles Configure 000: 1.5 periods 001: 7.5 periods 010: 13.5 periods 011: 28.5 periods 100: 41.5 periods 101: 55.5 periods 110: 71.5 periods 111: 239.5 periods
5:3	SMPCYCCFG11	R/W	Channel 11 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
8:6	SMPCYCCFG12	R/W	Channel 12 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
11:9	SMPCYCCFG13	R/W	Channel 13 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
14:12	SMPCYCCFG14	R/W	Channel 14 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
17:15	SMPCYCCFG15	R/W	Channel 15 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
20:18	SMPCYCCFG16	R/W	Channel 16 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
23:21	SMPCYCCFG17	R/W	Channel 17 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
31:24	Reserved		

25.6.5 ADC sampling time register 2 (ADC_SMPTIM2)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	SMPCYCCFG0	R/W	Channel 0 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
5:3	SMPCYCCFG1	R/W	Channel 1 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
8:6	SMPCYCCFG2	R/W	Channel 2 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
11:9	SMPCYCCFG3	R/W	Channel 3 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
14:12	SMPCYCCFG4	R/W	Channel 4 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
17:15	SMPCYCCFG5	R/W	Channel 5 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
20:18	SMPCYCCFG6	R/W	Channel 6 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
23:21	SMPCYCCFG7	R/W	Channel 7 Sample Cycles Configure

Field	Name	R/W	Description
			Refer to the description of SMPCYCCFG10.
26:24	SMPCYCCFG8	R/W	Channel 8 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
29:27	SMPCYCCFG9	R/W	Channel 9 Sample Cycles Configure Refer to the description of SMPCYCCFG10.
31:30	Reserved		

25.6.6 ADC injected channel data offset register x (ADC_INJDOFx) (x=1..4)

Offset address: 0x14-0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
11:0	INJDOFx	R/W	Data Offset for Injected Channel x When converting the injected channels, these bits define the values to be subtracted from the original converted data, and the result of the conversion can be read in the ADC_INJDATAx register.
31:12	Reserved		

25.6.7 Analog watchdog high-threshold register (ADC_AWDHT)

Offset address: 0x24

Reset value: 0x0000 0FFF

Field	Name	R/W	Description
11:0	AWDHT[11:0]	R/W	Analog Watchdog High Threshold
31:12	Reserved		

25.6.8 Analog watchdog low-threshold register (ADC_AWDLT)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
11:10	AWDLT[11:0]	R/W	Analog Watchdog Low Threshold
31:12	Reserved		

25.6.9 ADC regular sequence register 1 (ADC_REGSEQ1)

Offset address: 0x2C

Reset value: 0x0000 0000

Field	Name	R/W	Description
4:0	REGSEQC13	R/W	13^{th} Conversion In Regular Sequence Define the channel number of No. 13 conversion in regular sequence (0~17)
9:5	REGSEQC14	R/W	14^{th} Conversion In Regular Sequence Refer to the description of REGSEQC13.

Field	Name	R/W	Description
14:10	REGSEQC15	R/W	15th Conversion In Regular Sequence Refer to the description of REGSEQC13.
19:15	REGSEQC16	R/W	16th Conversion In Regular Sequence Refer to the description of REGSEQC13.
23:20	REGSEQLEN	R/W	Regular Channel Sequence Length These bits are defined by software as the number of channels in regular channel conversion sequence. 0000: One conversion 0001: Two conversions …… 1111: 16 conversions
31:24	Reserved		

25.6.10 ADC regular sequence register 2 (ADC_REGSEQ2)

Offset address: 0x30

Reset value: 0x0000 000

Field	Name	R/W	Description
4:0	REGSEQC7	R/W	7th Conversion In Regular Sequence Refer to the description of REGSEQC13.
9:5	REGSEQC8	R/W	8th Conversion In Regular Sequence Refer to the description of REGSEQC13.
14:10	REGSEQC9	R/W	9th Conversion In Regular Sequence Refer to the description of REGSEQC13.
19:15	REGSEQC10	R/W	10th Conversion In Regular Sequence Refer to the description of REGSEQC13.
24:20	REGSEQC11	R/W	11th Conversion In Regular Sequence Refer to the description of REGSEQC13.
29:25	REGSEQC12	R/W	12th Conversion In Regular Sequence Refer to the description of REGSEQC13.
31:30	Reserved		

25.6.11 ADC regular sequence register 3 (ADC_REGSEQ3)

Offset address: 0x34

Reset value: 0x0000 0000

Field	Name	R/W	Description
4:0	REGSEQC1	R/W	1st Conversion In Regular Sequence Refer to the description of REGSEQC13.
9:5	REGSEQC2	R/W	2nd Conversion In Regular Sequence Refer to the description of REGSEQC13.
14:10	REGSEQC3	R/W	3rd Conversion In Regular Sequence Refer to the description of REGSEQC13.
19:15	REGSEQC4	R/W	4th Conversion In Regular Sequence Refer to the description of REGSEQC13.

Field	Name	R/W	Description
24:20	REGSEQC5	R/W	5th Conversion In Regular Sequence Refer to the description of REGSEQC13.
29:25	REGSEQC6	R/W	6th Conversion In Regular Sequence Refer to the description of REGSEQC13.
31:30	Reserved		

25.6.12 ADC injected sequence register (ADC_INJSEQ)

Offset address: 0x38

Reset value: 0x0000 0000

Field	Name	R/W	Description
4:0	INJSEQC1	R/W	1st Conversion In Injected Sequence Define the channel number of No. 1 conversion in injected sequence (0~17)
9:5	INJSEQC2	R/W	2nd Conversion In Injected Sequence
14:10	INJSEQC3	R/W	3rd Conversion In Injected Sequence
19:15	INJSEQC4	R/W	4th Conversion In Injected Sequence
21:20	INJSEQLEN	R/W	Injected Channel Sequence Length These bits are defined by software as the number of channels in injected channel conversion sequence, and the conversion sequence is: INJSEQC(4-INJSEQLEN) →INJSEQ (5-INJSEQLEN) →INJSEQC(6-INJSEQLEN) →INJSEQC(7-INJSEQLEN); the details are as follows: 00: One conversion, only converting INJSEQC4 01: Two conversions; the conversion sequence is INJSEQC3→INJSEQC4 10: Three conversions; the conversion sequence is INJSEQC2→INJSEQC3→INJSEQC4 11: Four conversions; the conversion sequence is INJSEQC1→INJSEQC2→INJSEQC3→INJSEQC4
31:22	Reserved		

25.6.13 ADC injected data register x (ADC_INJDATAx) (x= 1..4)

Offset address: 0x3C–0x48

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	INJDATA	R	Injected Conversion Data Conversion result of injected channel, read-only.
31:16	Reserved		

25.6.14 ADC regular data register (ADC_REGDATA)

Offset address: 0x4C

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	REGDATA	R	Regular Conversion Data Conversion result of regular channel, read-only.
31:16	ADC2DATA	R	ADC2 Conversion Data (1) This bit is valid in ADC1, indicating the result of ADC2 regular channel conversion in dual-ADC mode; (2) This bit is reserved in ADC2.

26 Digital-to-analog Converter (DAC)

26.1 Full Name and Abbreviation Description of Terms

Table 92 Full Name and Abbreviation Description of DAC Terms

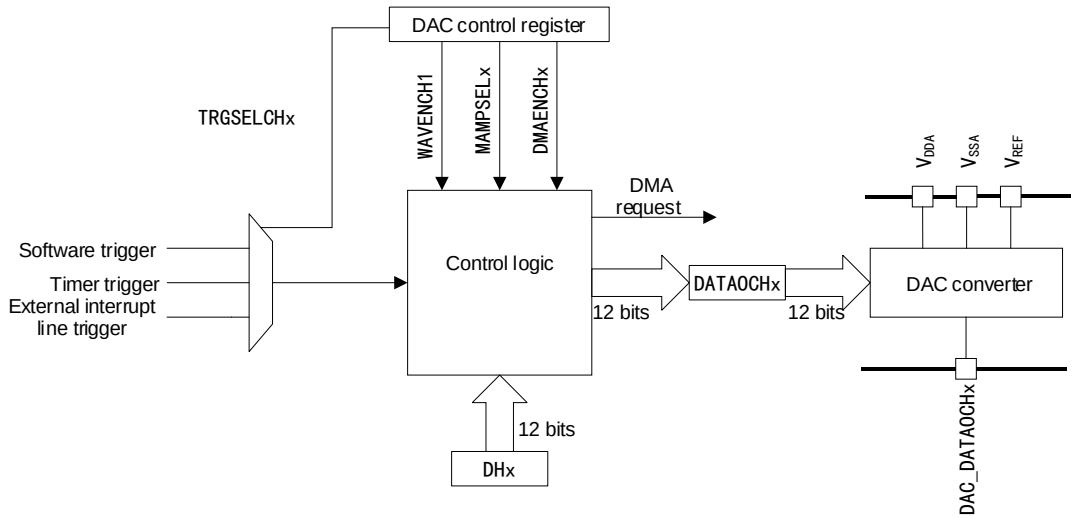
Full name in English	English abbreviation
Linear Feedback Shift Register	LFSR

26.2 Introduction

DAC is a digital/analog converter that can be configured to input 8-bit or 12-bit data and output voltage. When 12-bit data is input, the data can be set to be left aligned or right aligned. It has two-way DAC output channels, which do not affect each other; each channel has multiple trigger sources to trigger conversion; a single channel can trigger conversion output, or both channels can trigger conversion output at the same time. Both channels can generate noise waveform and triangle waveform independently.

26.3 Structure Block Diagram

Figure 113 DAC Structure Block Diagram



26.4 Functional Description

26.4.1 DAC Conversion and Trigger Source

DAC output can obtain corresponding voltage value by calculating the data in DAC_DATAOCHx register. However, it is impossible to write data directly to DAC_DATAOCHx register, and it is required to write to DAC_DHx register and then through corresponding trigger, load the data in DAC_DHx to

DAC_DATAOCHx.

When the channel trigger is disabled (TRGENCHx bit in the register DAC_CTRL is set to 0), write the value in DAC_DHx register and it will be automatically transferred to DAC_DATAOCHx after one APB1 clock cycle.

When the channel trigger is enabled (TRGENCHx bit in the register DAC_CTRL is set to 1), write the value in DAC_DHx register and it will be transferred to DAC_DATAOCHx after different clock cycles according to the selected trigger source. Three types of trigger sources can be selected:

- Timer update event
- External interrupt trigger
- Software trigger

When the update event and external interrupt of the timer are selected as the trigger source, the transmission will be completed after three APB clock cycles; when software trigger is selected, the transmission will be completed after one APB1 clock cycle.

When transmitting the data to DAC_DATAOCHx register, after a period of time, the digital quantity will be outputted after it is converted linearly into analog voltage. The intermediate conversion time will vary according to the power supply voltage and the analog output load.

26.4.2 DAC Reference Voltage and Output

DAC uses V_{REF} as reference voltage and by grounding the V_{SSA}, the output voltage range of DAC can be obtained, namely: 0-V_{REF}.

DAC output calculation formula is: DAC output=V_{REF} * (DATAOCHx/4095).

26.4.3 DAC Data Format

Single-channel DAC

The registers that are written in three modes are as follows

- 8-bit data right aligned: DAC_DH8Rx[7:0]
- 12-bit data left aligned: DAC_DH12Lx[15:4]
- 12-bit data right aligned: DAC_DH12Rx[11:0]

Double-channel DAC

The registers that are written in three modes are as follows

- 8-bit data right aligned: DAC_DH8RD[15:0]
- 12-bit data left aligned: DAC_DH12LDUAL[15:4], DAC_DH12LDUAL[31:20]
- 12-bit data right aligned: DAC_DH12RDUAL[11:0], DAC_DH12RDUAL[27:16]

26.4.4 DAC Waveform Generation

Each channel of DAC can independently generate noise and triangle wave.

26.4.5 DAC Double-channel Conversion

When two channels work at the same time, the written data can be written to the common registers: DH8RDUAL, DH12RDUAL and DH12LDUAL, so as to effectively use the bus bandwidth.

Dual-channel conversion can be divided into independent conversion and synchronous conversion. The specific configuration and description are as follows.

26.4.5.1 Independent trigger

Waveform generator disabled

（1） Enable two-channel trigger mode;

（2） Configure two channels and use different trigger sources.

Use the same LFSR

（1） Enable two-channel trigger mode;

（2） Configure two channels and use different trigger sources;

（3） Enable the noise generation function of two channels, and set the same LFSR mask value.

Use different LFSR

（1） Enable two-channel trigger mode;

（2） Configure two channels and use different trigger sources;

（3） Enable the noise generation function of two channels, and set different LFSR mask value.

Generate the same triangle wave

（1） Enable two-channel trigger mode;

（2） Configure two channels and use different trigger sources;

（3） Enable the triangle wave generation function of two channels, and set the same triangular amplitude.

Generate different triangle wave

（1） Enable two-channel trigger mode;

（2） Configure two channels and use different trigger sources;

（3） Enable the triangle wave generation function of two channels, and set different triangular amplitude.

26.4.5.2 Synchronous trigger

Synchronous software startup

Disable the trigger mode of two channels; after writing data, wait for one APB1 clock cycle and then transfer to DAC_DATAOCH1 and DAC_DATAOCH2 registers at the same time.

Waveform generator disabled

（1） Enable two-channel trigger mode;

（2） Configure two channels and use the same trigger source.

Use the same LFSR

（1） Enable two-channel trigger mode;

（2） Configure two channels and use the same trigger source;

（3） Enable the noise generation function of two channels, and set the same LFSR mask value.

Use different LFSR

（1） Enable two-channel trigger mode;

（2） Configure two channels and use the same trigger source;

（3） Enable the noise generation function of two channels, and set different LFSR mask value.

Generate the same triangle wave

（1） Enable two-channel trigger mode;

（2） Configure two channels and use the same trigger source;

（3） Enable the triangle wave generation function of two channels, and set the same triangular amplitude.

Use different triangle wave

（1） Enable two-channel trigger mode;

（2） Configure two channels and use the same trigger source;

（3） Enable the triangle wave generation function of two channels, and set different triangular amplitude.

26.5 Register Address Mapping

Table 93 DAC Register Address Mapping

Register name	Description	Offset address
DAC_CTRL	DAC control register	0x00
DAC_SWTRG	DAC software trigger register	0x04
DAC_DH12R1	DAC Channel 1 12-bit right-aligned data holding register	0x08
DAC_DH12L1	DAC Channel 1 12-bit left-aligned data holding register	0x0C
DAC_DH8R1	DAC Channel 1 8-bit right-aligned data holding register	0x10
DAC_DH12R2	DAC Channel 2 12-bit right-aligned data holding register	0x14
DAC_DH12L2	DAC Channel 2 12-bit left-aligned data holding register	0x18
DAC_DH8R2	DAC Channel 2 8-bit right-aligned data holding register	0x1C
DAC_DH12RDUAL	Dual-DAC 12-bit right-aligned data holding register	0x20
DAC_DH12LDUAL	Dual-DAC 12-bit left-aligned data holding register	0x24
DAC_DH8RDUAL	Dual-DAC 8-bit right-aligned data holding register	0x28
DAC_DATAOCH1	DAC Channel 1 data output register	0x2C
DAC_DATAOCH2	DAC Channel 2 data output register	0x30

26.6 Register Functional Description

26.6.1 DAC control register (DAC_CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ENCH1	R/W	DAC Channel1 Enable 0: Disable 1: Enable
1	BUFFDCH1	R/W	DAC Channel1 Output Buffer Disable 0: Enable 1: Disable
2	TRGENCH1	R/W	DAC Channel1 Trigger Enable 0: Disable 1: Enable
5:3	TRGSELCH1	R/W	DAC Channel1 Trigger Source Select The trigger source can be selected through this register when Channel 1 trigger is enabled (TRGENCH1=1).

Field	Name	R/W	Description
			000: TMR6 TRGO event 001: TMR8 TRGO event 010: TMR7 TRGO event 011: TMR5 TRGO event 100: TMR2 TRGO event 101: TMR4 TRGO event 110: External interrupt line 9 111: Software trigger
7:6	WAVENCH1	R/W	DAC Channel1 Noise/Triangle Wave Generation Enable 00: Waveform is not generated 10: Noise waveform is generated 1x: Triangle waveform is generated
11:8	MAMPSELCH1	R/W	Select DAC Channel1 LFSR Bit Mask/Triangle Wave Amplitude Selector In the mode of "generating LFSR noise", select the bit to mask LFSR through this bit; In the mode of "generating triangle wave", select the amplitude of triangle wave through this bit. 0000: Unmask LFSR bit [0]/triangle wave amplitude is 1 0001: Unmask LFSR bit [1:0]/triangle wave amplitude is 3 0010: Unmask LFSR bit [2:0]/triangle wave amplitude is 7 0011: Unmask LFSR bit [3:0]/triangle wave amplitude is 15 0100: Unmask LFSR bit [4:0]/triangle wave amplitude is 31 0101: Unmask LFSR bit [5:0]/triangle wave amplitude is 63 0110: Unmask LFSR bit [6:0]/triangle wave amplitude is 127 0111: Unmask LFSR bit [7:0]/triangle wave amplitude is 255 1000: Unmask LFSR bit [8:0]/triangle wave amplitude is 511 1001: Unmask LFSR bit [9:0]/triangle wave amplitude is 1023 1010: Unmask LFSR bit [10:0]/triangle wave amplitude is 2047 ≥1011: Unmask LFSR bit [11:0] / triangle wave amplitude is 4095
12	DMAENCH1	R/W	DAC Channel1 DMA Enable 0: Disable 1: Enable
15:13	Reserved		
16	ENCH2	R/W	DAC Channel2 Enable 0: Disable 1: Enable
17	BUFFDCH2	R/W	DAC Channel2 Output Buffer Disable 0: Enable 1: Disable
18	TRGENCH2	R/W	DAC Channel2 Trigger Enable 0: Disable 1: Enable
21:19	TRGSELCH2	R/W	DAC Channel2 Trigger Source Select The trigger source can be selected through this register when Channel 2 trigger is enabled (TRGENCH2=1)

Field	Name	R/W	Description
			000: TMR6 TRGO event 001: TMR8 TRGO event 010: TMR7 TRGO event 011: TMR5 TRGO event 100: TMR2 TRGO event 101: TMR4 TRGO event 110: External interrupt line 9 111: Software trigger
23:22	WAVENCH2	R/W	DAC Channel2 Noise/Triangle Wave Generation Enable 00: Waveform is not generated 01: Noise waveform is generated 1x: Triangle waveform is generated
27:24	MAMPSELCH2	R/W	Select DAC Channel2 LFSR Bit Mask/Triangle Wave Amplitude Selector In the mode of "generating LFSR noise", select the bit to mask LFSR through this bit; In the mode of "generating triangle wave", select the amplitude of triangle wave through this bit. 0000: Unmask LFSR bit [0]/triangle wave amplitude is 1 0001: Unmask LFSR bit [1:0]/triangle wave amplitude is 3 0010: Unmask LFSR bit [2:0]/triangle wave amplitude is 7 0011: Unmask LFSR bit [3:0]/triangle wave amplitude is 15 0100: Unmask LFSR bit [4:0]/triangle wave amplitude is 31 0101: Unmask LFSR bit [5:0]/triangle wave amplitude is 63 0110: Unmask LFSR bit [6:0]/triangle wave amplitude is 127 0111: Unmask LFSR bit [7:0]/triangle wave amplitude is 255 1000: Unmask LFSR bit [8:0]/triangle wave amplitude is 511 1001: Unmask LFSR bit [9:0]/triangle wave amplitude is 1023 1010: Unmask LFSR bit [10:0]/triangle wave amplitude is 2047 ≥1011: Unmask LFSR bit [11:0] / triangle wave amplitude is 4095
28	DMAENCH2	R/W	DAC Channel2 DMA Enable 0: Disable 1: Enable
31:29	Reserved		

26.6.2 DAC software trigger register (DAC_SWTRG)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SWTRG1	W	DAC Channel1 Software Trigger Enable This bit can be set to 1 and cleared by software; once the data in the register DAC_DH1 is transferred to the register DAC_DATAOCH1, this bit will be cleared by hardware. 0: Disable 1: Enable

Field	Name	R/W	Description
1	SWTRG2	W	DAC Channel2 Software Trigger Enable This bit can be set to 1 and cleared by software; once the data in the register DAC_DH2 is transferred to the register DAC_DATAOCH2, this bit will be cleared by hardware. 0: Disable 1: Enable
31:2	Reserved		

26.6.3 DAC Channel 1 12-bit right-aligned data holding register (DAC_DH12R1)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
11:0	DATA	R/W	DAC Channel1 12-bit Right-Aligned Data This bit is written by the software, representing the data of 12-bit DAC channel 1.
31:12	Reserved		

26.6.4 DAC Channel 1 12-bit left-aligned data holding register (DAC_DH12L1)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	Reserved		
15:4	DATA	R/W	DAC Channel1 12-Bit Left-Aligned Data
31:16	Reserved		

26.6.5 DAC Channel 1 8-bit right-aligned data holding register (DAC_DH8R1)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R/W	DAC Channel1 8-bit Right-Aligned Data
31:8	Reserved		

26.6.6 DAC Channel 2 12-bit right-aligned data holding register (DAC_DH12R2)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
11:0	DATA	R/W	DAC Channel2 12-bit Right-Aligned Data

Field	Name	R/W	Description
31:12	Reserved		

26.6.7 DAC Channel 2 12-bit left-aligned data holding register (DAC_DH12L2)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	Reserved		
15:4	DATA	R/W	DAC Channel2 12-Bit Left-Aligned Data
31:16	Reserved		

26.6.8 DAC Channel 2 8-bit right-aligned data holding register (DAC_DH8R2)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R/W	DAC Channel2 8-bit Right-Aligned Data
31:8	Reserved		

26.6.9 Dual-DAC 12-bit right-aligned data holding register (DAC_DH12RDUAL)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
11:0	DATACH1	R/W	DAC Channel1 12-bit Right-Aligned Data
15:12	Reserved		
27:16	DATACH2	R/W	DAC Channel2 12-bit Right-Aligned Data
31:28	Reserved		

26.6.10 Dual-DAC 12-bit left-aligned data holding register (DAC_DH12LDUAL)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	Reserved		
15:4	DATACH1	R/W	DAC Channel1 12-Bit Left-Aligned Data
19:16	Reserved		
31:20	DATACH2	R/W	DAC Channel212-Bit Left-Aligned Data

26.6.11 Dual-DAC 8-bit right-aligned data holding register (DAC_DH8RDUAL)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATACH1	R/W	DAC Channel1 8-bit Right-Aligned Data
15:8	DATACH2	R/W	DAC Channel2 8-bit Right-Aligned Data
31:16	Reserved		

26.6.12 DAC Channel 1 data output register (DAC_DATAOCH1)

Offset address: 0x2C

Reset value: 0x0000 0000

Field	Name	R/W	Description
11:0	DATA	R	DAC Channel1 Data Output
31:12	Reserved		

26.6.13 DAC Channel 2 data output register (DAC_DATAOCH2)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
11:0	DATA	R	DAC Channel2 Data Output
31:12	Reserved		

27 Cyclic Redundancy Check Computing Unit (CRC)

27.1 Introduction

The cyclic redundancy check (CRC) computing unit can get 32-bit CRC computing result by calculating the input data through a fixed generator polynomial, which is mainly used to detect or verify the correctness and integrity of the data after transmission or saving.

27.2 Functional Description

27.2.1 Calculation Method

Use CRC-32 (Ethernet) polynomial: 0x4C11DB7

$$（X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1）$$

27.2.2 Calculation Time

The calculation time is four AHB clock cycles.

Every time a new data is written, the result will be a combination of the last calculation result and the new calculation result. (Execute operation for the whole word). Write operation of CPU will be suspended during calculation, so that "Back-to-back" write or continuous "read" -"write" operation can be performed for the register CRC_DATA.

27.3 Register Address Mapping

Table 94 CRC Computing Unit Register Address Mapping

Register name	Description	Offset address
DATA	Data register	0x00
INDATA	Independent data register	0x04
CTRL	Control register	0x08

27.4 Register Functional Description

CRC computing unit contains two data registers and one control register.

27.4.1 Data register (CRC_DATA)

Offset address: 0x00

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	DATA	R/W	32bit Data Register It is used as a new data input port for CRC computing during write operation; when the read operation is executed, the result of CRC computing is returned.

27.4.2 Independent data register (CRC_INDATA)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	INDATA	R/W	Independent 8bit Data Register It can be used to temporarily store 1-byte data; the CRC reset generated by RST bit of the register CRC_CTRL has no effect on this register.
31:8	Reserved.		

Note: This register does not take part in CRC calculation and can store any data.

27.4.3 Control register (CRC_CTRL)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	RST	W	Reset CRC Calculation Unit After reset, set the data register as 0xFFFF FFFF, and this bit can only be written as 1 by software and automatically cleared by hardware.
31:1	Reserved		

28 Chip electronic signature

The chip electronic signature includes flash capacity information of main memory and 96-bit unique chip ID, which have been written into the system memory area of the chip before leaving the factory, and are read-only and can not be modified by users.

28.1 Capacity register of main memory area

28.1.1 Flash capacity register (16 bits)

Base address: 0x1FFF F7E0

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
15:0	F_SIZE	R	Flash Size Indicate the capacity of main memory area of the product (in KB). For example: 0x0800=256 KB

28.2 96-bit unique chip ID

Purposes of unique ID may be:

- As serial number (such as USBD character serial number or other terminal application)
- As a password; this unique identification can be used with software encryption and decryption algorithm to improve the security of the code in flash memory when writing the flash memory
- Used to activate the startup process with security mechanism
- The reference number provided by the identity is unique to any MCU series. Users cannot change the unique ID under no circumstances. According to different usage, users can choose to read the identity in byte, half word, or full word.

Base address: 0x1FFF F7E8

Offset address: 0x00

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
15:0	U_ID[15:0]	R	Unique identity flag 15:0 bits

Offset address: 0x02

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
15:0	U_ID[31:16]	R	Unique identity flag 31:16 bits

Offset address: 0x04

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
31:0	U_ID[63:32]	R	Unique identity flag 63:32 bits

Offset address: 0x08

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
31:0	U_ID[95:64]	R	Unique identity flag 95:64 bits

29 Version History

Table 95 Document Version History

Date	Version	Change History
Sep, 2022	0.1	New
Oct 31, 2022	0.2	(1) Modify clock tree (2) Modify RCM_ CFG1 register bit field description
Feb 7, 2023	0.3	(1) Modify the maximum value of APB1 clock frequency in the clock configuration register of the RCM module (2) Replace the SMREQ with SLEEPREQ in the document (3) Add the Version Recognition Number of “Device ID register” in DBGMCU module (4) Modify RCM_ CFG1 register bit field description

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