QUECTEL

SC606T Series
Hardware Design

Smart Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

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-	2021-01-25	Dorian MENG/ Mike ZENG	Creation of the document
1.0	2021-03-16	Dorian MENG/ Mike ZENG	First official release
1.1	2021-06-30	Dorian MENG/ Kevin JIN	1. Deleted information of SC606T-JP model. 2. Updated data in the Wi-Fi transmitting and receiving performance tables (Table 24 and Table 25). 3. Updated dimension tolerances not specified in the figures from 0.05 mm to 0.2 mm (Chapter 8). 4. Updated the note of storage chapter and temperature information of the recommended thermal profile parameters (Chapter 9).

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1 Introduction

This document provides information on the functional features, interface specifications, as well as electrical and mechanical details of the SC606T series modules (SC606T-EM, SC606T-NA, and SC606T-WF). Consult this document to learn about the air and hardware interfaces and external application reference designs among other related information of the series modules.

This document, coupled with application notes and user guides, makes it easy to design applications with the module.

2 Product Concept

2.1. General Description

SC606T is a series of smart modules applicable to Linux operating system and provides industrial-grade performance. Their general features are listed below:

- Support LTE-FDD, LTE-TDD, DC-HSDPA, DC-HSUPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE, GPRS and GSM;
- Support short-range wireless communication via Wi-Fi 802.11a/b/g/n/ac and *Bluetooth Core Specification Version 4.2*;
- Integrate GPS, GLONASS, BeiDou/COMPASS satellite positioning systems
- Support multiple audio and video codecs;
- With the built-in high-performance Adreno™506 graphics processing unit;
- Provide multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

The series comes in SC606T-EM, SC606T-NA, and SC606T-WF models.

The following tables show the frequency bands, CA combinations, as well as the Wi-Fi, Bluetooth, and GNSS frequency bands supported by each model.

Table 1: Frequency Bands, CA Combinations and GNSS Types of SC606T-EM

Mode	Details
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B20/B28A/B28B
LTE-TDD	B38/B40/B41
Intra-band 2CA (DL)	1A-1A, 1C, 2A-2A, 2C, 3A-3A, 3C, 4A-4A, 5A-5A, 5B, 7A-7A, 7C, 38C, 39C, 40C, 41A-41A, 41C
WCDMA	B1/B2/B4/B5/B8
GSM	850/900/1800/1900 MHz
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz; 5180–5825 MHz
Bluetooth	2402–2480 MHz

GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou/COMPASS: 1561.098 ±2.046 MHz

Table 2: Frequency Bands, CA Combinations and GNSS Types of SC606T-NA

Mode	Details
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41
Intra-band 2CA (DL)	2A-2A, 2C, 4A-4A, 5A-5A, 5B, 7A-7A,7C, 66A-66A, 66B, 66C, 41A-41A, 41C
WCDMA	B2/B4/B5
GSM	-
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz; 5180–5825 MHz
Bluetooth	2402–2480 MHz
GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou/COMPASS: 1561.098 ±2.046 MHz

Table 3: Frequency Bands of SC606T-WF

Mode	Details
LTE-FDD	-
LTE-TDD	-
WCDMA	-
GSM	-
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz; 5180–5825 MHz
Bluetooth	2402–2480 MHz
GNSS	-

SC606T is a series of SMD-type modules which can be embedded into applications through their 323 pins (152 LCC pins and 171 LGA pins). With a compact profile of 43.0 mm × 44.0 mm × 2.85 mm, a SC606T module can meet almost all requirements for M2M applications such as smart metering, smart

home, security, wireless POS, mobile computing devices, PDA phone and tablet PC.

2.2. Key Features

Table 4: Key Features

Features	Details
Application Processor	Octa-core ARM Cortex-A53 64-bit CPU @ 2.0 GHz (high performance) ● One quad-core with 1 MB L2 cache ● One quad-core with 512 KB L2 cache
Modem system	Hexagon DSP V56 core, up to 850 MHz 768 KB L2 caches
GPU	Adreno™ 506 with 64-bit addressing, designed for 650 MHz
Memory	16 GB eMMC + 2 GB LPDDR3 (default) 32 GB eMMC + 3 GB LPDDR3 (optional) 64 GB eMMC + 4 GB LPDDR3 (optional)
Operating System	Linux OS
Power Supply	VBAT Supply Voltage: 3.55–4.4 V Typical: 3.8 V
Transmitting Power	Class 4 (33 dBm ±2 dB) for GSM850 Class 4 (33 dBm ±2 dB) for EGSM900 Class 1 (30 dBm ±2 dB) for DCS1800 Class 1 (30 dBm ±2 dB) for PCS1900 Class E2 (27 dBm ±3 dB) for GSM850 8-PSK Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK Class 3 (24 dBm +1/-3 dB) for WCDMA bands Class 3 (23 dBm ±2 dB) for LTE-FDD bands Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	Support 3GPP Rel-10 Cat 6 and Cat 4 Support 1.4 to 20 MHz RF bandwidths Support Multiuser MIMO in DL direction ● Cat 6 FDD: Max 300 Mbps (DL)/Max 50 Mbps (UL) ● Cat 6 TDD: Max 265 Mbps (DL)/Max 30 Mbps (UL) ● Cat 4 FDD: Max 150 Mbps (DL)/Max 50 Mbps (UL) ● Cat 4 TDD: Max 130 Mbps (DL)/Max 30 Mbps (UL)
UMTS Features	Support 3GPP Rel-9 DC-HSDPA/DC-HSUPA/HSPA+/HSDPA/HSUPA/WCDMA

	Support QPSK, 16QAM and 64QAM modulation ● DC-HSDPA: Max. 42 Mbps (DL) ● DC-HSUPA: Max. 11.2 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/Max. 384 kbps (UL)
GSM Features	**R99** CSD: 9.6 kbps, 14.4 kbps **GPRS** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max. 107 kbps (DL), 85.6 kbps (UL) **EDGE** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: MCS 1-9 Uplink coding schemes: MCS 1-9 Max. 296 kbps (DL), 236.8 kbps (UL)
WLAN Features	2.4/5 GHz, 802.11a/b/g/n/ac, maximally up to 433 Mbps Support AP and STA modes
Bluetooth Features	***Bluetooth Core Specification Version 4.2***
GNSS Features	GPS; GLONASS; BeiDou/COMPASS
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast
LCM Interfaces	Support two groups of 4-lane MIPI_DSI Support dual LCDs Support WUXGA up to 1200 (RGB) × 1920 @ 60 fps
Camera Interfaces	Support three groups of 4-lane MIPI_CSI, up to 2.1 Gbps per lane Support 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane) Up to 24 MP with dual ISP
Video Codec	Video encoding and decoding: up to 4 K @ 30 fps, up to 1080 P @ 60 fps Wi-Fi Video: encoding up to 1080 P @ 30 fps; decoding up to 1080 P @ 60 fps
Audio Interfaces	**Audio Input** Three analog microphone inputs **Audio Output** Class AB stereo headphone output Class AB earpiece differential output Class D speaker differential amplifier output
Audio Codec	Support G711, QCELP, EVRC, EVRC-B, EVRC-WB, AMR-NB, AMR-WB, GSM-EFR, GSM-FR, GSM-HR

USB Interface	Support USB 3.0 or 2.0, with transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 Support USB OTG Used for AT command communication, data transmission, software debugging and firmware upgrade
UART Interfaces	Three UART Interfaces: UART5, UART4, and UART2 ● UART5: 4-wire UART interface with hardware flow control (RTS/CTS), baud rate up to 4 Mbps ● UART4: 2-wire UART interface ● UART2: 2-wire UART interface used for debugging
SD Card Interface	Support SD 3.0 Support SD card hot-plug
(U)SIM Interfaces	Two (U)SIM interfaces Support USIM/SIM card: 1.8/2.95 V Support Dual SIM Dual Standby by default
I2C Interfaces	Five I2C interfaces, used for peripherals such as TP, camera and sensor
ADC Interface	One general-purpose ADC interface Support up to 15-bit ADC resolution
SPI Interfaces	Two SPI interfaces, only support master mode ● One SPI interface used for peripheral device ● One SPI interface used for sensor application, such as fingerprint sensor
Real Time Clock	Supported
Antenna Interfaces	Main antenna, Rx-diversity antenna, GNSS antenna, Wi-Fi/Bluetooth antenna, and FM antenna
Physical Characteristics	Size: (43.0 ±0.15) mm × (44.0 ±0.15) mm × (2.85 ±0.2) mm Package: LCC + LGA Weight: approx. 13.0 g
Temperature Range	Operating temperature range: -35 to +75 °C [1] Storage temperature range: -40 to +90 °C
Firmware Upgrade	Over USB interface
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] Within the operating temperature range, the module is 3GPP compliant.

2.3. Functional Diagram

The following figure shows a block diagram of the series and illustrates the major functional parts.

- Power management
- Radio frequency
- Baseband
- LPDDR3 + eMMC flash
- Peripheral interfaces
  -- VRTC interface
  -- USB interface
  -- UART interfaces
  -- (U)SIM interfaces
  -- SD card interface
  -- GPIO interfaces
  -- I2C interfaces
  -- SPI interfaces
  -- ADC interface
  -- LCM (MIPI) interfaces
  -- Touch Panel (TP) interfaces
  -- Camera (MIPI) interfaces
  -- Sensor interfaces
  -- Audio interfaces
  -- USB_BOOT interface

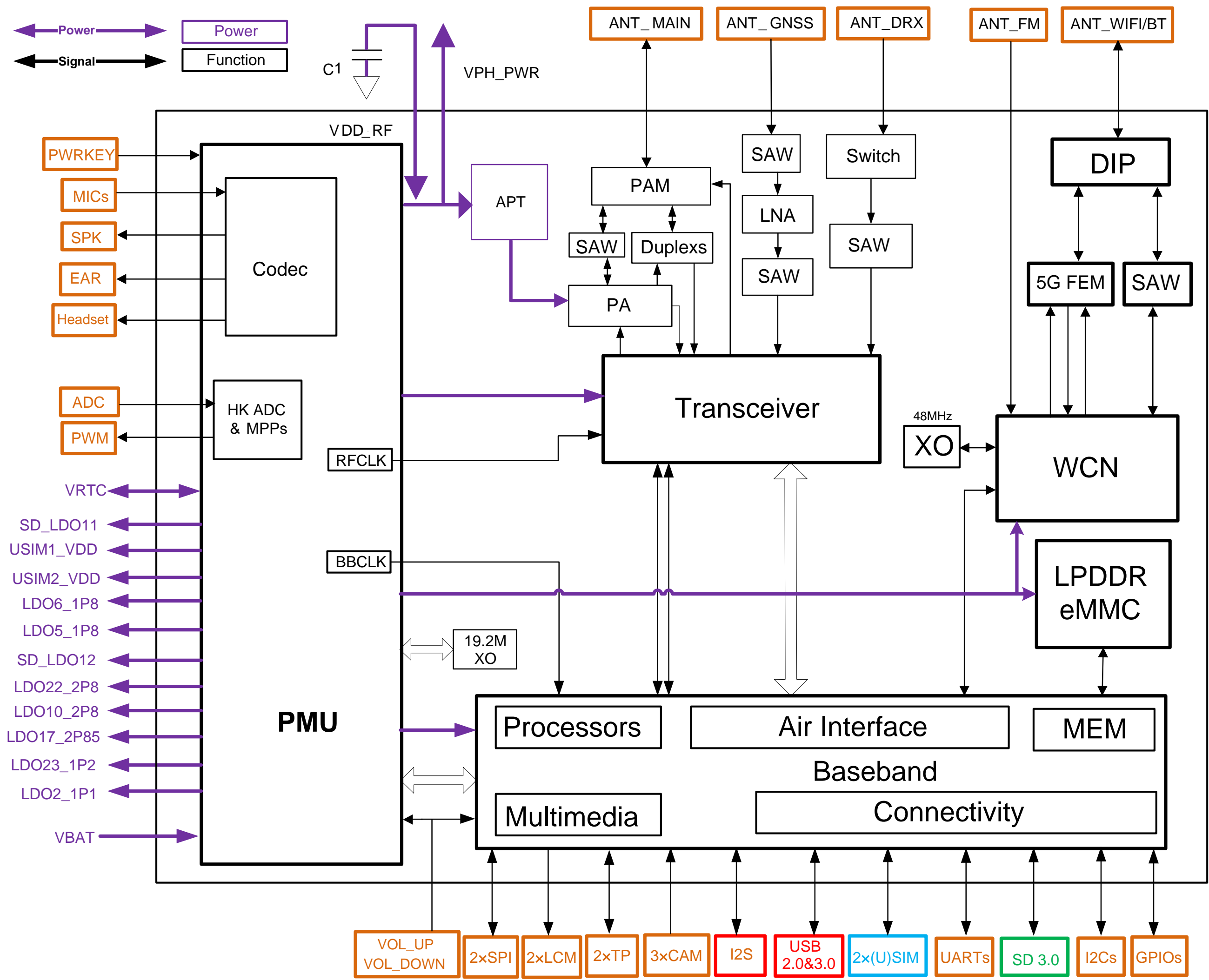

Figure 1: Functional Diagram

2.4. Evaluation Board

To help you develop applications with the module conveniently, Quectel supplies an evaluation board, a USB to RS232 converter cable, a USB Type-C data cable, a power adapter, an earphone, an antenna, and other peripherals to control or test the module. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

The following chapters describe in detail the pins/interfaces listed below.

- Power supply
- VRTC interface
- USB interface
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- SPI interfaces
- ADC interface
- LCM interfaces
- TP interfaces
- Camera interfaces
- Sensor interfaces
- Audio interfaces
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of the series.

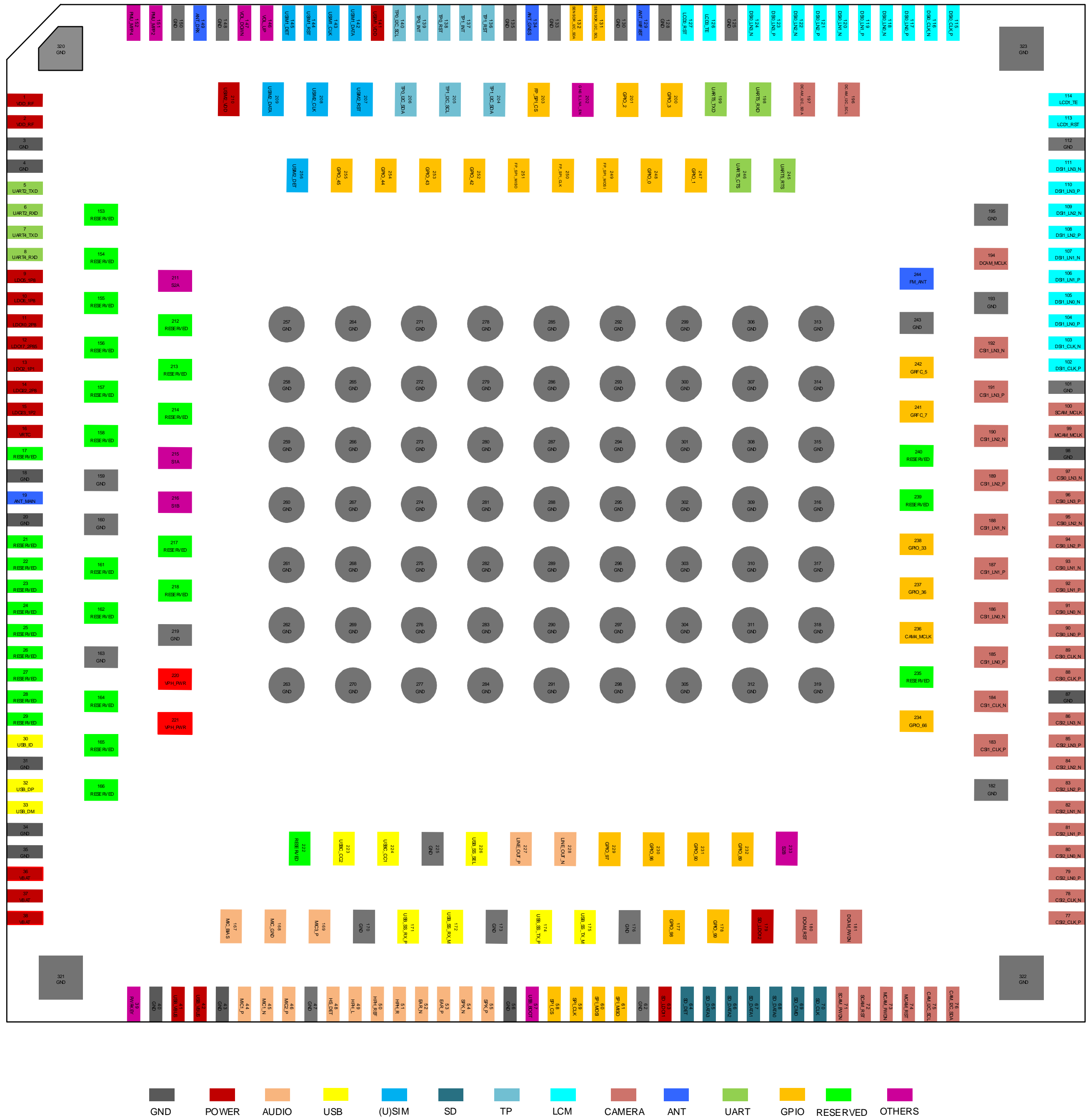

Figure 2: Pin Assignment (Perspective View)

3.3. Pin Description

Table 5: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
AIO	Analog input/output
DI	Digital input
DO	Digital output
DIO	Digital input/output
OD	Open drain
PI	Power input
PO	Power output

The following tables show the module's pin definition and electrical characteristics.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	36, 37, 38	PI/ PO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It must be provided with a sufficient current of at least 3.0 A. A TVS is suggested to be applied to increase the voltage surge withstand capability.
VDD_RF	1, 2	PO	Connects to external bypass capacitors to eliminate voltage		It cannot be used to power external loads.

			fluctuation of the RF part		
VPH_PWR	220, 221	PO	Power supply for peripherals	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It can provide a maximum continuous current of about 1 A. The value of capacitors put on this pin should not exceed 120 μF.
VRTC	16	PI/ PO	Power supply for RTC	$V_O$max = 3.2 V V_I = 2.0–3.25 V	
LDO5_1P8	9	PO	1.8 V output power for external GPIO's pull-up circuits and level shifter	Vnom = 1.8 V $I_O$max = 20 mA	
LDO10_2P8	11	PO	2.8 V output power for VDD of sensors and TPs	Vnom = 2.8 V $I_O$max = 150 mA	Add a 1.0–4.7 μF bypass capacitor if the pin is used. If unused, keep this pin open.
LDO6_1P8	10	PO	1.8 V output power for I/O VDD of cameras, LCDs and sensors	Vnom = 1.8 V $I_O$max = 300 mA	Add a 1.0–2.2 μF bypass capacitor if the pin is used. If unused, keep this pin open.
LDO17_ 2P85	12	PO	2.85 V output power for cameras and LCDs	Vnom = 2.85 V $I_O$max = 300 mA	Add a 1.0–4.7 μF bypass capacitor if this pin is used. If unused, keep this pin open.
LDO23_1P2	15	PO	1.2 V output power for DVDD of the front camera	Vnom = 1.2 V $I_O$max = 600 mA	Add a 1.0–2.2 μF bypass capacitor if this pin is used. If unused, keep this pin open.
LDO2_1P1	13	PO	1.1 V output power for DVDD of the rear camera	Vnom = 1.1 V $I_O$max = 1200 mA	Add a 1.0–2.2 μF bypass capacitor if this pin is used. If unused, keep this pin open.
LDO22_2P8	14	PO	2.8 V output power for AVDD of camera	Vnom = 2.8 V $I_O$max = 150 mA	Add a 1.0–4.7 μF bypass capacitor

					if this pin is used. If unused, keep this pin open.
GND	3, 4, 18, 20, 31, 34, 35, 40, 43, 47, 56, 62, 87, 98, 101, 112, 125, 128, 130, 133, 135, 148, 150, 159, 160, 163, 170, 173, 176, 182, 193, 195, 219, 225, 243, 257–323				
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS	167	PO	Bias voltage output for microphone	V_O = 1.6–2.85V	
MIC1_P	44	AI	Microphone input for channel 1 (+)		
MIC1_N	45	AI	Microphone input for channel 1 (-)		
MIC_GND	168		Microphone reference ground		If this pin is unused, connect it to the ground.
MIC2_P	46	AI	Microphone input for headset (+)		
MIC3_P	169	AI	Microphone input for channel 2 (+)		
EAR_P	53	AO	Earpiece output (+)		
EAR_N	52	AO	Earpiece output (-)		
SPK_P	55	AO	Speaker output (+)		
SPK_N	54	AO	Speaker output (-)		
HPH_R	51	AO	Headphone right channel output		
HPH_REF	50	AI	Headphone reference ground		It should be connected to the main GND.
HPH_L	49	AO	Headphone left channel output		
HS_DET	48	AI	Headset hot-plug detect		Pulled up internally.
LINE_OUT_P	227	AO	Audio line differential output (+)		
LINE_OUT_N	228	AO	Audio line differential output (-)		
USB Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	41, 42	AI	USB connection detect	Vmax = 10.0 V Vmin = 4.0 V Vnom = 5.0 V	
USB_DM	33	AIO	USB differential data (-)		90 Ω differential impedance. USB 2.0 standard compliant.
USB_DP	32	AIO	USB differential data (+)		
USB_ID	30	DO	USB ID detect		High level by default.
GPIO_1	247	DI	USB ID interrupt detection		Pulled up internally. If the default function of this pin is not used, it can be configured into a general-purpose GPIO.
USB_SS_RX_P	171	AI	USB 3.0 super-speed receive (+)		90 Ω differential impedance. USB 3.0 standard compliant.
USB_SS_RX_M	172	AI	USB 3.0 super-speed receive (-)		
USB_SS_TX_P	174	AO	USB 3.0 super-speed transmit (+)		
USB_SS_TX_M	175	AO	USB 3.0 super-speed transmit (-)		
USBC_CC2	223	AIO	USB Type-C control configuration channel 2		
USBC_CC1	224	AIO	USB Type-C control configuration channel 1		
USB_SS_SEL	226	DO	USB Type-C switch control		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low. Require to be externally pulled up to 1.8 V. If unused, keep it

					open. Disabled by default, but can be enabled through software configuration.
USIM1_RST	144	DO	(U)SIM1 card reset	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	
USIM1_CLK	143	DO	(U)SIM1 card clock	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	
USIM1_DATA	142	DIO	(U)SIM1 card data	V_{IL}max = 0.2 × USIM1_VDD V_{IH}min = 0.7 × USIM1_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	Requires to be pulled up to USIM1_VDD with a 10 kΩ resistor.
USIM1_VDD	141	PO	(U)SIM1 card power supply	**1.8 V (U)SIM:** Vmax = 1.90 V Vmin = 1.70 V **2.95 V (U)SIM:** Vmax = 3.04 V Vmin = 2.7 V	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM2_DET	256	DI	(U)SIM2 card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low. Requires to be externally pulled up to 1.8 V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.
USIM2_RST	207	DO	(U)SIM2 card reset	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	
USIM2_CLK	208	DO	(U)SIM2 card clock	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	
USIM2_DATA	209	DIO	(U)SIM2 card data	V_{IL}max =	Requires to be

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
				0.2 × USIM2_VDD V_{IH}min = 0.7 × USIM2_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	pulled up to USIM2_VDD with a 10 kΩ resistor.
USIM2_VDD	210	PO	(U)SIM2 card power supply	**1.8 V (U)SIM:** Vmax = 1.90 V Vmin = 1.70 V **2.95 V (U)SIM:** Vmax = 3.04 V Vmin = 2.7 V	Either 1.8 V or 2.95 V (U)SIM card is supported.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART2_TXD	5	DO	UART2 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep these pins open.
UART2_RXD	6	DI	UART2 receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART4_TXD	7	DO	UART4 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART4_RXD	8	DI	UART4 receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART5_RXD	198	DI	UART5 receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART5_TXD	199	DO	UART5 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART5_RTS	245	DO	UART5 request to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART5_CTS	246	DI	UART5 clear to send	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	70	DO	SD card clock	**1.8 V SD card:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.95 V SD card:** V_{OL}max = 0.37 V V_{OH}min = 2.2 V	
SD_CMD	69	DIO	SD card command	**1.8 V SD card:** V_{IL}max = 0.58 V	

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
				$V_{IH}min$ = 1.27 V $V_{OL}max$ = 0.45 V $V_{OH}min$ = 1.4 V **2.95 V SD card:** $V_{IL}max$ = 0.73 V $V_{IH}min$ = 1.84 V $V_{OL}max$ = 0.37 V $V_{OH}min$ = 2.2 V	
SD_DATA0	68	DIO	SDIO data bit 0	**1.8 V SD card:** $V_{IL}max$ = 0.58 V $V_{IH}min$ = 1.27 V $V_{OL}max$ = 0.45 V $V_{OH}min$ = 1.4 V **2.95 V SD card:** $V_{IL}max$ = 0.73 V $V_{IH}min$ = 1.84 V $V_{OL}max$ = 0.37 V $V_{OH}min$ = 2.2 V	
SD_DATA1	67	DIO	SDIO data bit 1		
SD_DATA2	66	DIO	SDIO data bit 2		
SD_DATA3	65	DIO	SDIO data bit 3		
SD_DET	64	DI	SD card hot-plug detect	$V_{IL}max$ = 0.63 V $V_{IH}min$ = 1.17 V	Active low.
SD_LDO11	63	PO	SD card power supply	Vnom = 2.95 V $I_{O}max$ = 800 mA	
SD_LDO12	179	PO	1.8/2.95 V output power for SD card pull-up circuits	Vnom = 1.8/2.95 V $I_{O}max$ = 50 mA	
TP (Touch Panel) Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP0_RST	138	DO	TP0 reset	$V_{OL}max$ = 0.45 V $V_{OH}min$ = 1.35 V	1.8 V power domain. Active low.
TP0_INT	139	DI	TP0 interrupt	$V_{IL}max$ = 0.63 V $V_{IH}min$ = 1.17 V	1.8 V power domain.
TP0_I2C_SCL	140	OD	TP0 I2C clock		1.8 V power domain.
TP0_I2C_SDA	206	OD	TP0 I2C data		1.8 V power domain.
TP1_RST	136	DO	TP1 reset	$V_{OL}max$ = 0.45 V $V_{OH}min$ = 1.35 V	1.8 V power domain. Active low.
TP1_INT	137	DI	TP1 interrupt	$V_{IL}max$ = 0.63 V $V_{IH}min$ = 1.17 V	1.8 V power domain.

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
TP1_I2C_SDA	204	OD	TP1 I2C data		1.8 V power domain.
TP1_I2C_SCL	205	OD	TP1 I2C clock		1.8 V power domain.
LCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PMU_MPP4	152	DO	General-purpose ADC interface	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
GPIO_33	238	DO	General-purpose clock output for blacklight driver		If the default function of this pin is not used, it can be configured into a general-purpose GPIO.
LCD0_RST	127	DO	LCD0 reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active low.
LCD0_TE	126	DI	LCD0 tearing effect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
LCD1_RST	113	DO	LCD1 reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active low.
LCD1_TE	114	DI	LCD1 tearing effect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
DSI0_CLK_N	116	AO	LCD0 MIPI clock (-)		
DSI0_CLK_P	115	AO	LCD0 MIPI clock (+)		
DSI0_LN0_N	118	AO	LCD0 MIPI lane 0 data (-)		
DSI0_LN0_P	117	AO	LCD0 MIPI lane 0 data (+)		
DSI0_LN1_N	120	AO	LCD0 MIPI lane 1 data (-)		
DSI0_LN1_P	119	AO	LCD0 MIPI lane 1 data (+)		
DSI0_LN2_N	122	AO	LCD0 MIPI lane 2 data (-)		
DSI0_LN2_P	121	AO	LCD0 MIPI lane 2 data (+)		
DSI0_LN3_N	124	AO	LCD0 MIPI lane 3 data (-)		

DSI0_LN3_P	123	AO	LCD0 MIPI lane 3 data (+)		
DSI1_CLK_N	103	AO	LCD1 MIPI clock (-)		
DSI1_CLK_P	102	AO	LCD1 MIPI clock(+)		
DSI1_LN0_N	105	AO	LCD1 MIPI lane 0 data (-)		
DSI1_LN0_P	104	AO	LCD1 MIPI lane 0 data (+)		
DSI1_LN1_N	107	AO	LCD1 MIPI lane 1 data (-)		
DSI1_LN1_P	106	AO	LCD1 MIPI lane 1 data (+)		
DSI1_LN2_N	109	AO	LCD1 MIPI lane 2 data (-)		
DSI1_LN2_P	108	AO	LCD1 MIPI lane 2 data (+)		
DSI1_LN3_N	111	AO	LCD1 MIPI lane 3 data (-)		
DSI1_LN3_P	110	AO	LCD1 MIPI lane 3 data (+)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_N	89	AI	MIPI clock of rear camera (-)		
CSI0_CLK_P	88	AI	MIPI clock of rear camera (+)		
CSI0_LN0_N	91	AI	MIPI lane 0 data of rear camera (-)		
CSI0_LN0_P	90	AI	MIPI lane 0 data of rear camera (+)		
CSI0_LN1_N	93	AI	MIPI lane 1 data of rear camera (-)		
CSI0_LN1_P	92	AI	MIPI lane 1 data of rear camera (+)		
CSI0_LN2_N	95	AI	MIPI lane 2 data of rear camera (-)		
CSI0_LN2_P	94	AI	MIPI lane 2 data of rear camera (+)		
CSI0_LN3_N	97	AI	MIPI lane 3 data of rear camera (-)		

CSI0_LN3_P	96	AI	MIPI lane 3 data of rear camera (+)
CSI1_CLK_N	184	AI	MIPI clock of depth camera (-)
CSI1_CLK_P	183	AI	MIPI clock of depth camera (+)
CSI1_LN0_N	186	AI	MIPI lane 0 data of depth camera (-)
CSI1_LN0_P	185	AI	MIPI lane 0 data of depth camera (+)
CSI1_LN1_N	188	AI	MIPI lane 1 data of depth camera (-)
CSI1_LN1_P	187	AI	MIPI lane 1 data of depth camera (+)
CSI1_LN2_N	190	AI	MIPI lane 2 data of depth camera (-)
CSI1_LN2_P	189	AI	MIPI lane 2 data of depth camera (+)
CSI1_LN3_N	192	AI	MIPI lane 3 data of depth camera (-)
CSI1_LN3_P	191	AI	MIPI lane 3 data of depth camera (+)
CSI2_CLK_N	78	AI	MIPI clock of front camera (-)
CSI2_CLK_P	77	AI	MIPI clock of front camera (+)
CSI2_LN0_N	80	AI	MIPI lane 0 data of front camera (-)
CSI2_LN0_P	79	AI	MIPI lane 0 data of front camera (+)
CSI2_LN1_N	82	AI	MIPI lane 1 data of front camera (-)
CSI2_LN1_P	81	AI	MIPI lane 1 data of front camera (+)
CSI2_LN2_N	84	AI	MIPI lane 2 data of front camera (-)
CSI2_LN2_P	83	AI	MIPI lane 2 data of front camera (+)
CSI2_LN3_N	86	AI	MIPI lane 3 data of front camera (-)
CSI2_LN3_P	85	AI	MIPI lane 3 data of front camera (+)

MCAM_MCLK	99	DO	Master clock of rear camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
SCAM_MCLK	100	DO	Master clock of front camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
MCAM_RST	74	DO	Reset of rear camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
MCAM_PWDN	73	DO	Power down of rear camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
SCAM_RST	72	DO	Reset of front camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
SCAM_PWDN	71	DO	Power down of front camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras		1.8 V power domain.
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras		1.8 V power domain.
DCAM_MCLK	194	DO	Master clock of depth camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
CAM4_MCLK	236	DO	Master clock of fourth camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
DCAM_RST	180	DO	Reset of depth camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
DCAM_PWDN	181	DO	Power down of depth camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
DCAM_I2C_SDA	197	OD	I2C data of depth camera		1.8 V power domain.
DCAM_I2C_SCL	196	OD	I2C clock of depth camera		1.8 V power domain.
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	39	DI	Turn on/off the module	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Pulled up to 1.8 V internally. Active low.
VOL_UP	146	DI	Volume up	V_{IL}max = 0.63 V V_{IH}min=1.17 V	If unused, keep this pin open.
VOL_DOWN	147	DI	Volume down	V_{IL}max=0.63 V V_{IH}min= 1.17 V	If unused, keep this pin open.
SENSOR_I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor		1.8 V power domain.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor		1.8 V power domain.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PMU_MPP2	151	AI	General-purpose ADC interface		Maximum input voltage: 1.7 V.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	19	AIO	Main antenna interface		50 Ω impedance.
ANT_DRX	149	AI	Diversity antenna interface		
ANT_GNSS	134	AI	GNSS antenna interface		
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface		
FM_ANT	244	AI	FM antenna interface		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_0	248	DIO	General-purpose input/output	$V_{IL}max$ = 0.63 V $V_{IH}min$ = 1.17 V $V_{OL}max$ = 0.45 V $V_{OH}min$ = 1.4 V	
GPIO_2	201	DIO	General-purpose input/output		
GPIO_3	200	DIO	General-purpose input/output		
GPIO_33	238	DIO	General-purpose input/output		
GPIO_36	237	DIO	General-purpose input/output		
GPIO_42	252	DIO	General-purpose input/output		
GPIO_43	253	DIO	General-purpose input/output		
GPIO_44	254	DIO	General-purpose input/output		

GPIO_45	255	DIO	General-purpose input/output		
GPIO_66	234	DIO	General-purpose input/output		
GPIO_89	232	DIO	General-purpose input/output		
GPIO_90	231	DIO	General-purpose input/output		
GPIO_96	230	DIO	General-purpose input/output		
GPIO_97	229	DIO	General-purpose input/output		
GPIO_98	177	DIO	General-purpose input/output		
GPIO_99	178	DIO	General-purpose input/output		
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	58	DO	SPI chip select		
SPI_CLK	59	DO	SPI clock		
SPI_MOSI	60	DO	SPI master-out slave-in		
SPI_MISO	61	DI	SPI master-in salve-out		
FP_SPI_CS	203	DO	FP SPI chip select		
FP_SPI_CLK	250	DO	FP SPI clock		
FP_SPI_MOSI	249	DO	FP SPI master-out slave-in		
FP_SPI_MISO	251	DI	FP SPI master-in salve-out		
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	57	DI	Force the module into emergency download mode		Pulling it up to LDO5_1P8 during power-up forces the module into emergency download mode.

Other Interfaces					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GNSS_LNA_EN	202	DO	GNSS LNA enable control		For test purpose only. If unused, keep this pin open.
GRFC_5	242	DIO	Generic RF controller		Only used for RF tuner control.
GRFC_7	241	DIO	Generic RF controller		
S1A	215		S1A and S1B are connected in the module		
S1B	216				
S2A	211		S2A and S2B are connected in the module		
S2B	233				

Reserved Interface		
Pin Name	Pin No.	Comment
RESERVED	17, 21–29, 153–158, 161, 162, 164–166, 212–214, 217, 218, 222, 235, 239, 240	Keep these pins open.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides 3 VBAT pins and 2 VPH_PWR pins. VBAT pins are dedicated for connection with an external power supply. VPH_PWR pins can supply power for peripherals, and they can provide a maximum continuous current of 1 A approximately. The value of capacitors placed on the VPH_PWR pins should not exceed 120 μF.

3.4.2. Decrease Voltage Drop

The power supply range of the module is from 3.55 V to 4.4 V, and the recommended value is 3.8 V. The power supply performance, such as the power supply capacity and voltage ripple, directly influences the module’s performance and stability. Under extreme conditions, the module may have a transient peak current up to 3 A. If the power supply capacity is not sufficient, there will be the risk that the voltage drops below 3.1 V and as a result the module powers off automatically. Therefore, it is necessary to ensure that the input voltage never drops below 3.1 V.

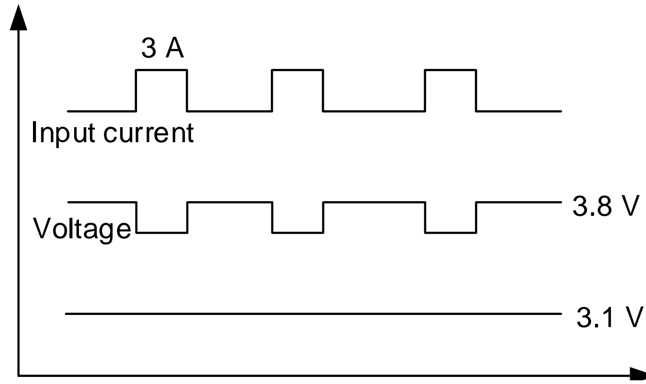

Figure 3: Voltage Drop Sample

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (0.7 Ω) should be used for VBAT pins, and multi-layer ceramic chip capacitor (MLCC) arrays should be added for their ultra-low ESR. It is suggested to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose each MLCC array and place these arrays close to the VBAT/VDD_RF/VPH_PWR pins separately. The width of the VBAT trace should be no less than 3 mm. In theory, the longer the VBAT trace is, the wider it should be. In addition, in order to get a stable power source, it is suggested to place a 2000 W TVS as close to the VBAT pins as possible to increase voltage surge withstand capability. The following figure shows the structure of the power supply.

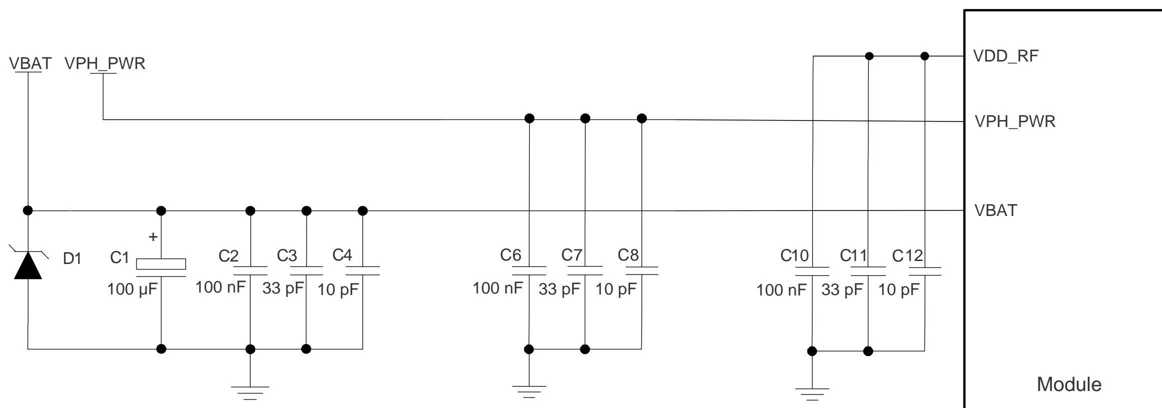

Figure 4: Star Structure of Power Supply

3.4.3. Reference Design for Power Supply

A good power design for the module is essential, as the performance of the module largely depends on the capacity and reliability of the power supply. The power supply of the module should be able to provide a sufficient current of at least 3 A. It is recommended to use a battery to supply power for the module, and that if not using a battery, add a voltage regulator. In the latter case, if the voltage drop is not too much, use a low dropout regulator (LDO); otherwise, use a buck converter instead.

The following figure shows the reference design for a +5 V power supply which is regulated with an LDO (MIC29502WU) from Microchip. The typical output volage of the LDO is 3.8 V and the rated current of it is 5.0 A.

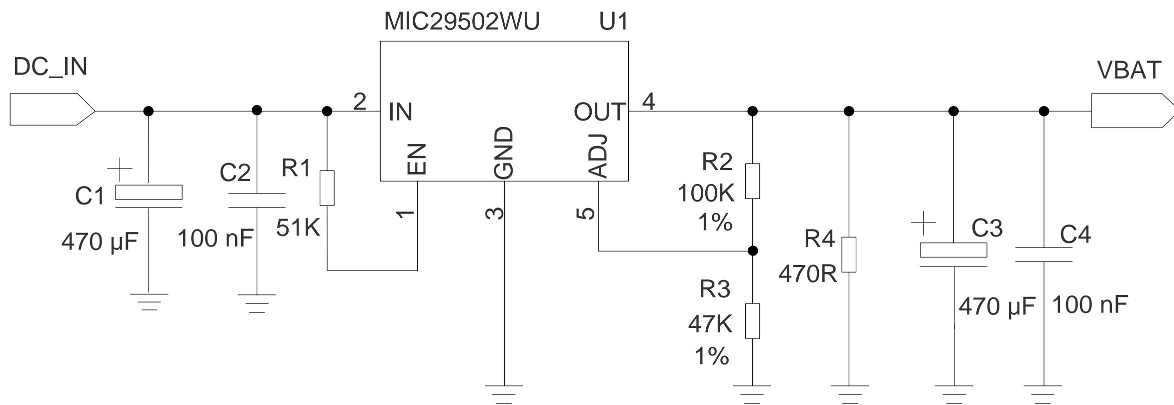

Figure 5: Reference Design for Power Supply

NOTE

If the module happens to get into an abnormal state, it is recommended to switch off and on its power supply to restart it.

3.5. Turn-On and Turn-Off Timing

3.5.1. Turn On Module

The PWRKEY pin is pulled up to 1.8 V internally. Driving it low for at least 1.6 s turns on the module. It is recommended to control the pin with an open drain/collector driver. A simple reference design is shown in the following figure.

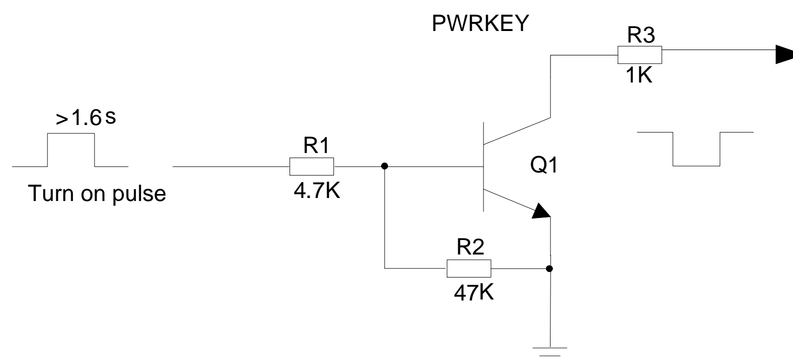

Figure 6: Turn On Module Using Driving Circuit

Another way to control PWRKEY is with a button. A Transient Voltage Suppressor (TVS) should be placed nearby the button for ESD protection. A reference design is shown in the following figure.

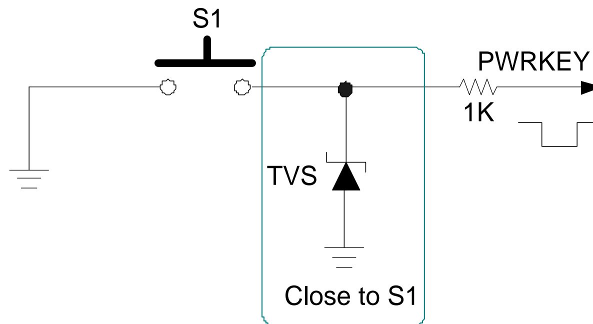

Figure 7: Turn On Module Using Button

The timing of turning on the module is illustrated in the following figure.

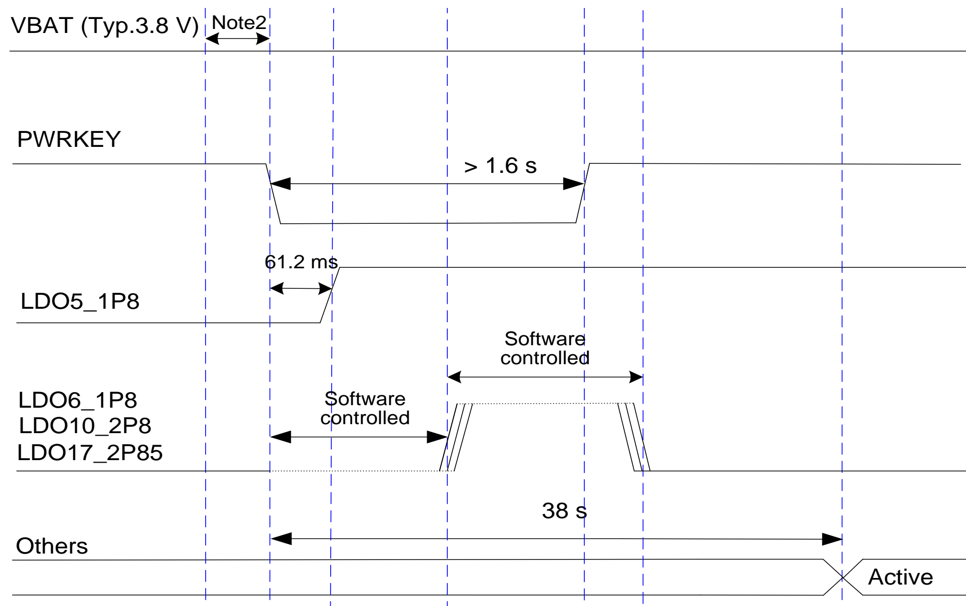

Figure 8: Power-up Timing

NOTE

1. When the module powers on for the first time, the power-up timing might be different from what is shown in the figure above.
2. Ensure that VBAT is stable for at least 30 ms before pulling down the PWRKEY pin.

3.5.2. Turn Off Module

One way to turn off the module is to pull down PWRKEY for at least 1 s, and then choose to turn off

when the prompt window comes up on the display screen connected to an LCM interface of the module.

Another way is to drive PWRKEY low for at least 8 s, which forces the module to shut down. The forced power-down timing is illustrated in the following figure.

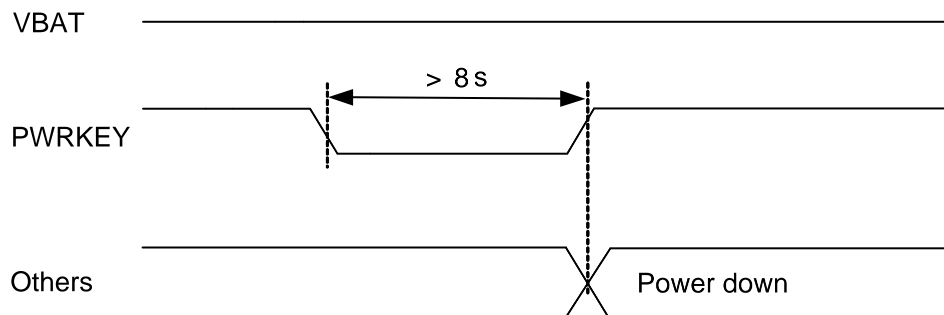

Figure 9: Power-off Timing

3.6. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supplied to the VBAT. The external power source can be a rechargeable battery (such as coil cells) according to application demands. The following figure shows a reference design for powering RTC with an external battery.

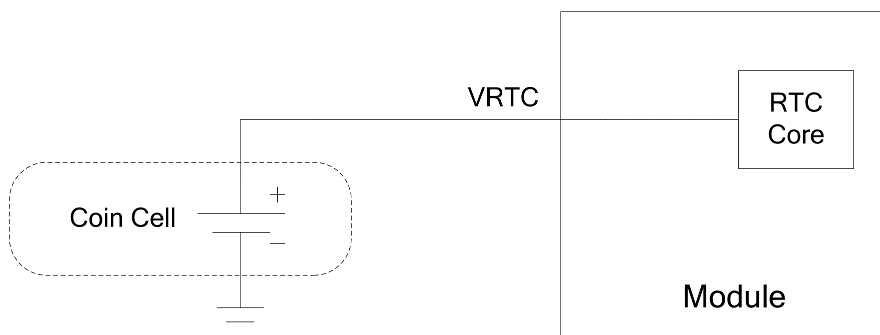

Figure 10: RTC Powered by Coin Cell

If RTC is ineffective, it can be synchronized through network after the module is powered on.

- When VBAT is disconnected, the input voltage range of VRTC is 2.0–3.25 V with the typical value being 3.0 V;
- When powered by VBAT, the RTC has an error rate of 50 ppm, while when powered by VRTC, the RTC deviation is about 200 ppm;
- If a rechargeable battery is used, the ESR of the battery should be less than 2 kΩ, and it is recommended to use the battery MS621FE FL11E from Seiko.

3.7. Power Output

The module can output regulated voltages for peripheral circuits. During application, it is recommended to use parallel capacitors (33 pF and 10 pF) on the circuits to suppress high-frequency noise.

Table 7: Power Description

Pin Name	Default Voltage (V)	Drive Current (mA)	Comment
LDO5_1P8	1.8	20	So long as the module is powered on, the pin retains its power.
LDO6_1P8	1.8	300	
LDO10_2P8	2.8	150	
LDO17_2P85	2.85	300	
LDO2_1P1	1.1	1200	
LDO22_2P8	2.8	150	
LDO23_1P2	1.2	600	
SD_LDO12	1.8/2.95	50	
SD_LDO11	2.95	800	
USIM1_VDD	1.8/2.95	50	
USIM2_VDD	1.8/2.95	50	
VPH_PWR	Equal to VBAT voltage	1000	So long as the module is powered on, the pin retains its power.

3.8. USB Interface

The module is integrated with a USB interface that is USB 3.0/2.0 specifications compliant and supports super speed (5 Gbps) on USB 3.0, high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0, as well as USB OTG function on both USB 2.0 and USB 3.0. This USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 8: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	AI	USB connection detect	Vmax = 10.0 V Vmin = 4.0 V Vnom = 5.0 V
USB_DM	33	AIO	USB differential data (-)	90 Ω differential impedance. USB 2.0 standard compliant.
USB_DP	32	AIO	USB differential data (+)	
USB_ID [2]	30	DO	USB ID detect	High level by default.
GPIO_1	247	DI	USB ID interrupt detection	Pulled up internally. If the default function is not used, it can be configured into a general-purpose GPIO.
USB_SS_RX_P	171	AI	USB 3.0 super-speed receive (+)	90 Ω differential impedance. USB 3.0 standard compliant.
USB_SS_RX_M	172	AI	USB 3.0 super-speed receive (-)	
USB_SS_TX_P	174	AO	USB 3.0 super-speed transmit (+)	
USB_SS_TX_M	175	AO	USB 3.0 super-speed transmit (-)	
USBC_CC2	223	AIO	USB Type-C control configuration channel 2	
USBC_CC1	224	AIO	USB Type-C control configuration channel 1	
USB_SS_SEL	226	DO	USB Type-C switch control	

[2] The module supports USB ID detection for USB Type-C interface through USBC_CC1, USBC_CC2, USB_ID and GPIO_1 pins. When an OTG is connected to the USB Type-C interface, the USBC_CC1 and USBC_CC2 will force the USB_ID to output a low voltage level to pull down GPIO_1, thus making the module enter Host mode. If USB OTG is not used, the USB_ID should be kept open.

In the design of the USB 2.0 interface, it is recommended to connect the module's GPIO_1 directly to the USB_ID of external micro USB interface for USB ID detection. If the external micro USB interface serves as a host, the module's GPIO_1 will be pulled down to force the module into Host mode. The following figure is a reference design for the USB 2.0 interface:

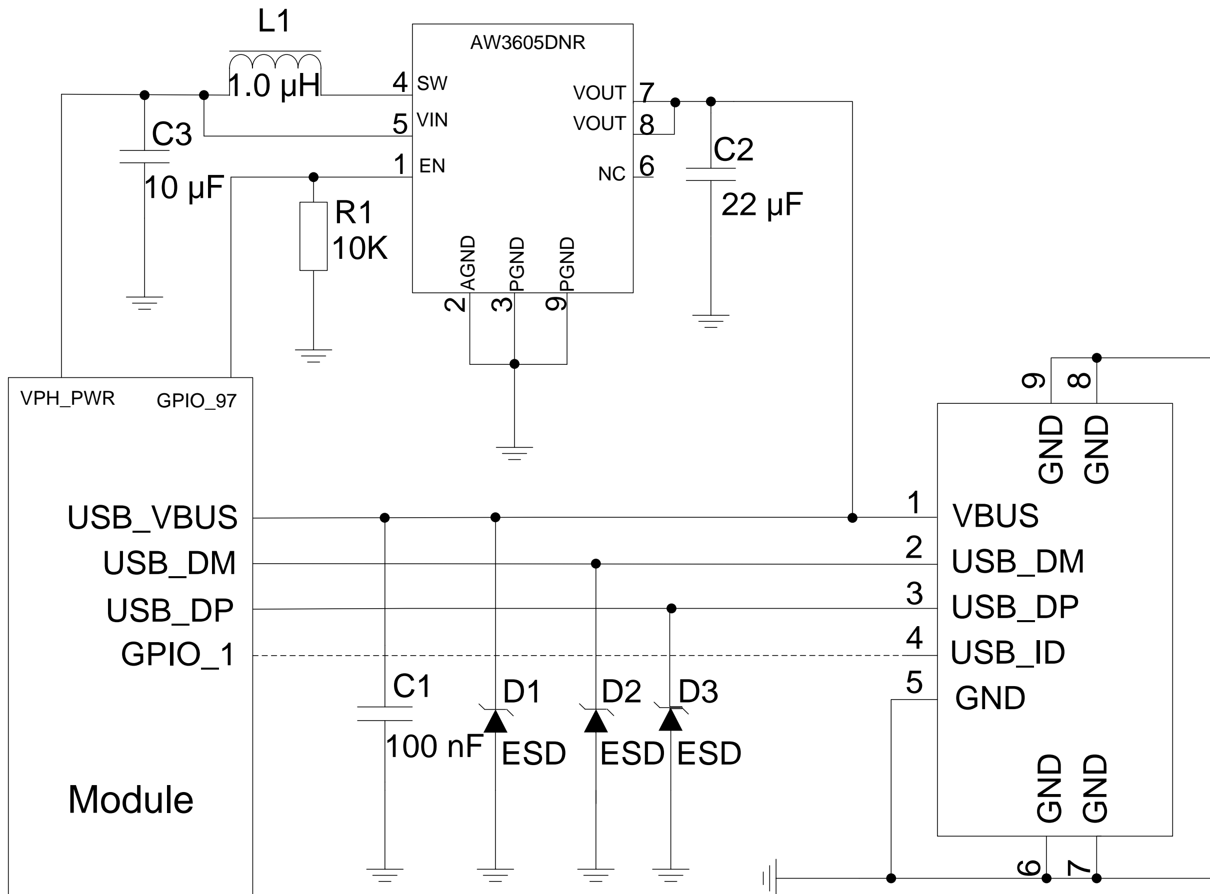

Figure 11: USB 2.0 Interface Reference Design

For the reference design of the USB 3.0 interface, see ***document [2].***

The following is a reference design for the USB Type-C interface:

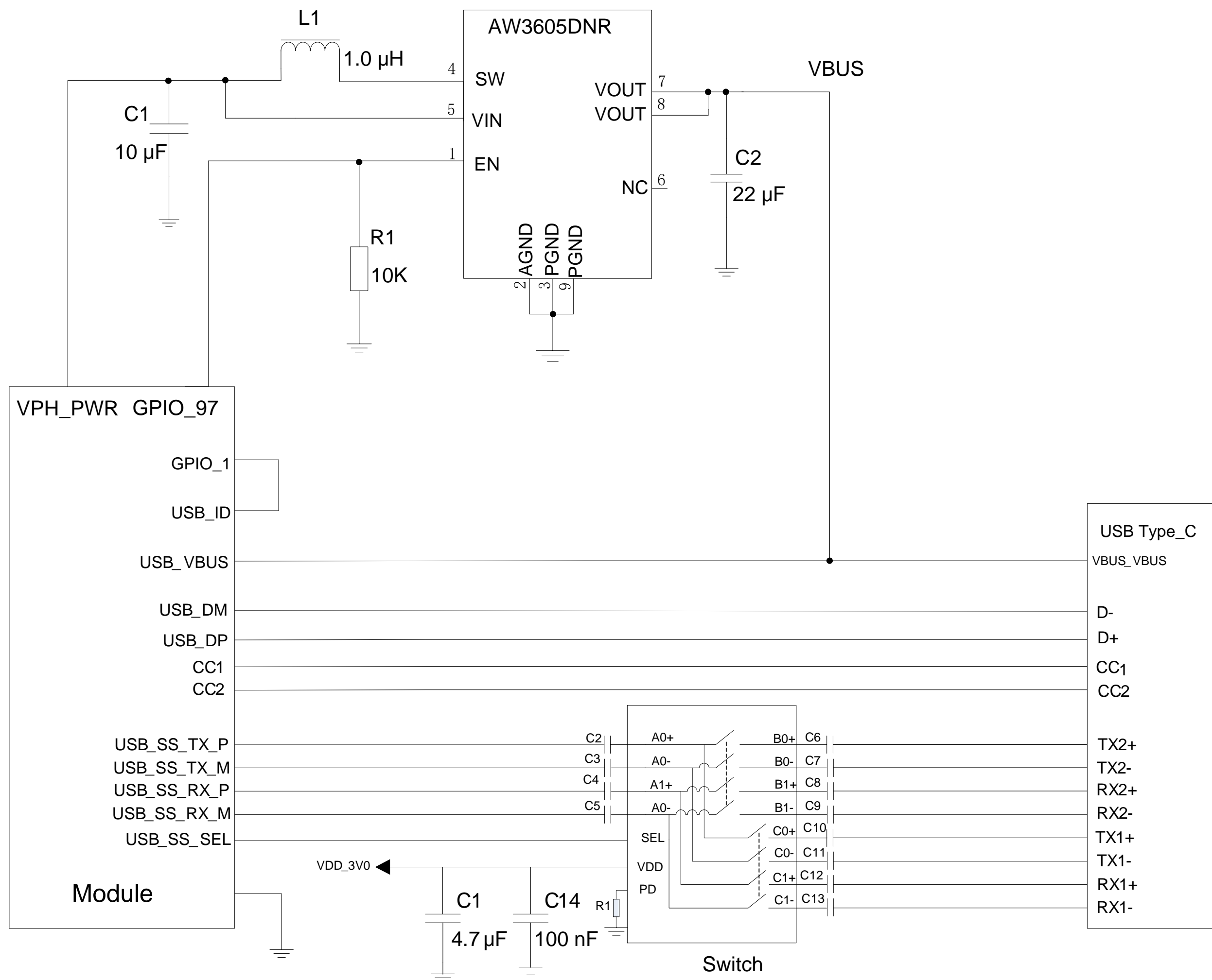

Figure 12: USB Type-C Interface Reference Design

To ensure sound USB performance, please follow these principles in your design:

- Route the USB signal traces as differential pairs with total grounding and keep the impedance of USB differential traces at 90 Ω.
- Pay attention to the influence of junction capacitance of ESD protection devices upon USB data lines. Typically, the capacitance should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.0.
- Avoid routing the USB signal traces under crystals, oscillators, magnetic devices, or RF signal traces. Route the traces in the inner-layer of PCB with ground shielding on not only upper and lower layers but also right and left sides.
- Keep the ESD protection devices as close to the USB connector as possible.
- Ensure the trace length differences between the USB 2.0 DM/DP differential pair and between the USB 3.0 RX/TX differential pairs do not exceed 0.7 mm.

Table 9: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (mm)
33	USB_DM	39.52	-0.45
32	USB_DP	39.07	
171	USB_SS_RX_P	28.55	0.32
172	USB_SS_RX_M	28.23	
174	USB_SS_TX_P	19.58	0.23
175	USB_SS_TX_M	19.35	

3.9. UART Interfaces

The module provides the following three UART interfaces:

- **UART2:** 2-wire UART interface, used for debugging.
- **UART4:** 2-wire UART interface.
- **UART5:** 4-wire UART interface, hardware flow control supported.

Table 10: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART2_TXD	5	DO	UART2 transmit	1.8 V power domain. Keep the unused of these pins open.
UART2_RXD	6	DI	UART2 receive	
UART4_TXD	7	DO	UART4 transmit	
UART4_RXD	8	DI	UART4 receive	
UART5_RXD	198	DI	UART5 receive	
UART5_TXD	199	DO	UART5 transmit	
UART5_CTS	246	DI	UART5 clear to send	
UART5_RTS	245	DO	UART5 request to send	

UART5 is a 4-wire UART interface with 1.8 V power domain. A level translator chip should be used if your application is equipped with a 3.3 V UART interface. The level translator chip TXS0104EPWR provided by Texas Instruments is recommended. The following figure shows a reference design for the level translator chip.

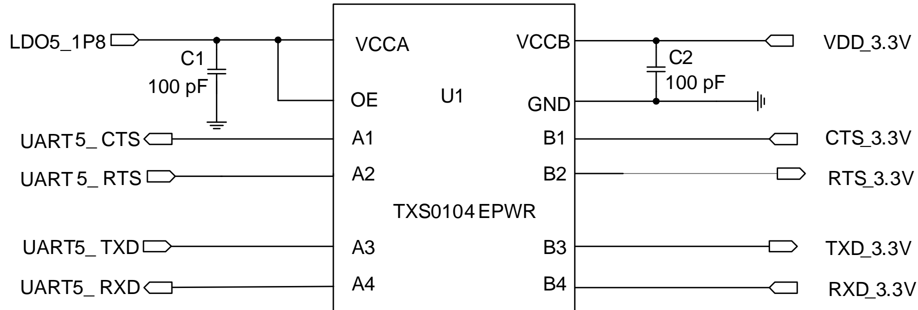

Figure 13: Reference Design of Level Translator Chip (for UART5)

The following figure is an example connection between the module and PC. A voltage level translator and an RS-232 transceiver are recommended to be added between the module and PC, as shown in the figure below:

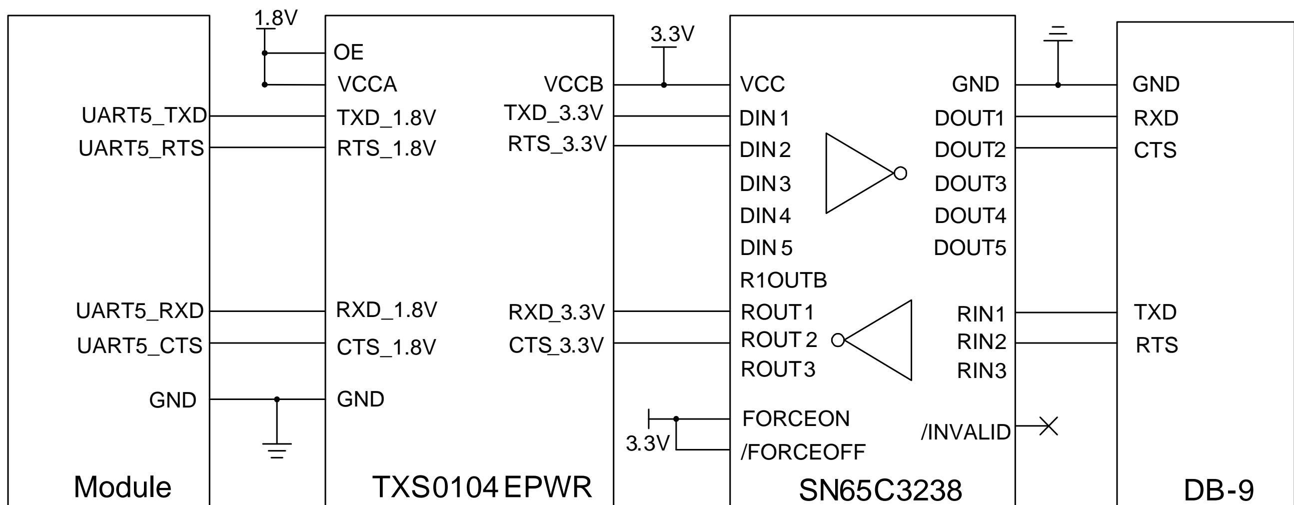

Figure 14: Reference Design of RS-232 Level Matching Circuit (for UART5)

NOTE

The level translation reference designs for UART2 and UART4 are similar with those for UART5.

3.10. (U)SIM Interfaces

The module provides two (U)SIM interfaces which meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Both 1.8 V and 2.95 V (U)SIM cards are supported, and the (U)SIM interfaces are powered via dedicated LDOs in the module.

Table 11: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect	Active low. Require to be externally pulled up to 1.8 V. If unused, keep this pin open. Disabled by default, and can be enabled through software configuration.
USIM1_RST	144	DO	(U)SIM1 card reset	
USIM1_CLK	143	DO	(U)SIM1 card clock	
USIM1_DATA	142	DIO	(U)SIM1 card data	Require to be pulled up to USIM1_VDD with a 10 kΩ resistor.
USIM1_VDD	141	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM2_DET	256	DI	(U)SIM2 card hot-plug detect	Active low. Require to be externally pulled up to 1.8 V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.
USIM2_RST	207	DO	(U)SIM2 card reset	
USIM2_CLK	208	DO	(U)SIM2 card clock	
USIM2_DATA	209	DIO	(U)SIM2 card data	Require to be pulled up to USIM2_VDD with a 10 kΩ resistor.
USIM2_VDD	210	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.

The module supports (U)SIM card hot-plug via the USIM_DET pin, which is disabled by default and can be enabled through software configuration. A reference design for the (U)SIM interfaces connected with

an 8-pin (U)SIM card connector is shown below.

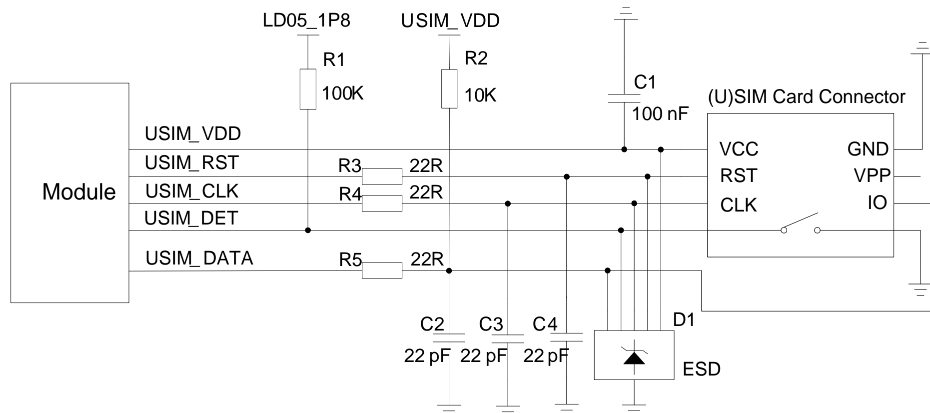

Figure 15: Reference Design for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If there is no need to use USIM_DET, keep it open. The following is a reference design for the (U)SIM interfaces connected with a 6-pin (U)SIM card connector.

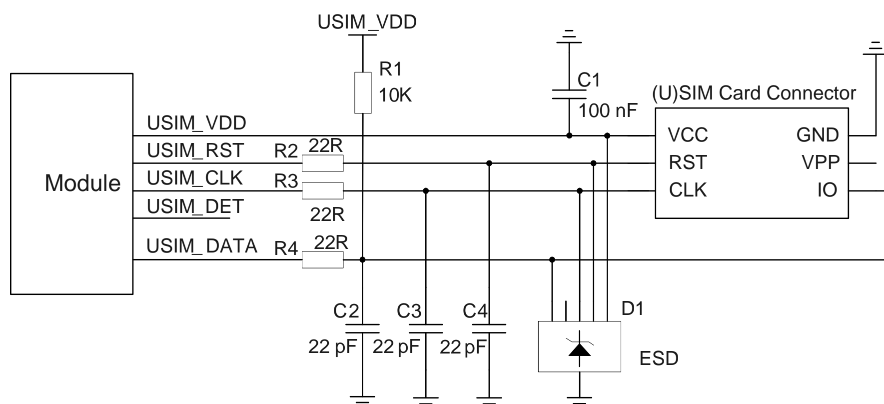

Figure 16: Reference Design for (U)SIM Interface with a 6-pin (U)SIM Card Connector

To ensure good performance and avoid damage of (U)SIM cards, please follow these principles in your design:

- Place the (U)SIM card connector as close to the module as possible. Keep the (U)SIM trace length as less than 200 mm as possible.
- Keep (U)SIM card signal traces away from RF and VBAT traces.
- Reserve a filter capacitor for USIM_VDD, and keep the capacitance of the capacitor within 1 μF. Place the capacitor near to the (U)SIM card.
- To avoid cross-talk between USIM_DATA and USIM_CLK traces, keep them away from each other and shield them with the ground. USIM_RST also needs such ground protection.
- To offer good ESD protection, add a TVS diode array with a parasitic capacitance within 50 pF. The 22 Ω resistors should be added in series between the module and (U)SIM card so as to suppress

EMI spurious transmission and enhance ESD protection. Ensure the ESD device is close to the (U)SIM card connector.

- Add 22 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST signal traces so as to filter RF interference, and place these capacitors as close to the (U)SIM card connector as possible.

3.11. SD Card Interface

The SD card interface of the module complies with SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 12: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_LDO11	63	PO	SD card power supply	Vnom = 2.95 V $I_O$max = 800 mA
SD_LDO12	179	PO	1.8/2.95 V output power for SD card pull-up circuits	1.8/2.95 V output.
SD_CLK	70	DO	SD card clock	Control the characteristic impedance at 50 Ω.
SD_CMD	69	DIO	SD card command	
SD_DATA0	68	DIO	SDIO data bit 0	
SD_DATA1	67	DIO	SDIO data bit 1	
SD_DATA2	66	DIO	SDIO data bit 2	
SD_DATA3	65	DIO	SDIO data bit 3	
SD_DET	64	DI	SD card hot-plug detect	Active low.

A reference design for SD card interface is shown as below.

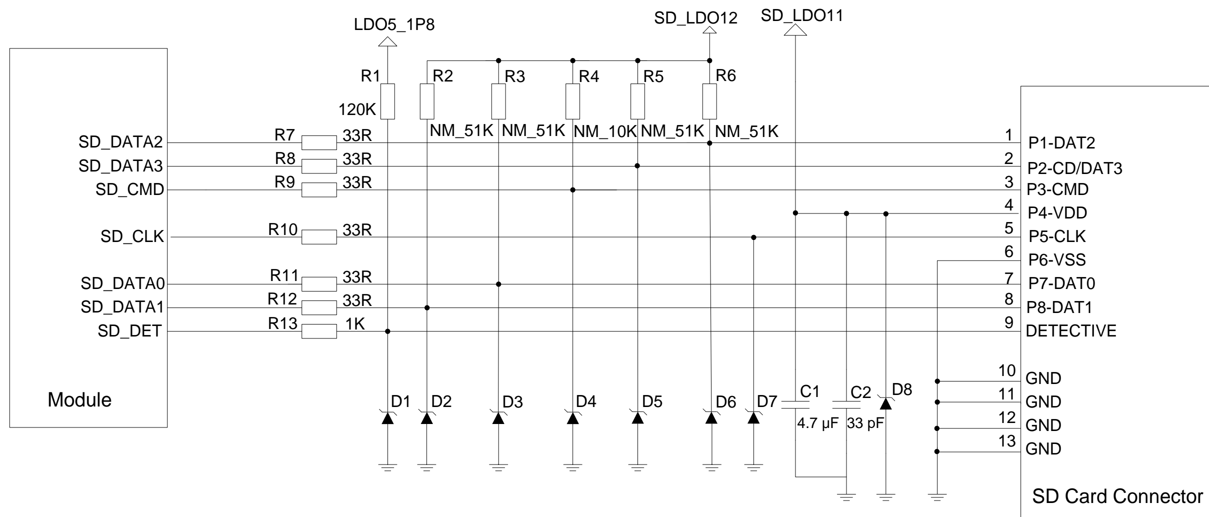

Figure 17: Reference Design for SD Card Interface

SD_LDO11 is a peripheral driver power supply for SD card. The maximum drive current of the pin is approximately 800 mA. Because of the high drive current, it is recommended to keep the trace width at 0.5 mm or above. To ensure the stability of supply power, a 4.7 μF and a 33 pF capacitor should be added in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA0, SD_DATA1, SD_DATA2, and SD_DATA3 traces are all high speed signal traces. In PCB design, control the characteristic impedance of these traces at 50 Ω ±10 %, and avoid crossing them with other traces. It is recommended to route the traces on the inner layer of PCB and keep their lengths the same. The CLK trace should be encircled by ground traces individually.

Please follow these guidelines in your design:

- SD_DATA0, SD_DATA1, SD_DATA2, and SD_DATA3 should be encircled by ground traces.
- The trace length difference between CLK and other signal traces should not exceed 1 mm.
- Keep the maximum bus capacitance of SD card traces within 15 pF.

Table 13: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)
70	SD_CLK	32.11
69	SD_CMD	32.11
68	SD_DATA0	32.11

67	SD_DATA1	32.11
66	SD_DATA2	32.11
65	SD_DATA3	32.11

3.12. GPIO Interfaces

The module has multiple GPIO interfaces with power domain of 1.8 V. The pin definition is listed below.

Table 14: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	Description	Comment
GPIO_0	248	General-purpose input/output	
GPIO_1	247	General-purpose input/output	Wakeup [3]
GPIO_2	201	General-purpose input/output	
GPIO_3	200	General-purpose input/output	
GPIO_33	238	General-purpose input/output	
GPIO_36	237	General-purpose input/output	Wakeup
GPIO_42	252	General-purpose input/output	Wakeup
GPIO_43	253	General-purpose input/output	Wakeup
GPIO_44	254	General-purpose input/output	Wakeup
GPIO_45	255	General-purpose input/output	Wakeup
GPIO_66	234	General-purpose input/output	
GPIO_89	232	General-purpose input/output	
GPIO_90	231	General-purpose input/output	Wakeup
GPIO_96	230	General-purpose input/output	
GPIO_97	229	General-purpose input/output	Wakeup
GPIO_98	177	General-purpose input/output	

3 Wakeup: interrupt pins that can wake up the system.

GPIO_99	178	General-purpose input/output

NOTE

For more details about GPIO configuration, see ***document [3]***.

3.13. I2C Interfaces

Every model of the series provides five groups of I2C interfaces. As an open-drain output, each I2C interface should be pulled up to 1.8 V. The SENSOR_I2C interface supports only sensors of the ADSP architecture. CAM/DCAM_I2C bus is controlled by Linux Kernel code and can be connected to video output related devices.

Table 15: Pin Definition of I2C Interfaces

Pin Name	Pin No	I/O	Description	Comment
TP0_I2C_SCL	140	OD	TP0 I2C clock	Used for TP0
TP0_I2C_SDA	206	OD	TP0 I2C data	
TP1_I2C_SCL	205	OD	TP1 I2C clock	Used for TP1
TP1_I2C_SDA	204	OD	TP1 I2C data	
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras	Used for front and rear cameras
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras	
DCAM_I2C_SCL	196	OD	I2C clock of depth camera	Used for the depth camera
DCAM_I2C_SDA	197	OD	I2C data of depth camera	
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	Used for external sensors
SENSOR_I2C_SDA	132	OD	I2C data for external sensor	

3.14. SPI Interfaces

The module provides two SPI interfaces which only support Master mode. The two interfaces are typically applied for fingerprint identification.

Table 16: Pin Definition of SPI Interfaces

Pin Name	Pin No	I/O	Description	Comment
SPI_CS	58	DO	SPI chip select	
SPI_CLK	59	DO	SPI clock	
SPI_MOSI	60	DO	SPI master-out slave-in	
SPI_MISO	61	DI	SPI master-in salve-out	
FP_SPI_CS	203	DO	FP SPI chip select	
FP_SPI_CLK	250	DO	FP SPI clock	
FP_SPI_MOSI	249	DO	FP SPI master-out slave-in	
FP_SPI_MISO	251	DI	FP SPI master-in salve-out	

3.15. ADC Interface

The module provides one analog-to-digital converter (ADC) interfaces, and the pin definition is shown below. The resolution of the ADC is up to 15 bits.

Table 17: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
PMU_MPP2	151	AI	General-purpose ADC interface	Maximum input voltage: 1.7 V.

3.16. LCM Interfaces

The module provides two LCM interfaces, supports dual LCDs and features WUXGA display with a resolution up to 1200 (RGB) × 1920. These interfaces support high-speed differential data transmission along up to 8 lanes.

Table 18: Pin Definition of LCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LDO6_1P8	10	PO	1.8 V output	Power supply for VDD of sensor, camera, LCD and I2C's pull-up circuits.
LDO17_2P85	12	PO	2.85 V output	Power supply for VDD of LCD and camera.
PMU_MPP4	152	DO	PWM output	
GPIO_33	238	DIO	General-purpose clock signal output for backlight driver	If its default function is not used, it can be configured into a general-purpose GPIO.
LCD0_RST	127	DO	LCD0 reset	Active low.
LCD0_TE	126	DI	LCD0 tearing effect	
LCD1_RST	113	DO	LCD1 reset	Active low.
LCD1_TE	114	DI	LCD1 tearing effect	
DSI0_CLK_N	116	AO	LCD0 MIPI clock (-)	
DSI0_CLK_P	115	AO	LCD0 MIPI clock (+)	
DSI0_LN0_N	118	AO	LCD0 MIPI lane 0 data (-)	
DSI0_LN0_P	117	AO	LCD0 MIPI lane 0 data (+)	
DSI0_LN1_N	120	AO	LCD0 MIPI lane 1 data (-)	
DSI0_LN1_P	119	AO	LCD0 MIPI lane 1 data (+)	
DSI0_LN2_N	122	AO	LCD0 MIPI lane 2 data (-)	
DSI0_LN2_P	121	AO	LCD0 MIPI lane 2 data (+)	

DSI0_LN3_N	124	AO	LCD0 MIPI lane 3 data (-)
DSI0_LN3_P	123	AO	LCD0 MIPI lane 3 data (+)
DSI1_CLK_N	103	AO	LCD1 MIPI clock (-)
DSI1_CLK_P	102	AO	LCD1 MIPI clock (+)
DSI1_LN0_N	105	AO	LCD1 MIPI lane 0 data (-)
DSI1_LN0_P	104	AO	LCD1 MIPI lane 0 data (+)
DSI1_LN1_N	107	AO	LCD1 MIPI lane 1 data (-)
DSI1_LN1_P	106	AO	LCD1 MIPI lane 1 data (+)
DSI1_LN2_N	109	AO	LCD1 MIPI lane 2 data (-)
DSI1_LN2_P	108	AO	LCD1 MIPI lane 2 data (+)
DSI1_LN3_N	111	AO	LCD1 MIPI lane 3 data (-)
DSI1_LN3_P	110	AO	LCD1 MIPI lane 3 data (+)

The following figures are reference designs for LCM interfaces.

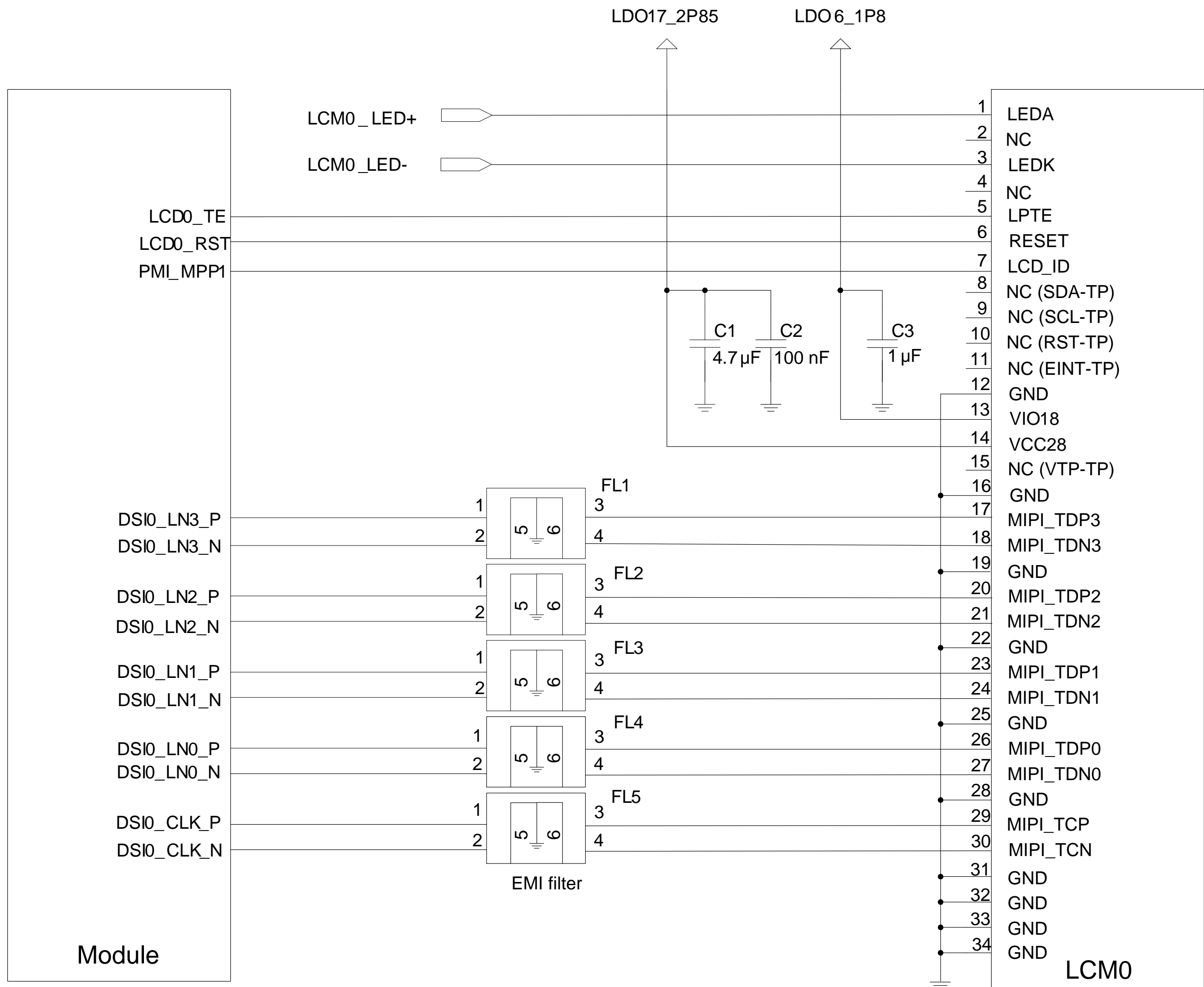

Figure 18: Reference Design for LCM0 Interface

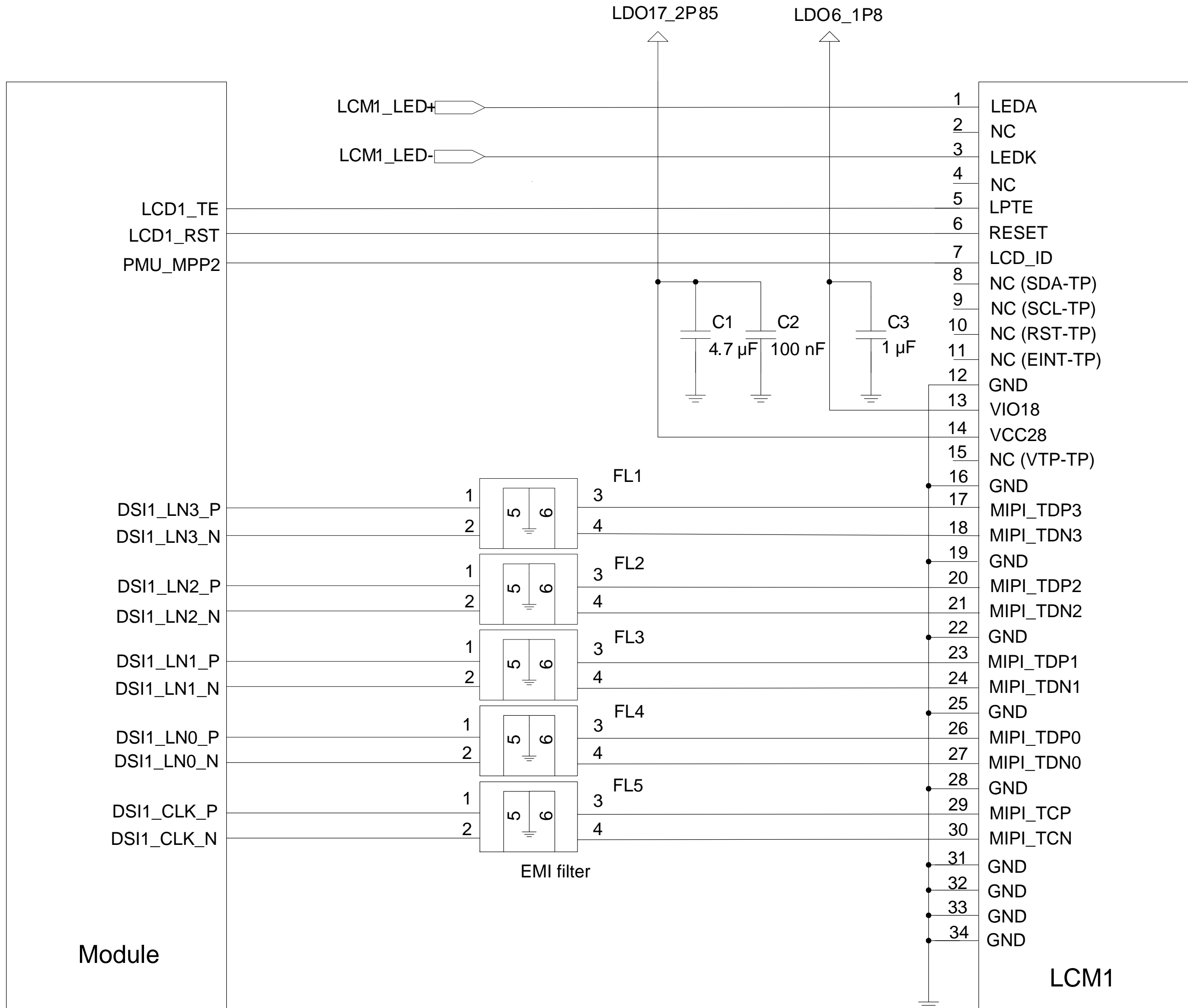

Figure 19: Reference Design for LCM1 Interface

For high-speed MIPI_CSI signals, common-mode filters should be added in series near the LCM connector to improve protection against electromagnetic radiation interference.

When compatible design with other displays is required, connect the LCD_ID pin of LCM to the module's ADC pin, and ensure the output voltage of LCD_ID never exceeds the voltage range of ADC.

Use an external backlight driving circuit for LCM according to the practical demand. The following figure is a reference design for the driving circuit with PMU_MPP4 and GPIO_33 used to adjust the backlight brightness.

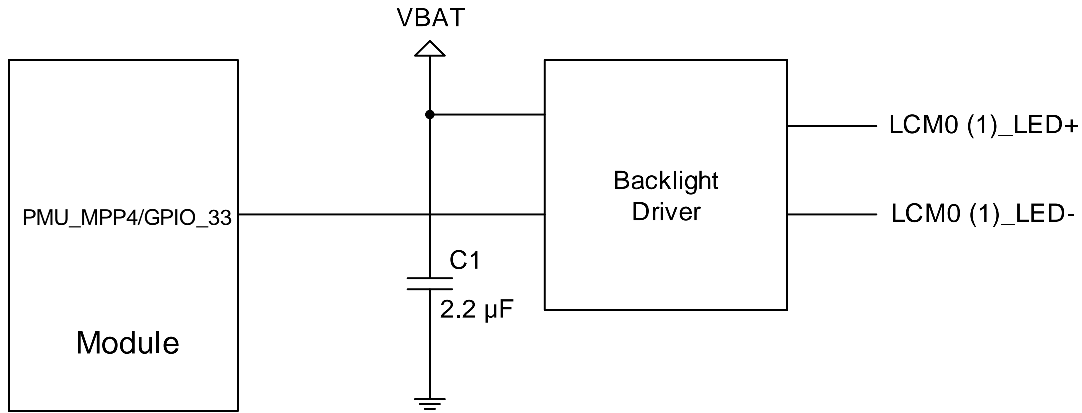

Figure 20: Reference Design for LCM External Backlight Driver

3.17. Touch Panel Interfaces

The module provides two touch panel interfaces for connection with touch panel, and also provides the corresponding power pins and interrupt pins. The pin definition of the touch panel interfaces is illustrated below.

Table 19: Pin Definition of Touch Panel Interfaces

Pin Name	Pin No	I/O	Description	Comment
LDO10_2P8	11	PO	2.8 V output power for VDD of Sensor and TP	Vnom = 2.8 V $I_O$max = 150 mA
LDO6_1P8	10	PO	1.8 V output power for VDD of Sensor, Camera, LCD and I2C's pull-up circuits	Vnom = 1.8 V $I_O$max = 300 mA
TP0_INT	139	DI	TP0 Interrupt	1.8 V power domain.
TP0_RST	138	DO	TP0 reset	1.8 V power domain. Active low.
TP0_I2C_SCL	140	OD	TP0 I2C clock	1.8 V power domain.
TP0_I2C_SDA	206	OD	TP0 I2C data	1.8 V power domain.
TP1_INT	137	DI	TP1 Interrupt	1.8 V power domain.
TP1_RST	136	DO	TP1 reset	Active low.
TP1_I2C_SCL	205	OD	TP1 I2C clock	1.8 V power domain.

TP1_I2C_SDA	204	OD	TP1 I2C data	1.8 V power domain.

A reference design for touch panel interfaces is shown below.

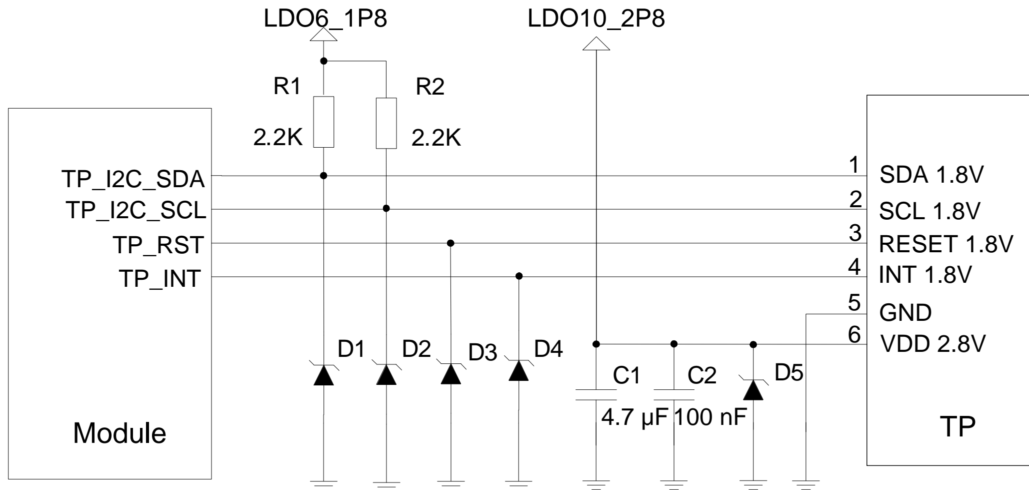

Figure 21: Reference Design for Touch Panel Interface

NOTE

By default, TP is powered by LDO10_2P8, which outputs a current of 150 mA. When dual-TP or other applications need to be supported, it is recommended to use an external LDO instead.

3.18. Camera Interfaces

Based on standard MIPI_CSI input interface, The module supports 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane). The video and photo quality is determined by various factors such as the quality of camera sensor and camera lens.

Table 20: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LDO2_1P1	13	PO	1.1 V output power for DVDD of rear Camera	Vnom = 1.1 V $I_O$max = 1200 mA
LDO6_1P8	10	PO	1.8 V output power for VDD of Sensor, Camera, LCD and I2C's pull-up circuits	Vnom = 1.8 V $I_O$max = 300 mA

LDO17_2P85	12	PO	2.85 V output power for VDD of LCD and Camera	Vnom = 2.85 V $I_O$max = 300 mA
LDO22_2P8	14	PO	2.8 V output power for AVDD of Camera	Vnom = 2.8 V $I_O$max = 150 mA
LDO23_1P2	15	PO	1.2 V output power for DVDD of front Camera.	Vnom = 1.2 V $I_O$max = 600 mA
CSI0_CLK_N	89	AI	MIPI clock of rear camera (-)	
CSI0_CLK_P	88	AI	MIPI clock of rear camera (+)	
CSI0_LN0_N	91	AI	MIPI lane 0 data of rear camera (-)	
CSI0_LN0_P	90	AI	MIPI lane 0 data of rear camera (+)	
CSI0_LN1_N	93	AI	MIPI lane 1 data of rear camera (-)	
CSI0_LN1_P	92	AI	MIPI lane 1 data of rear camera (+)	
CSI0_LN2_N	95	AI	MIPI lane 2 data of rear camera (-)	
CSI0_LN2_P	94	AI	MIPI lane 2 data of rear camera (+)	
CSI0_LN3_N	97	AI	MIPI lane 3 data of rear camera (-)	
CSI0_LN3_P	96	AI	MIPI lane 3 data of rear camera (+)	
CSI1_CLK_N	184	AI	MIPI clock signal of depth camera (-)	
CSI1_CLK_P	183	AI	MIPI clock signal of depth camera (+)	
CSI1_LN0_N	186	AI	MIPI lane 0 data of depth camera (-)	
CSI1_LN0_P	185	AI	MIPI lane 0 data of depth camera (+)	
CSI1_LN1_N	188	AI	MIPI lane 1 data of depth camera (-)	
CSI1_LN1_P	187	AI	MIPI lane 1 data of depth camera (+)	
CSI1_LN2_N	190	AI	MIPI lane 2 data of depth camera (-)	
CSI1_LN2_P	189	AI	MIPI lane 2 data of depth camera (+)	
CSI1_LN3_N	192	AI	MIPI lane 3 data of depth camera (-)	
CSI1_LN3_P	191	AI	MIPI lane 3 data of depth camera (+)	
CSI2_CLK_N	78	AI	MIPI clock of front camera (-)	

CSI2_CLK_P	77	AI	MIPI clock of front camera (+)	
CSI2_LN0_N	80	AI	MIPI lane 0 data of front camera (-)	
CSI2_LN0_P	79	AI	MIPI lane 0 data of front camera (+)	
CSI2_LN1_N	82	AI	MIPI lane 1 data of front camera (-)	
CSI2_LN1_P	81	AI	MIPI lane 1 data of front camera (+)	
CSI2_LN2_N	84	AI	MIPI lane 2 data of front camera (-)	
CSI2_LN2_P	83	AI	MIPI lane 2 data of front camera (+)	
CSI2_LN3_N	86	AI	MIPI lane 3 data of front camera (-)	
CSI2_LN3_P	85	AI	MIPI lane 3 data of front camera (+)	
MCAM_MCLK	99	DO	Master clock of rear camera	1.8 V power domain.
SCAM_MCLK	100	DO	Master clock of front camera	1.8 V power domain.
MCAM_RST	74	DO	Reset of rear camera	1.8 V power domain.
MCAM_PWDN	73	DO	Power down of rear camera	1.8 V power domain.
SCAM_RST	72	DO	Reset of front camera	1.8 V power domain.
SCAM_PWDN	71	DO	Power down of front camera	1.8 V power domain.
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras	1.8 V power domain.
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras	1.8 V power domain.
DCAM_MCLK	194	DO	Master clock of depth camera	1.8 V power domain.
CAM4_MCLK	236	DO	Master clock of fourth camera	1.8 V power domain.
DCAM_RST	180	DO	Reset of depth camera	1.8 V power domain.
DCAM_PWDN	181	DO	Power down of depth camera	1.8 V power domain.
DCAM_I2C_SDA	197	OD	I2C data of depth camera	1.8 V power domain.
DCAM_I2C_SCL	196	OD	I2C clock of depth camera	1.8 V power domain.

The following is a reference design for dual camera application.

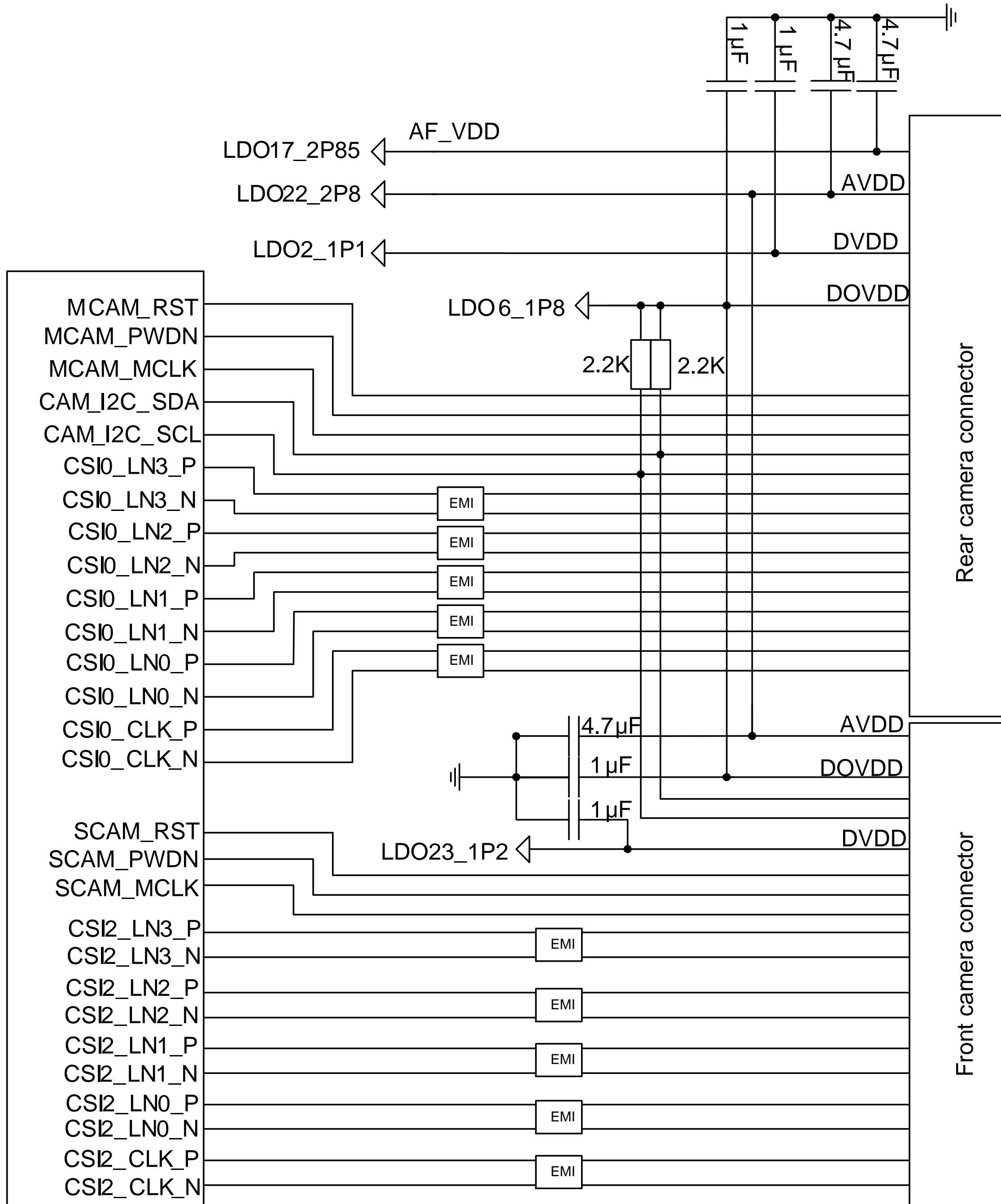

Figure 22: Reference Design for Dual Camera Application

The following is a reference design for triple camera application.

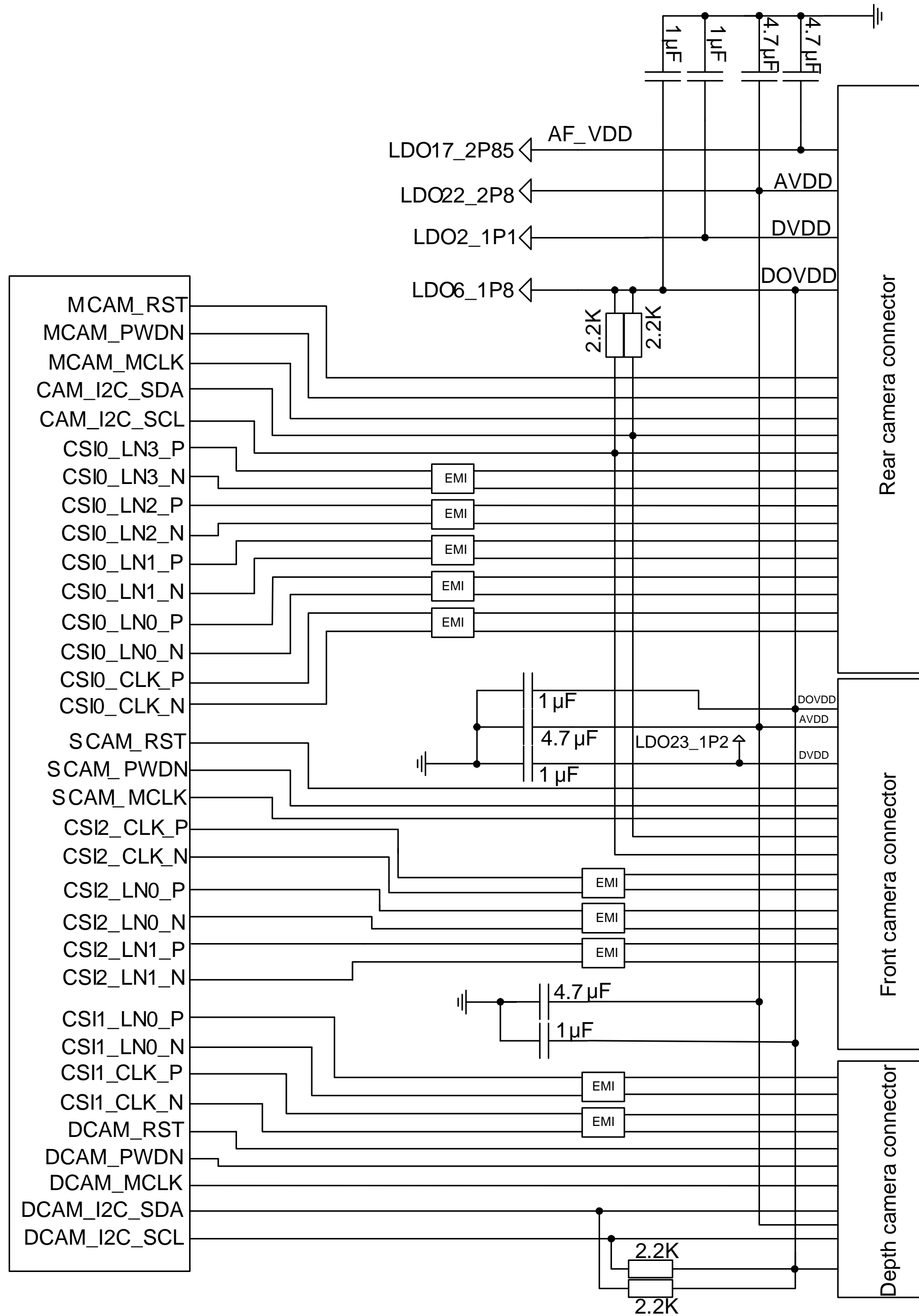

Figure 23: Reference Design for Triple Camera Application

3.18.1. Design Considerations

- Pay attention to the pin definitions of LCM and camera connectors to ensure the module and the connectors are connected correctly.
- MIPI is a high-speed signal line whose data rate reaches 2.1 Gbps. The differential impedance should be kept at 100 Ω, and the trace be routed on the inner layer of PCB and not crossed with other traces. For the same group of DSI or CSI signals, the length of all MIPI traces should be kept the same. In order to avoid crosstalk, keep the intra-lane spacing as wide as the MIPI trace and the inter-lane spacing two times the MIPI trace width. Avoid any cut or hole on the GND reference plane under MIPI signal traces.
- It is recommended to select a low capacitance TVS for ESD protection and the recommended parasitic capacitance is below 1 pF.
- Route MIPI traces according to the following rules:

  a) The total trace length should not exceed 305 mm;
  b) Keep the differential impedance at 100 Ω ±10 %;
  c) Control the intra-lane length difference within 0.67 mm;
  d) Control the inter-lane length difference within 1.3 mm.

Table 21: MIPI Trace Length Inside the Module

Pin Name	Pin No.	Length (mm)	Length Difference (mm)
DSI0_CLK_N	116	20.82	-0.45
DSI0_CLK_P	115	20.37	
DSI0_LN0_N	118	24.84	0
DSI0_LN0_P	117	24.84	
DSI0_LN1_N	120	24.85	-0.03
DSI0_LN1_P	119	24.82	
DSI0_LN2_N	122	25.94	0.24
DSI0_LN2_P	121	26.18	
DSI0_LN3_N	124	29.31	0.2
DSI0_LN3_P	123	29.51	
DSI1_CLK_N	103	9.52	-0.05
DSI1_CLK_P	102	9.47	

DSI1_LN0_N	105	10.27	-0.11
DSI1_LN0_P	104	10.16	
DSI1_LN1_N	107	11.75	-0.17
DSI1_LN1_P	106	11.58	
DSI1_LN2_N	109	14.86	-0.36
DSI1_LN2_P	108	14.5	
DSI1_LN3_N	111	15.73	0.15
DSI1_LN3_P	110	15.88	
CSI0_CLK_N	89	16.54	0.03
CSI0_CLK_P	88	16.57	
CSI0_LN0_N	91	17.47	-0.07
CSI0_LN0_P	90	17.4	
CSI0_LN1_N	93	12.13	-0.05
CSI0_LN1_P	92	12.08	
CSI0_LN2_N	95	9.56	0.14
CSI0_LN2_P	94	9.7	
CSI0_LN3_N	97	8.73	0.13
CSI0_LN3_P	96	8.86	
CSI1_CLK_N	184	20.32	-0.23
CSI1_CLK_P	183	20.09	
CSI1_LN0_N	186	12.09	0.57
CSI1_LN0_P	185	12.66	
CSI1_LN1_N	188	11.33	0.37
CSI1_LN1_P	187	11.70	
CSI1_LN2_N	190	5.86	0.19
CSI1_LN2_P	189	6.05	

CSI1_LN3_N	192	10.49	-0.43
CSI1_LN3_P	191	10.06	
CSI2_CLK_N	78	22.00	0.17
CSI2_CLK_P	77	22.17	
CSI2_LN0_N	80	22.07	-0.07
CSI2_LN0_P	79	22.00	
CSI2_LN1_N	82	22.54	-0.49
CSI2_LN1_P	81	22.05	
CSI2_LN2_N	84	22.03	-0.11
CSI2_LN2_P	83	21.92	
CSI2_LN3_N	86	21.90	0.59
CSI2_LN3_P	85	22.49	

3.19. Sensor Interfaces

The module communicates with sensors via the I2C interface, which supports the communication with various sensors such as acceleration sensors, gyroscopic sensors, compasses, optical sensors and temperature sensors.

Table 22: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	Dedicated for external sensors. Cannot be used for other devices such as touch panel, NFC and keypad.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor	

3.20. Audio Interfaces

The module provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 23: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	44	AI	Microphone input for channel 1 (+)	
MIC1_N	45	AI	Microphone input for channel 1 (-)	
MIC_GND	168		Microphone reference ground	If unused, connect this pin to the ground.
MIC2_P	46	AI	Microphone input for headset (+)	
MIC3_P	169	AI	Microphone input for channel 2 (+)	
MIC_BIAS	167	PO	Bias voltage output for microphone	
EAR_P	53	AO	Earpiece output (+)	
EAR_N	52	AO	Earpiece output (-)	
SPK_P	55	AO	Speaker output (+)	
SPK_N	54	AO	Speaker output (-)	
HPH_R	51	AO	Headphone right channel output	
HPH_REF	50	AI	Headphone reference ground	It should be connected to the main GND.
HPH_L	49	AO	Headphone left channel output	
HS_DET	48	AI	Headset hot-plug detect	High level by default.

- The module offers three audio input channels, including one differential input pair and two single-ended channels. The three sets of MICs are integrated with internal bias voltage.
- The output voltage range of MIC_BIAS can be set at between 1.6 V and 2.85 V, and the maximum output current is 3 mA.
- The earpiece interface is a differential output pair.
- The loudspeaker interface is a differential output pair as well. This output channel is available with a Class-D amplifier whose maximum output power is 1.5 W when the load is 8 Ω.
- The headphone interface features stereo audio output via left and right channels, as well as the

function of headphone insertion detect.

3.20.1. Reference Design for Microphone Interfaces

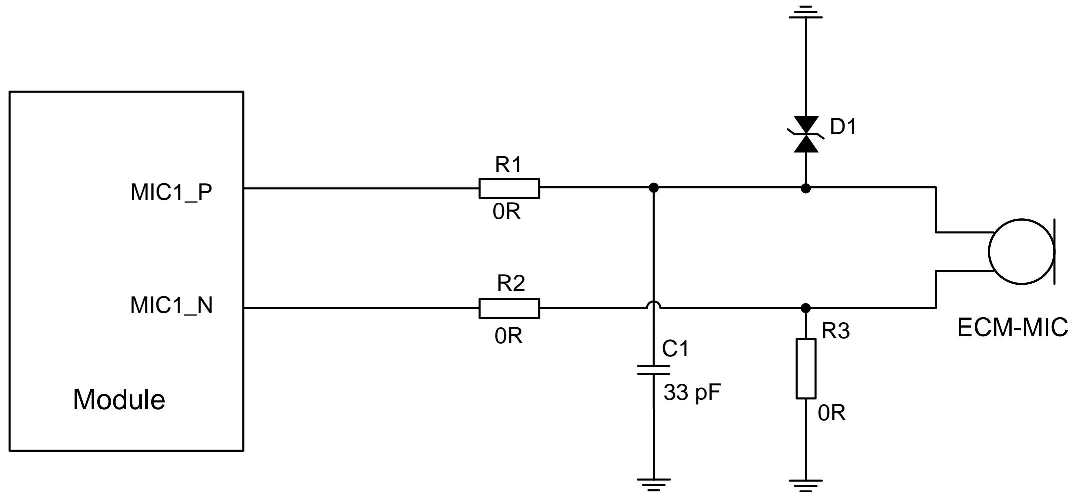

Figure 24: Reference Design for Analog ECM-type Microphone

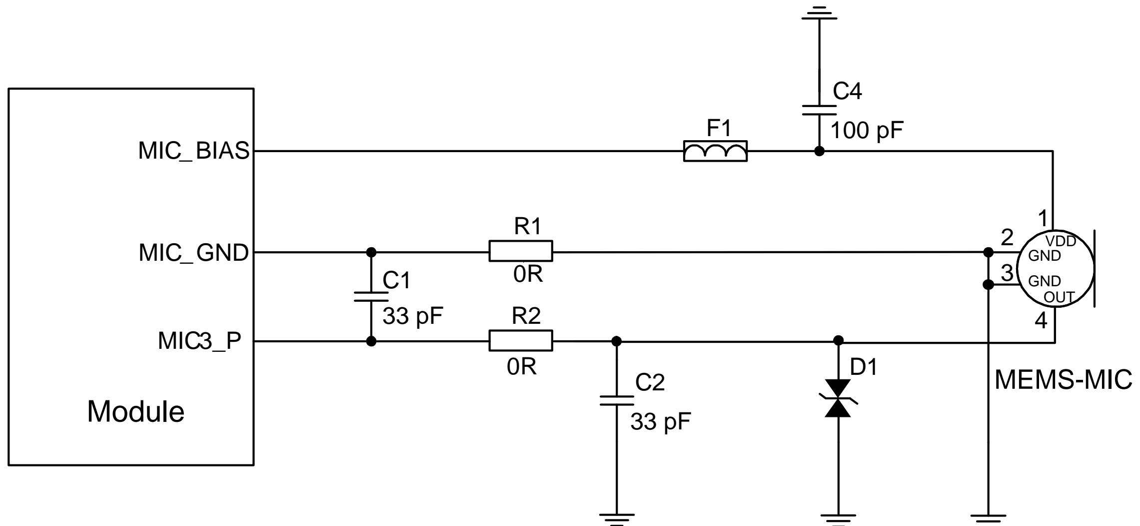

Figure 25: Reference Design for MEMS-type Microphone

3.20.2. Reference Design for Earpiece Interface

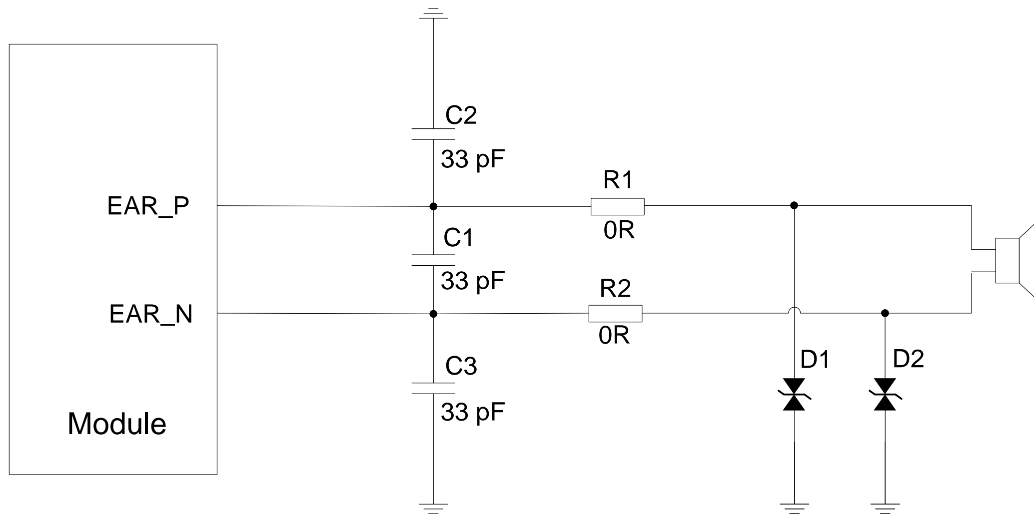

Figure 26: Reference Design for Earpiece Interface

3.20.3. Reference Design for Headphone Interface

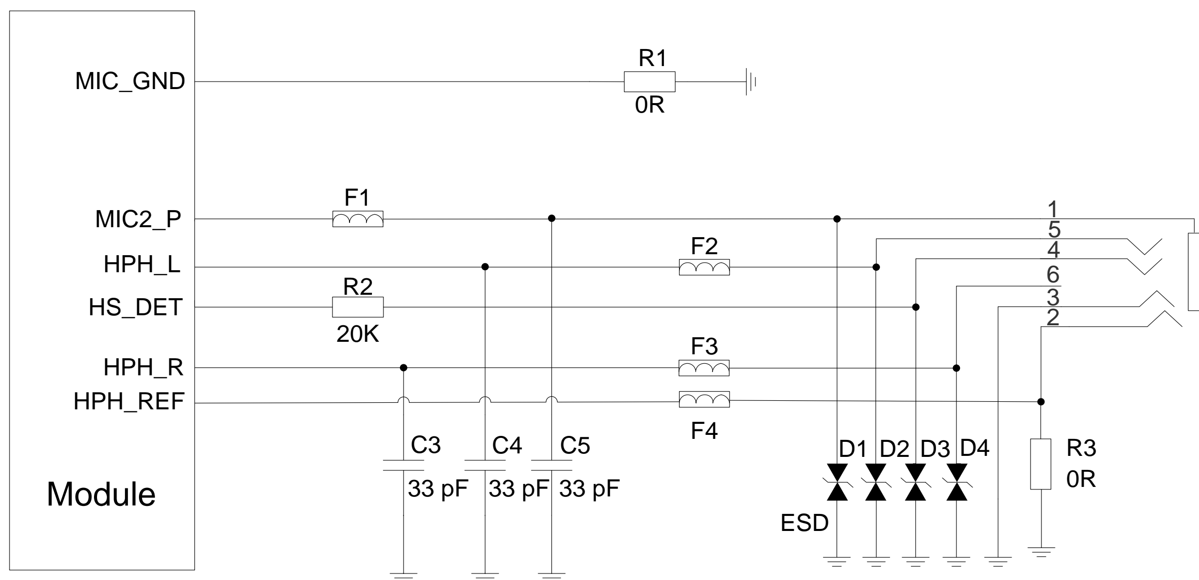

Figure 27: Reference Design for Headphone Interface with Normally Open Jack

3.20.4. Reference Design for Loudspeaker Interface

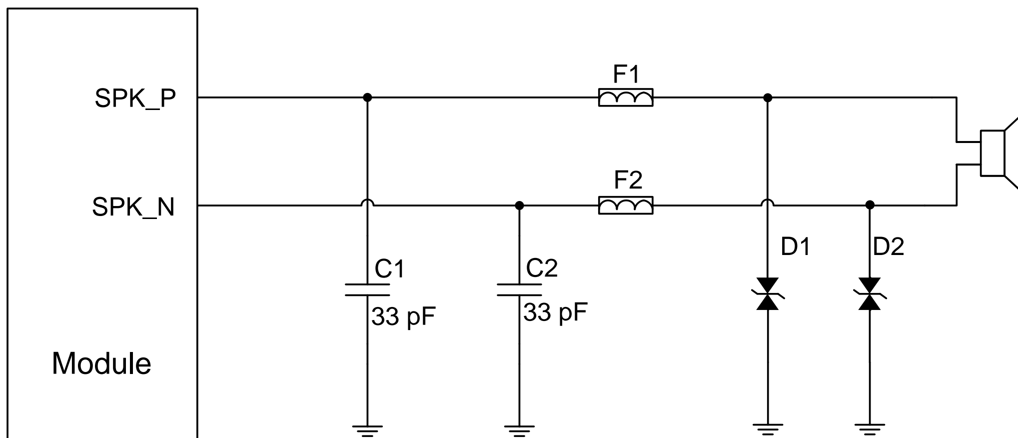

Figure 28: Reference Design for Loudspeaker Interface

3.20.5. Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, and thereby reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Note that the self-resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, it is advisable to choose the most suitable capacitor for filtering out high-frequency noises after consulting your capacitor supplier.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor should be selected based on test results. Sometimes, even no RF filtering capacitor is required.

To decrease radio or other signal interference, RF antennas and power traces should be placed away from audio interfaces and audio traces. Besides, power traces cannot be in parallel with the audio traces.

The differential audio traces must be kept at the same length.

3.21. Emergency Download Interface

USB_BOOT is used to force USB booting. Pulling it up to LDO5_1P8 before power-up will force the module into download mode. This is a solution when there are failures such as an abnormal startup or operation. For convenient firmware upgrade and debugging in the future, it is recommended to reserve the reference design shown below.

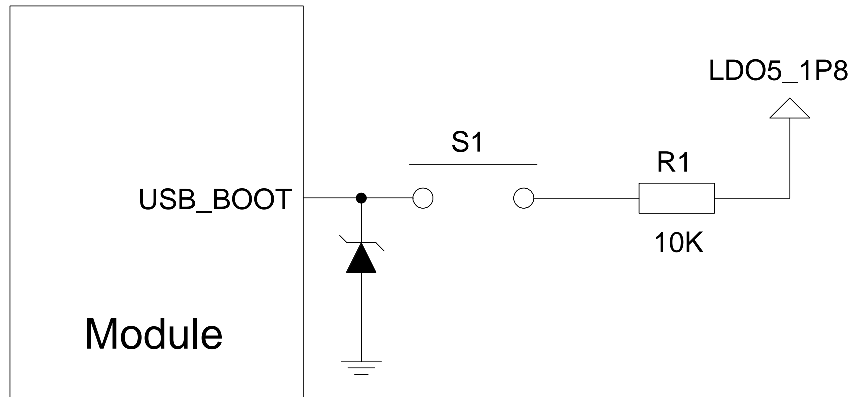

Figure 29: Reference Design for USB_BOOT

4 Wi-Fi and Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The interface impedance is 50 Ω. External antennas such as the PCB antenna, the sucker antenna, and the ceramic antenna can be connected to the module via the interface to provide Wi-Fi and Bluetooth functions.

4.1. Wi-Fi Function Overview

The module supports 2.4 GHz and 5 GHz dual-band WLAN wireless communications based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is 433 Mbps.

The features available are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of the module.

Table 24: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	16 dBm ±2.5 dB
	802.11b	11 Mbps	16 dBm ±2.5 dB
	802.11g	6 Mbps	16 dBm ±2.5 dB

	802.11g	54 Mbps	14 dBm ±2.5 dB
	802.11n HT20	MCS0	15 dBm ±2.5 dB
	802.11n HT20	MCS7	13 dBm ±2.5 dB
	802.11n HT40	MCS0	14 dBm ±2.5 dB
	802.11n HT40	MCS7	13 dBm ±2.5 dB
5 GHz	802.11a	6Mbps	14 dBm ±2.5 dB
	802.11a	54Mbps	13 dBm ±2.5 dB
	802.11n HT20	MCS0	15 dBm ±2.5 dB
	802.11n HT20	MCS7	13 dBm ±2.5 dB
	802.11n HT40	MCS0	15 dBm ±2.5 dB
	802.11n HT40	MCS7	13 dBm ±2.5 dB
	802.11ac VHT20	MCS0	15 dBm ±2.5 dB
	802.11ac VHT20	MCS8	13 dBm ±2.5 dB
	802.11ac VHT40	MCS0	14 dBm ±2.5 dB
	802.11ac VHT40	MCS9	13 dBm ±2.5 dB
	802.11ac VHT80	MCS0	13 dBm ±2.5 dB
	802.11ac VHT80	MCS9	12 dBm ±2.5 dB

Table 25: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-94 dBm
	802.11b	11 Mbps	-86 dBm
	802.11g	6 Mbps	-88 dBm
	802.11g	54 Mbps	-72 dBm
	802.11n HT20	MCS0	-87 dBm

	802.11n HT20	MCS7	-69 dBm
	802.11n HT40	MCS0	-85 dBm
	802.11n HT40	MCS7	-67 dBm
5 GHz	802.11a	6 Mbps	-89 dBm
	802.11a	54 Mbps	-72 dBm
	802.11n HT20	MCS0	-88 dBm
	802.11n HT20	MCS7	-69 dBm
	802.11n HT40	MCS0	-86 dBm
	802.11n HT40	MCS7	-67 dBm
	802.11ac VHT20	MCS8	-66 dBm
	802.11ac VHT40	MCS9	-62 dBm
	802.11ac VHT80	MCS9	-57 dBm

The reference specifications are listed below:

- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i: IEEE 802.11-2007 WLAN MAC and PHY, June 2007

4.2. Bluetooth Function Overview

The module supports ***Bluetooth Core Specification Version 4.2*** (BR/EDR + BLE) specifications, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Support up to 7 wireless connections
- Support up to 3.5 piconets at the same time
- Support one SCO or eSCO (Extended Synchronous Connection Oriented) connection

The BR/EDR channel bandwidth is 1 MHz and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz and can accommodate 40 channels.

Table 26: Bluetooth Data Rate and Versions

Version	Data rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 kbit/s
2.0+EDR	3 Mbit/s	> 80 kbit/s
3.0+HS	24 Mbit/s	Refer to 3.0+HS
4.0	24 Mbit/s	Refer to 4.0 LE
4.2	60 Mbit/s	Refer to 4.2 LE

The reference specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specifications 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specifications, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specifications, Core_v4.2, December 12, 2014

4.2.1. Bluetooth Performance

The following table lists the Bluetooth transmitting and receiving performance of the module.

Table 27: Bluetooth Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	10 dBm ±2.5 dB	8 dBm ±2.5 dB	8 dBm ±2.5 dB
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-90 dBm	-90 dBm	-85 dBm

5 GNSS

The module integrates a GNSS engine (Gen 8C) which supports multiple positioning and navigation systems including GPS, GLONASS, and BeiDou/COMPASS. With an embedded LNA, the positioning accuracy of the module has been significantly improved.

5.1. GNSS Performance

The following table lists the GNSS performance of the module in conduction mode.

Table 28: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity (GNSS)	Cold start	-145	dBm
	Reacquisition	-157	dBm
	Tracking	-157	dBm
TTFF (GNSS)	Cold start	34.3	s
	Warm start	26.9	s
	Hot start	3.7	s
Static Drift (GNSS)	CEP-50	< 2.5	m

5.2. GNSS Design Guidelines

Bad design of antenna signal traces layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, and reduced positioning accuracy. To avoid these, follow the design rules listed below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna traces layout) to avoid mutual interference.
- In user systems, GNSS RF signal traces and RF components should be placed far away from high-speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with a harsh electromagnetic environment or high ESD-protection requirements, it is recommended to add ESD protection diodes for the antenna interface. Only diodes with ultra-low junction capacitance such as 0.5 pF can be selected. Otherwise, there will be effects on the impedance characteristic of the RF circuit loop or attenuation of the bypass RF signal may be caused.
- Control the impedance of both the antenna feeder and PCB trace at 50 Ω, and keep the trace length as short as possible.
- See ***Chapter 6.3*** for GNSS antenna reference circuit designs.

6 Antenna Interfaces

The module provides five antenna interfaces for five types of antennas: the main antenna, the Rx-diversity/MIMO antenna, the GNSS antenna, the Wi-Fi/BT antenna and the FM antenna. Each antenna port has an impedance of 50 Ω.

6.1. Main and Rx-diversity Antenna Interfaces

The pin definition of main/Rx-diversity antenna interfaces is shown below.

Table 29: Pin Definition of Main and Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	19	AIO	Main antenna interface	50 Ω impedance
ANT_DRX	149	AI	Diversity and MIMO antenna interface	50 Ω impedance

The operating frequencies of the series are listed in the following tables.

Table 30: SC606T-EM Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869–894	824–849	MHz
EGSM900	925–960	880–915	MHz
DCS1800	1805–1880	1710–1785	MHz
PCS1900	1930–1990	1850–1910	MHz
WCDMA B1	2110–2170	1920–1980	MHz
WCDMA B2	1930–1990	1850–1910	MHz
WCDMA B4	2110–2155	1710–1755	MHz

WCDMA B5	869–894	824–849	MHz
WCDMA B8	925–960	880–915	MHz
LTE-FDD B1	2110–2170	1920–1980	MHz
LTE-FDD B2	1930–1990	1850–1910	MHz
LTE-FDD B3	1805–1880	1710–1785	MHz
LTE-FDD B4	2110–2155	1710–1755	MHz
LTE-FDD B5	869–894	824–849	MHz
LTE-FDD B7	2620–2690	2500–2570	MHz
LTE-FDD B8	925–960	880–915	MHz
LTE-FDD B20	791–821	832–862	MHz
LTE-FDD B28A	758–788	703–733	MHz
LTE-FDD B28B	773–803	718–748	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41 1)	2496–2690	2496–2690	MHz

Table 31: SC606T-NA Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B2	1930–1990	1850–1910	MHz
WCDMA B4	2110–2155	1710–1755	MHz
WCDMA B5	869–894	824–849	MHz
LTE-FDD B2	1930–1990	185–1910	MHz
LTE-FDD B4	2110–2155	1710–1755	MHz
LTE-FDD B5	869–894	824–849	MHz
LTE-FDD B7	2620–2690	2500–2570	MHz
LTE-FDD B12	729–746	699–716	MHz

LTE-FDD B13	746–756	777–787	MHz
LTE-FDD B14	758–768	788–798	MHz
LTE-FDD B17	734–746	704–716	MHz
LTE-FDD B25	1930–1995	1850–1915	MHz
LTE-FDD B26	859–894	814–849	MHz
LTE-FDD B66	2110–2200	1710–1780	MHz
LTE-FDD B71	617–652	663–698	MHz
LTE-TDD B41 [4]	2496–2690	2496–2690	MHz

6.1.1. Reference Design for Main and Rx-diversity Antenna Interfaces

A reference circuit design for the main and Rx-diversity antenna interfaces is shown below. A π-type matching circuit should be reserved for both ANT_MAIN and ANT_DRX for better RF performance, and the π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default and the resistors are 0 Ω.

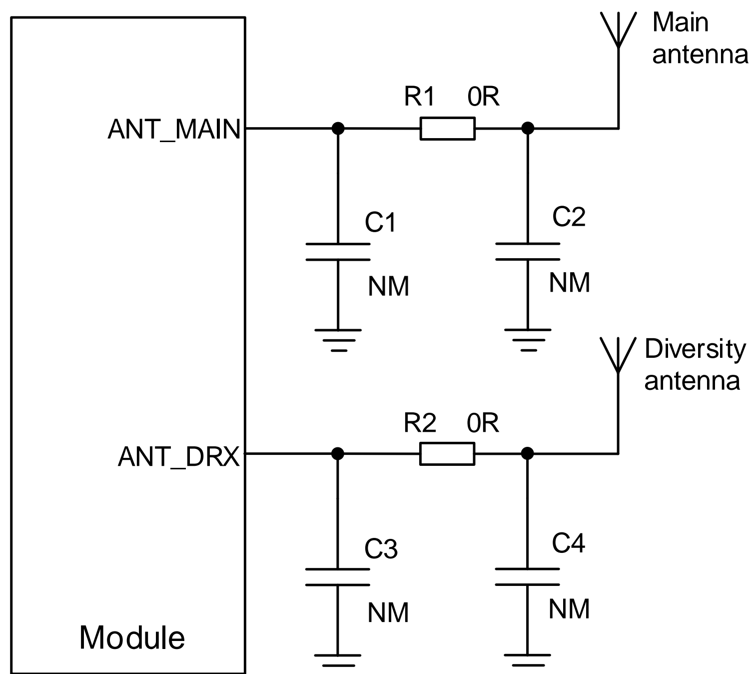

Figure 30: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

[4] The bandwidth of LTE-TDD B41 for SC606T-EM, SC606T-NA is 200 MHz (2496–2690 MHz), and the corresponding uplink EARFCN ranges from 39650 to 41589.

6.1.2. Reference Designs for RF Layouts

For the user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

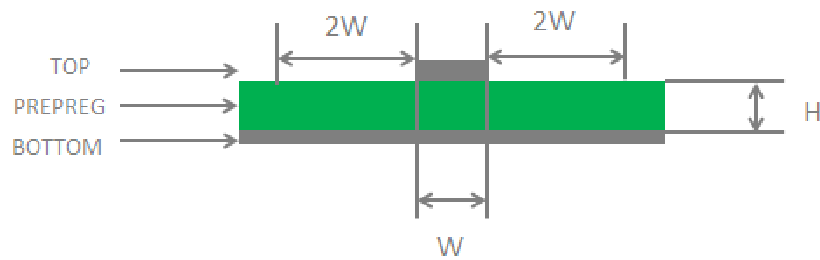

Figure 31: Microstrip Design on a 2-layer PCB

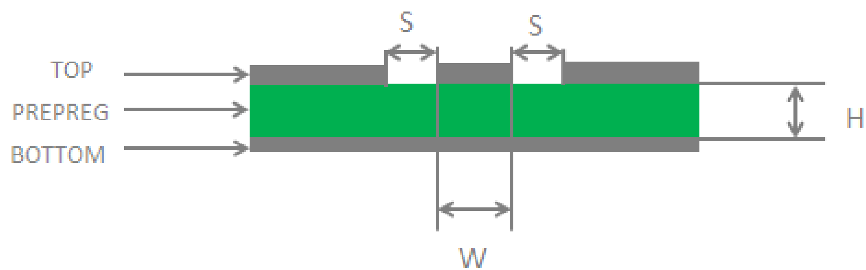

Figure 32: Coplanar Waveguide Design on a 2-layer PCB

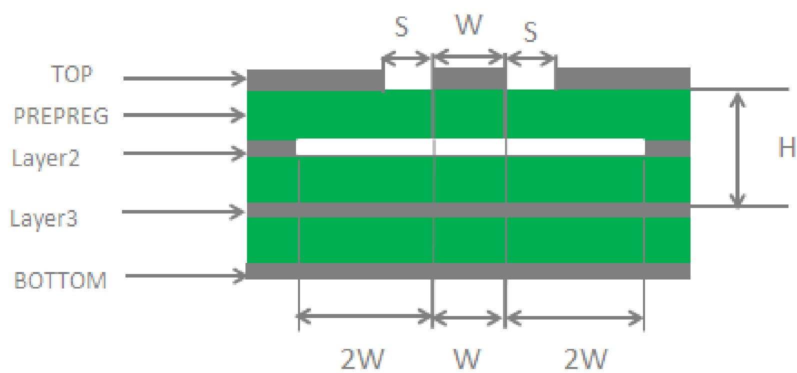

Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

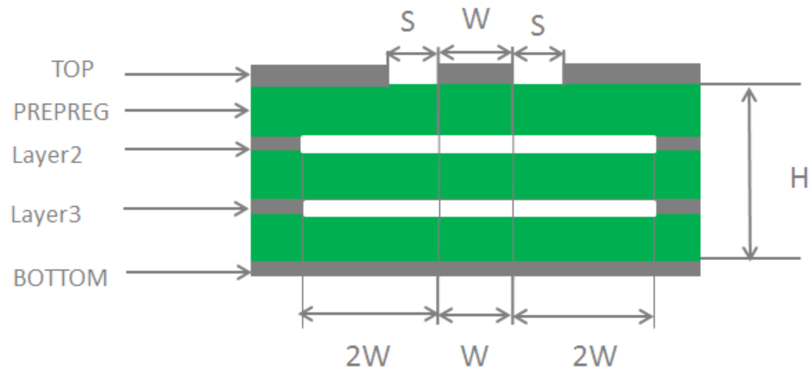

Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pins and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curve ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2 × W).

For more details about the RF layout, see ***document [4]***.

6.2. Wi-Fi/Bluetooth and FM Antenna Interfaces

The pin definition of Wi-Fi/Bluetooth and FM antenna interfaces and operating frequencies are shown below.

Table 32: Pin Definition of Wi-Fi/Bluetooth and FM Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω impedance

ANT_FM	244	AI	FM antenna interface	50 Ω impedance

Table 33: Wi-Fi/Bluetooth and FM Frequency

Type	Frequency	Unit
Wi-Fi 802.11a/b/g/n/ac	2402–2482 5180–5825	MHz
Bluetooth Core Specification Version 4.2	2402–2480	MHz
FM	76–108	MHz

The reference circuit designs for the Wi-Fi/Bluetooth antenna interface and the FM antenna interface are shown below. A π-type matching circuit is recommended to be reserved for both interfaces for better RF performance. The capacitors are not mounted by default and resistors are 0 Ω.

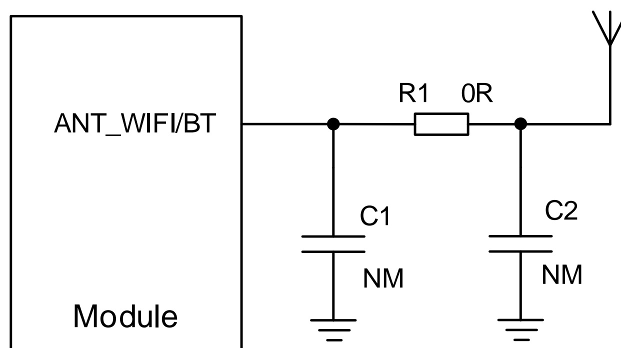

Figure 35: Reference Circuit Design for Wi-Fi/Bluetooth Antenna Interface

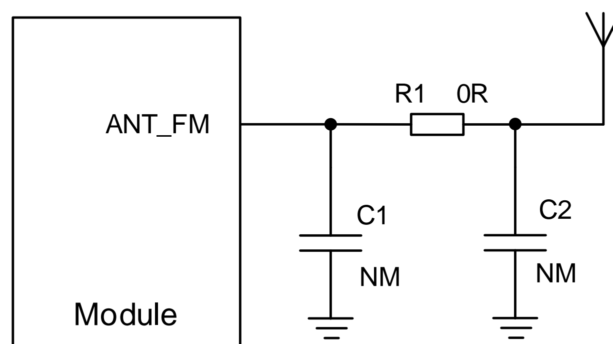

Figure 36: Reference Circuit Design for FM Antenna Interface

6.3. GNSS Antenna Interface

The pin definition of GNSS antenna interface and operating frequencies are shown below.

Table 34: Pin Definition of GNSS Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	134	AI	GNSS antenna Interface	50 Ω impedance
GNSS_LNA_EN	202	DO	LNA enable control	For test purpose only. If unused, keep it open.

Table 35: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
BeiDou	1561.098 ±2.046	MHz

6.3.1. Reference Design for Passive Antenna

The GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

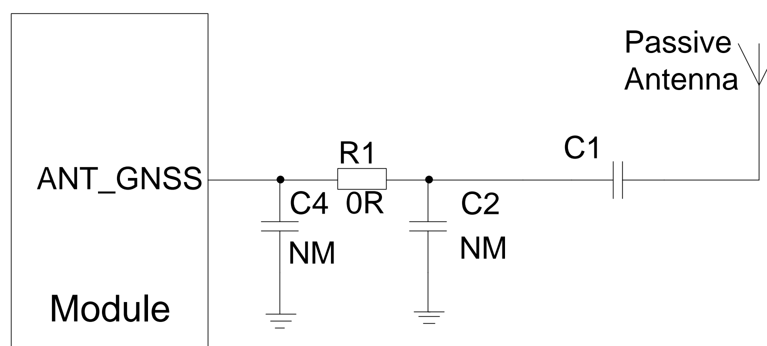

Figure 37: Reference Design for GNSS Passive Antenna

NOTE

When the passive antenna is placed far away from the module and the trace is long, it is recommended to add an external LNA circuit for better GNSS receiving performance, and the LNA should be placed close to the antenna.

6.3.2. Reference Design for Active Antenna

The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Featuring low power consumption, the active antenna requires a stable and clean power. It is recommended to use a high-performance LDO to regulate the supply voltage for the active antenna. A reference design of GNSS active antenna is shown below.

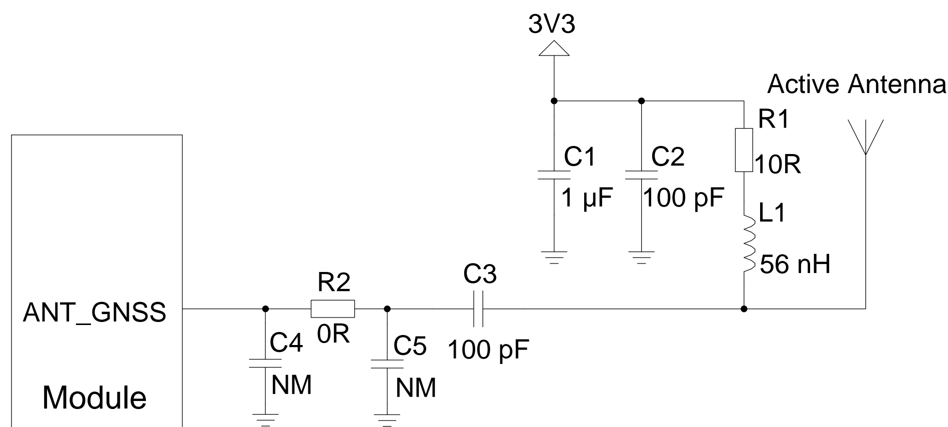

Figure 38: Reference Design for GNSS Active Antenna

6.4. Antenna Installation

6.4.1. Antenna Requirements

The following table shows the requirements on the main antenna, the Rx-diversity antenna, the Wi-Fi/Bluetooth antenna, and the GNSS antenna.

Table 36: Antenna Requirements

Antenna Type	Requirements
GSM/WCDMA/ LTE	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50

	Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1 dB (GSM850, EGSM900, WCDMA B5/B6/B8/B19, LTE B5/B8/B12/B13/B14/B17/B18/B19/B20/B26/B28A/B28B/B71) Cable Insertion Loss: < 1.5 dB (DCS1800, PCS1900, WCDMA B1/B2/B4, LTE B1/B2/B3/B4/B11/B21/B25/B34/B39/B66) Cable Insertion Loss: < 2 dB (LTE-FDD B7, LTE-TDD B38/B40/B41)
Wi-Fi/Bluetooth	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1 dB
GNSS [5]	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive Antenna Gain: > 0 dBi Active Antenna Noise Figure: <1.5 dB (Typ.) Active Antenna Gain: > -2 dBi Active Antenna Embedded LNA Gain: < 17 dB (Typ.) Active Antenna Total Gain: < 17 dBi (Typ.)

[5] As the harmonics generated by LTE B13 and B14 may saturate the LNA of active antennas, it is recommended to use the passive antenna in such networks.

6.4.2. Recommended RF Connector for Antenna Installation

If an RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by HIROSE.

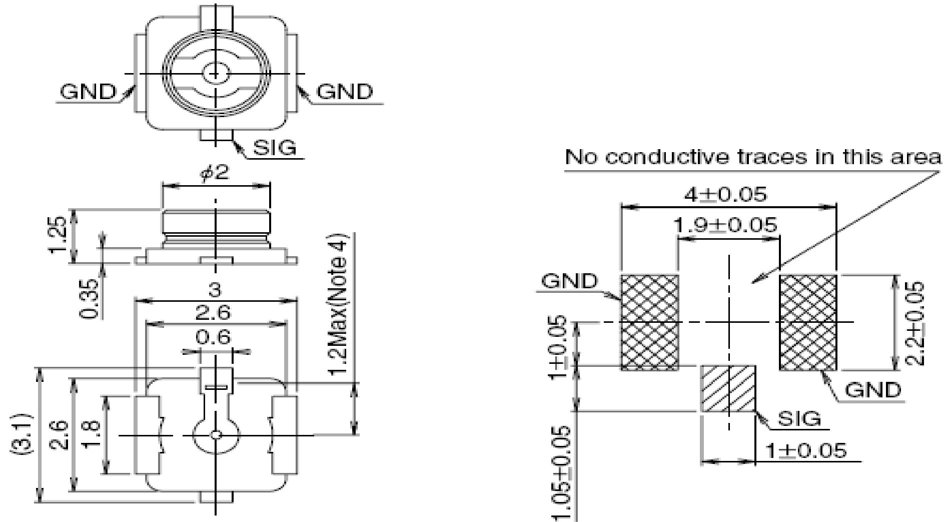

Figure 39: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

The U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Mechanicals of U.FL-LP Connectors

The following figure describes the form factor of the mated connectors.

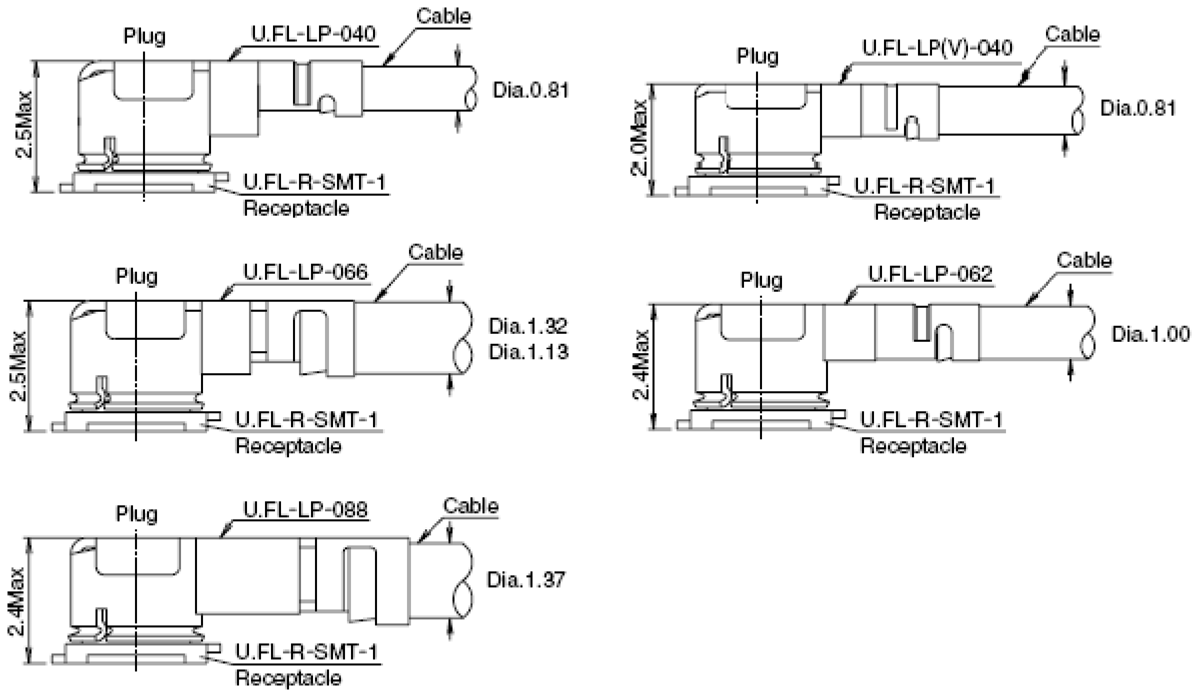

Figure 41: Form Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

7 Reliability, Electrical and Radio Characteristics

7.1. Absolute Maximum Ratings

The absolute maximum ratings of the power and voltage supplied to the digital and analog pins of the module are listed in the following table.

Table 37: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	6	V
USB_VBUS	-0.3	10	V
Current on VBAT	0	3	A
Voltage on Digital Pins	-0.3	2.16	V

7.2. Operating Power

Table 38: Operating Power

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	Peak supply voltage for VBAT	The actual input voltage must fall between the minimum and maximum values	3.55	3.8	4.4	V
	Voltage drop during a transmitting burst	Maximum power control level at EGSM900	-	-	400	mV

I_{VBAT}	Peak supply current (during a transmission slot)	Maximum power control level at EGSM900	-	1.8	3.0	A
USB_VBUS			4.0	5.0	6.0	V
VRTC	Supply voltage of a backup battery		2.0	3.0	3.25	V

7.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 39: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [6]	-35	+25	+75	°C
Storage temperature range	-40		+90	°C

7.4. Current Consumption

The current consumptions of the module in different conditions are listed in the following tables.

Table 40: SC606T-EM Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	80	μA
GSM supply current	Sleep (USB disconnected) @ DRX = 2	4.5	mA
	Sleep (USB disconnected) @ DRX = 5	3.5	mA
	Sleep (USB disconnected) @ DRX = 9	3	mA
WCDMA supply current	Sleep (USB disconnected) @ DRX = 6	3.47	mA

[6] Within the operating temperature range, the module is 3GPP compliant.

	Sleep (USB disconnected) @ DRX = 8	3.11	mA
	Sleep (USB disconnected) @ DRX = 9	2.75	mA
LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 6	3.85	mA
	Sleep (USB disconnected) @ DRX = 8	2.96	mA
LTE-TDD supply current	Sleep (USB disconnected) @ DRX = 6	4.27	mA
	Sleep (USB disconnected) @ DRX = 8	3.17	mA
GSM voice call	GSM850 @ PCL 5	280	mA
	GSM850 @ PCL 12	125	mA
	GSM850 @ PCL 19	110	mA
	EGSM900 @ PCL 5	280	mA
	EGSM900 @ PCL 12	120	mA
	EGSM900 @ PCL 19	100	mA
	DCS1800 @ PCL 0	210	mA
	DCS1800 @ PCL 7	140	mA
	DCS1800 @ PCL 15	130	mA
	PCS1900 @ PCL 0	210	mA
	PCS1900 @ PCL 7	130	mA
	PCS1900 @ PCL 15	125	mA
WCDMA voice call	B1 @ max power	620	mA
	B2 @ max power	550	mA
	B4 @ max power	580	mA
	B5 @ max power	590	mA
	B8 @ max power	560	mA
GPRS data transfer	GSM850 (1UL/4DL) @ PCL 5	240	mA
	GSM850 (2UL/3DL) @ PCL 5	370	mA

	GSM850 (3UL/2DL) @ PCL 5	440	mA
	GSM850 (4UL/1DL) @ PCL 5	500	mA
	EGSM900 (1UL/4DL) @ PCL 5	260	mA
	EGSM900 (2UL/3DL) @ PCL 5	380	mA
	EGSM900 (3UL/2DL) @ PCL 5	490	mA
	EGSM900 (4UL/1DL) @ PCL 5	520	mA
	DCS1800 (1UL/4DL) @ PCL 0	190	mA
	DCS1800 (2UL/3DL) @ PCL 0	280	mA
	DCS1800 (3UL/2DL) @ PCL 0	350	mA
	DCS1800 (4UL/1DL) @ PCL 0	420	mA
	PCS1900 (1UL/4DL) @ PCL 0	190	mA
	PCS1900 (2UL/3DL) @ PCL 0	290	mA
	PCS1900 (3UL/2DL) @ PCL 0	370	mA
	PCS1900 (4UL/1DL) @ PCL 0	420	mA
EDGE data transfer	GSM850 (1UL/4DL) @ PCL 8	170	mA
	GSM850 (2UL/3DL) @ PCL 8	250	mA
	GSM850 (3UL/2DL) @ PCL 8	320	mA
	GSM850 (4UL/1DL) @ PCL 8	370	mA
	EGSM900 (1UL/4DL) @ PCL 8	170	mA
	EGSM900 (2UL/3DL) @ PCL 8	260	mA
	EGSM900 (3UL/2DL) @ PCL8	340	mA
	EGSM900 (4UL/1DL) @ PCL 8	380	mA
	DCS1800 (1UL/4DL) @ PCL 2	170	mA
	DCS1800 (2UL/3DL) @ PCL 2	260	mA
	DCS1800 (3UL/2DL) @ PCL 2	330	mA

	DCS1800 (4UL/1DL) @ PCL 2	400	mA
	PCS1900 (1UL/4DL) @ PCL 2	170	mA
	PCS1900 (2UL/3DL) @ PCL 2	260	mA
	PCS1900 (3UL/2DL) @ PCL 2	400	mA
	PCS1900 (4UL/1DL) @ PCL 2	410	mA
WCDMA data transfer	B1 (HSDPA) @ max power	550	mA
	B2 (HSDPA) @ max power	510	mA
	B4 (HSDPA) @ max power	530	mA
	B5 (HSDPA) @ max power	550	mA
	B8 (HSDPA) @ max power	510	mA
	B1 (HSUPA) @ max power	580	mA
	B2 (HSUPA) @ max power	530	mA
	B4 (HSUPA) @ max power	550	mA
	B5 (HSUPA) @ max power	520	mA
	B8 (HSUPA) @ max power	520	mA
LTE data transfer	LTE-FDD B1 @ max power	550	mA
	LTE-FDD B2 @ max power	530	mA
	LTE-FDD B3 @ max power	650	mA
	LTE-FDD B4 @ max power	530	mA
	LTE-FDD B5 @ max power	560	mA
	LTE-FDD B7 @ max power	680	mA
	LTE-FDD B8 @ max power	550	mA
	LTE-FDD B20 @ max power	530	mA
	LTE-FDD B28A @ max power	580	mA
	LTE-FDD B28B @ max power	570	mA

	LTE-TDD B38 @ max power	600	mA
	LTE-TDD B40 @ max power	430	mA
	LTE-TDD B41 @ max power	580	mA

7.5. RF Output Power

The following tables show the RF output power of the series.

Table 41: SC606T-EM RF Output Power

Frequency	Max.	Min.
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
WCDMA B1	24 dBm +1/-3 dB	< -49 dBm
WCDMA B2	24 dBm +1/-3 dB	< -49 dBm
WCDMA B4	24 dBm +1/-3 dB	< -49 dBm
WCDMA B5	24 dBm +1/-3 dB	< -49 dBm
WCDMA B8	24 dBm +1/-3 dB	< -49 dBm
LTE-FDD B1	23 dBm ±2 dB	< -39 dBm
LTE-FDD B2	23 dBm ±2 dB	< -39 dBm
LTE-FDD B3	23 dBm ±2 dB	< -39 dBm
LTE-FDD B4	23 dBm ±2 dB	< -39 dBm
LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B7	23 dBm ±2 dB	< -39 dBm
LTE-FDD B8	23 dBm ±2 dB	< -39 dBm

LTE-FDD B20	23 dBm ±2 dB	< -39 dBm
LTE-FDD B28A	23 dBm ±2 dB	< -39 dBm
LTE-FDD B28B	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38	23 dBm ±2 dB	< -39 dBm
LTE-TDD B40	23 dBm ±2 dB	< -39 dBm
LTE-TDD B41	23 dBm ±2 dB	< -39 dBm

Table 42: SC606T-NA RF Output Power

Frequency	Max.	Min.
WCDMA B2	24 dBm +1/-3 dB	< -49 dBm
WCDMA B4	24 dBm +1/-3 dB	< -49 dBm
WCDMA B5	24 dBm +1/-3 dB	< -49 dBm
LTE-FDD B2	23 dBm ±2 dB	< -39 dBm
LTE-FDD B4	23 dBm ±2 dB	< -39 dBm
LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B7	23 dBm ±2 dB	< -39 dBm
LTE-FDD B12	23 dBm ±2 dB	< -39 dBm
LTE-FDD B13	23 dBm ±2 dB	< -39 dBm
LTE-FDD B14	23 dBm ±2 dB	< -39 dBm
LTE-FDD B17	23 dBm ±2 dB	< -39 dBm
LTE-FDD B25	23 dBm ±2 dB	< -39 dBm
LTE-FDD B26	23 dBm ±2 dB	< -39 dBm
LTE-FDD B66	23 dBm ±2 dB	< -39 dBm
LTE-FDD B71	23 dBm ±2 dB	< -39 dBm
LTE-TDD B41	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3 dB. This design conforms to the GSM specifications as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

7.6. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of the series.

Table 43: SC606T-EM RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-109	-	-	-102.4 dBm
EGSM900	-108	-	-	-102.4 dBm
DCS1800	-107	-	-	-102.4 dBm
PCS1900	-107	-	-	-102.4 dBm
WCDMA B1	-109	-109	-110	-106.7 dBm
WCDMA B2	-109	-109	-110	-106.7 dBm
WCDMA B4	-109	-108.5	-110	-104.7 dBm
WCDMA B5	-109.5	-108	-110.5	-104.7 dBm
WCDMA B8	-109	-109	-110.5	-104.7 dBm
LTE-FDD B1 (10 MHz)	-97	-97	-100	-96.3 dBm
LTE-FDD B2 (10 MHz)	-97	-97	-100	-94.3 dBm
LTE-FDD B3 (10 MHz)	-96.5	-96.5	-99	-93.3 dBm
LTE-FDD B4 (10 MHz)	-97	-97	-100	-96.3 dBm
LTE-FDD B5 (10 MHz)	-97.5	-98	-100	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96	-96	-99	-94.3 dBm

LTE-FDD B8 (10 MHz)	-97.5	-97.5	-100.5	-93.3 dBm
LTE-FDD B20 (10 MHz)	-96.5	-97.5	-100	-93.3 dBm
LTE-FDD B28A (10 MHz)	-97	-96.5	-99.5	-94.8 dBm
LTE-FDD B28B (10 MHz)	-97	-95.5	-99	-94.8 dBm
LTE-TDD B38 (10 MHz)	-96.5	-96	-99	-96.3 dBm
LTE-TDD B40 (10 MHz)	-96.5	-95.5	-99	-96.3 dBm
LTE-TDD B41 (10 MHz)	-96.5	-95.5	-99	-94.3 dBm

Table 44: SC606T-NA RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	-109	-109	-111	-106.7 dBm
WCDMA B4	-109	-109	-110.5	-104.7 dBm
WCDMA B5	-109.5	-109.5	-111	-104.7 dBm
LTE-FDD B2 (10 MHz)	-97	-97	-99.5	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97	-96.5	-98.5	-96.3 dBm
LTE-FDD B5 (10 MHz)	-98	-97.5	-100	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96	-96	-98	-94.3 dBm
LTE-FDD B12 (10 MHz)	-96	-97.5	-98.5	-93.3 dBm
LTE-FDD B13 (10 MHz)	-95.5	-97.5	-98	-93.3 dBm
LTE-FDD B14 (10 MHz)	-97	-97	-99	-93.3 dBm
LTE-FDD B17 (10 MHz)	-96	-97	-98	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97	-97	-99	-92.8 dBm
LTE-FDD B26 (10 MHz)	-97.5	-98	-99.5	-93.8 dBm
LTE-FDD B66 (10 MHz)	-97	-96.5	-98.5	-95.8 dBm

LTE-FDD B71 (10 MHz)	-96.5	-96.5	-99	-93.5 dBm
LTE-TDD B41 (10 MHz)	-96	-96	-98	-94.3 dBm

7.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of the module.

Table 45: ESD Characteristics (Temperature: 25 °C, Humidity: 45 %)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	+/-5	+/-10	kV
All Antenna Interfaces	+/-5	+/-10	kV
Other Interfaces	+/-0.5	+/-1	kV

8 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimension tolerances are ±0.2 mm unless otherwise specified.

8.1. Mechanical Dimensions of the Module

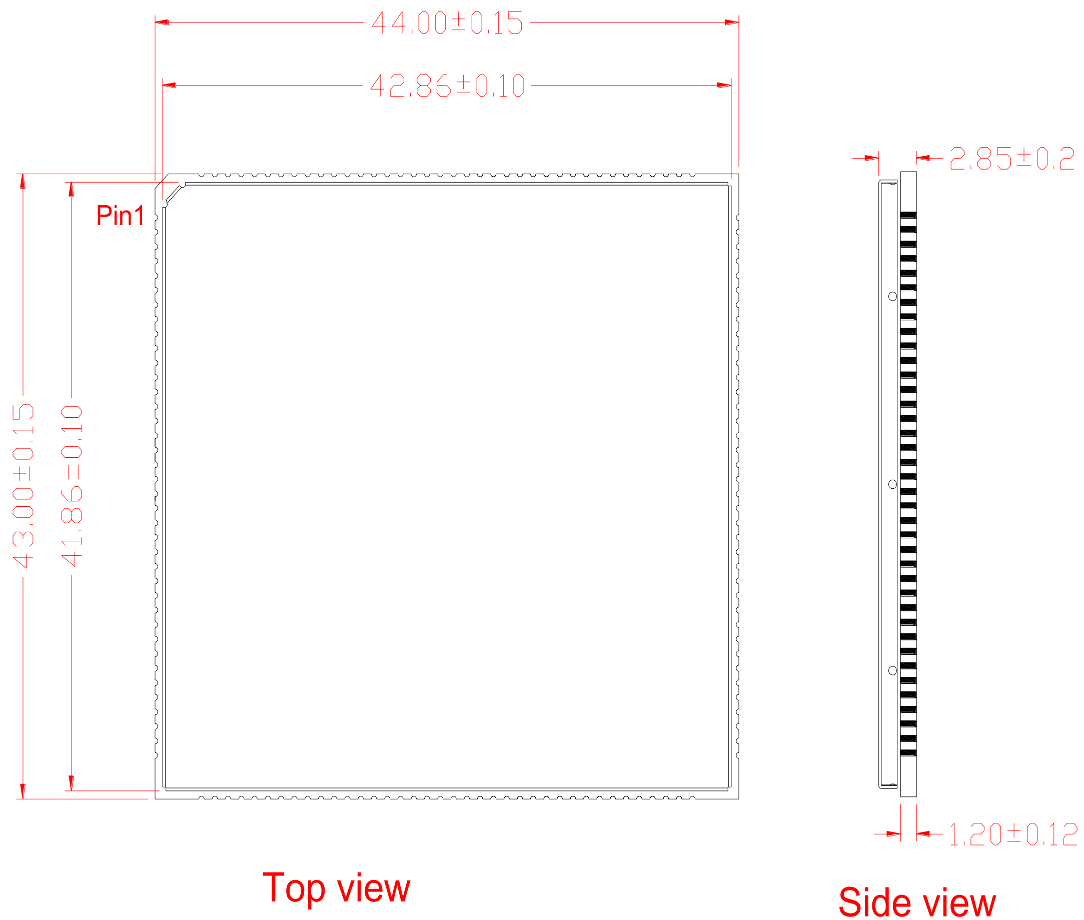

Figure 42: Top and Side Dimensions (Unit: mm)

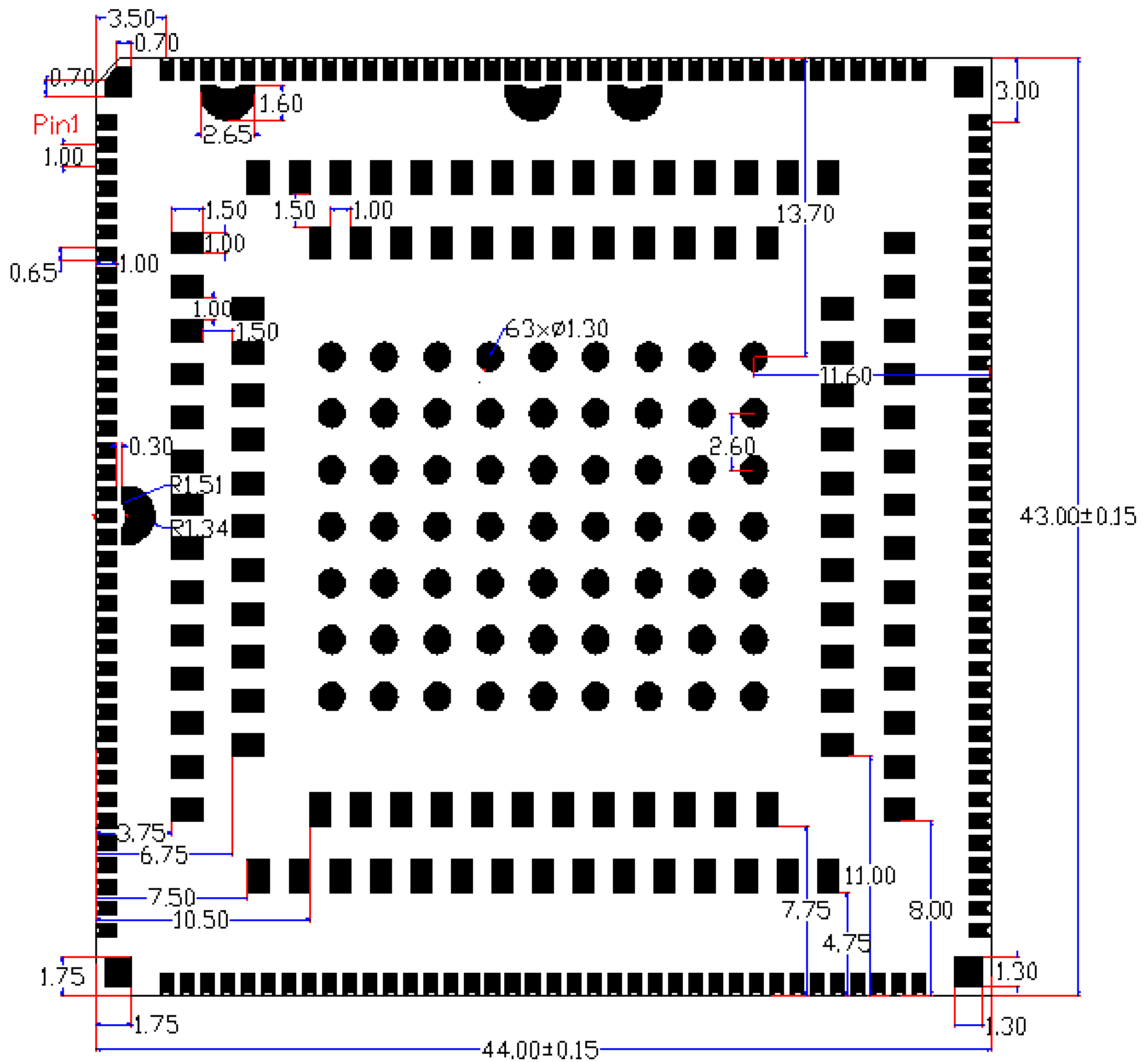

Figure 43: Bottom Dimensions (Perspective View)

NOTE

The package warpage level of the module conforms to JEITA ED-7306 standard.

8.2. Recommended Footprint

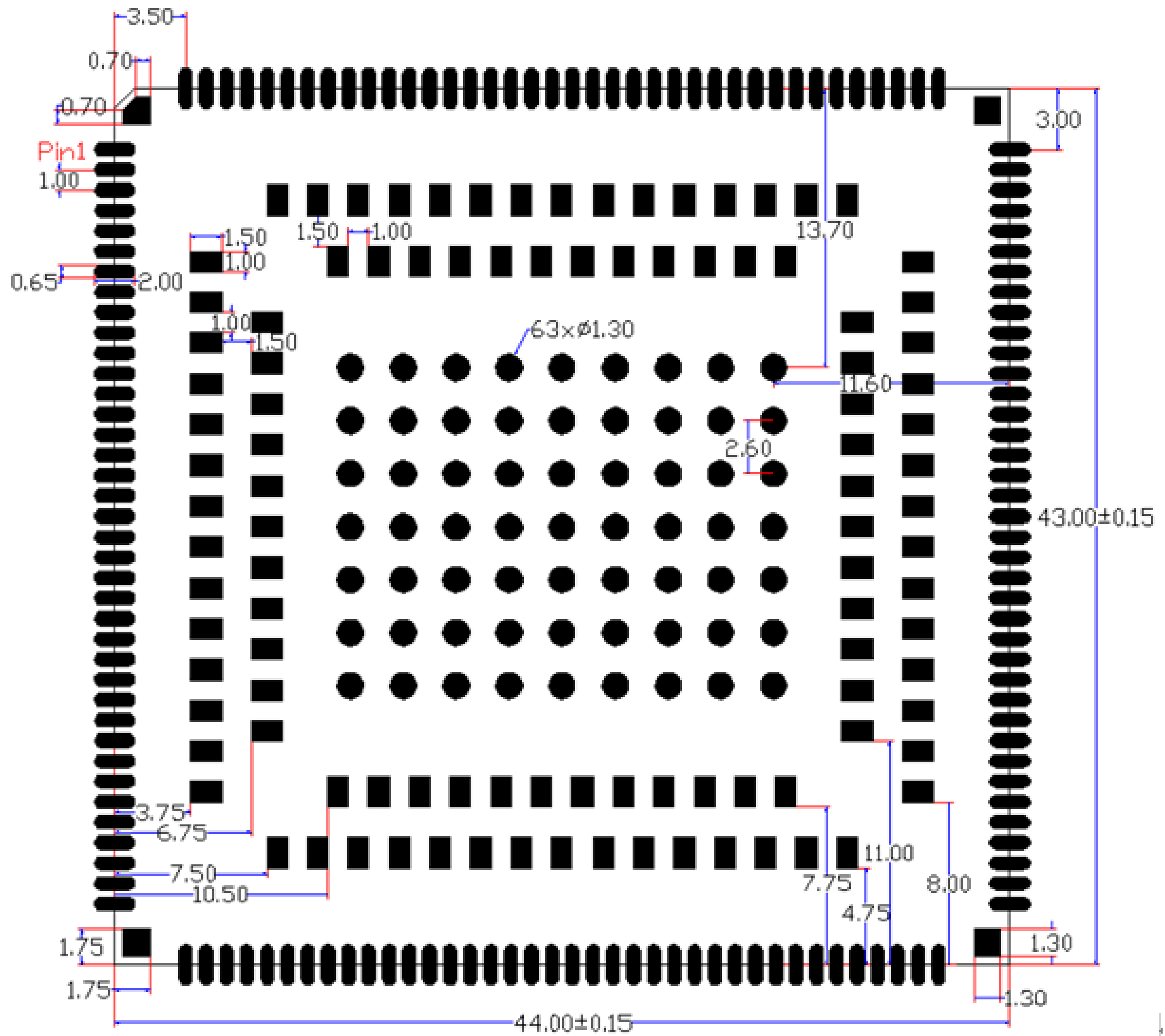

Figure 44: Recommended Footprint (Perspective View)

NOTE

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the host PCB.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

8.3. Top and Bottom Views of the Module

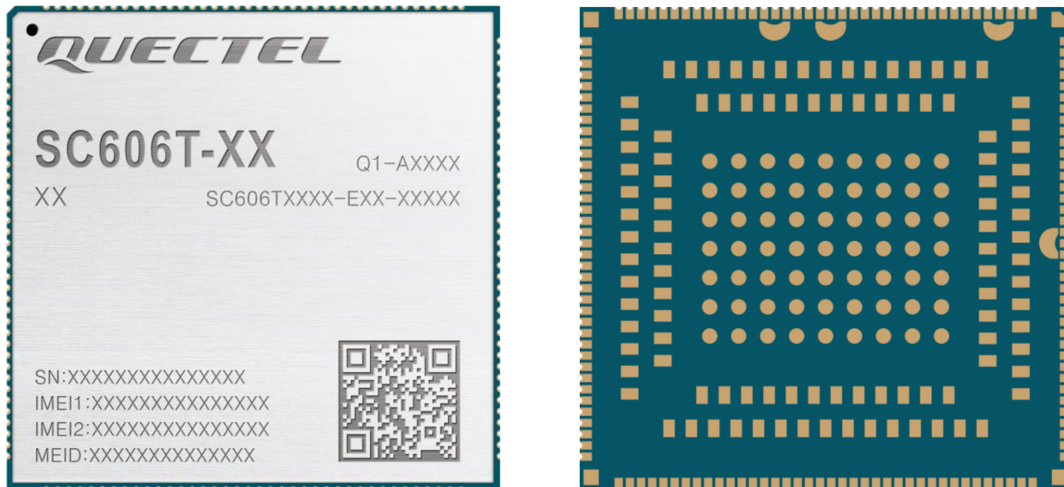

Figure 45: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60%.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours[7] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

5. If needed, the pre-baking should follow the requirements below:

- The module should be baked for 8 hours at 120 ±5 °C;
- All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [5]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

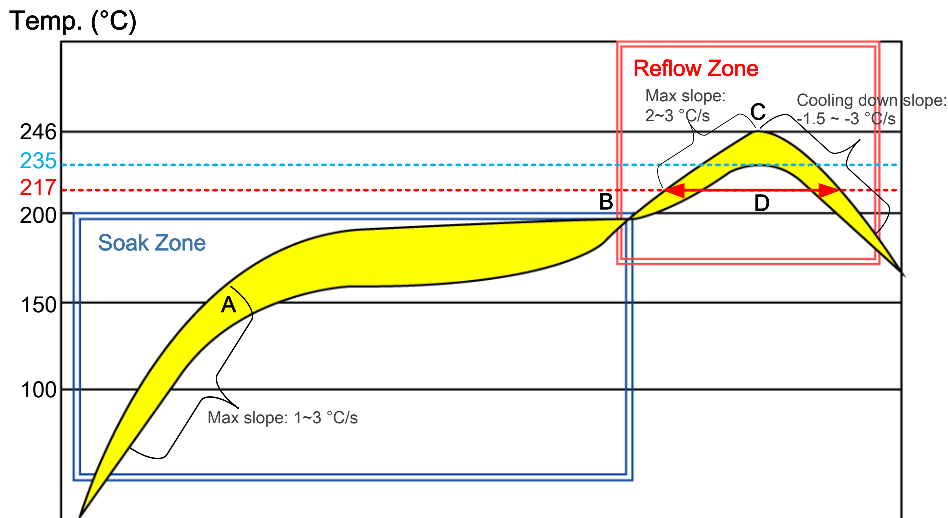

Figure 46: Recommended Reflow Soldering Thermal Profile

Table 46: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.

2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

9.3. Packaging

SC606T series module is packaged in tape and reel carriers. Each reel is 330 mm in diameter and contains 200 modules. The following figures show the package details, measured in mm.

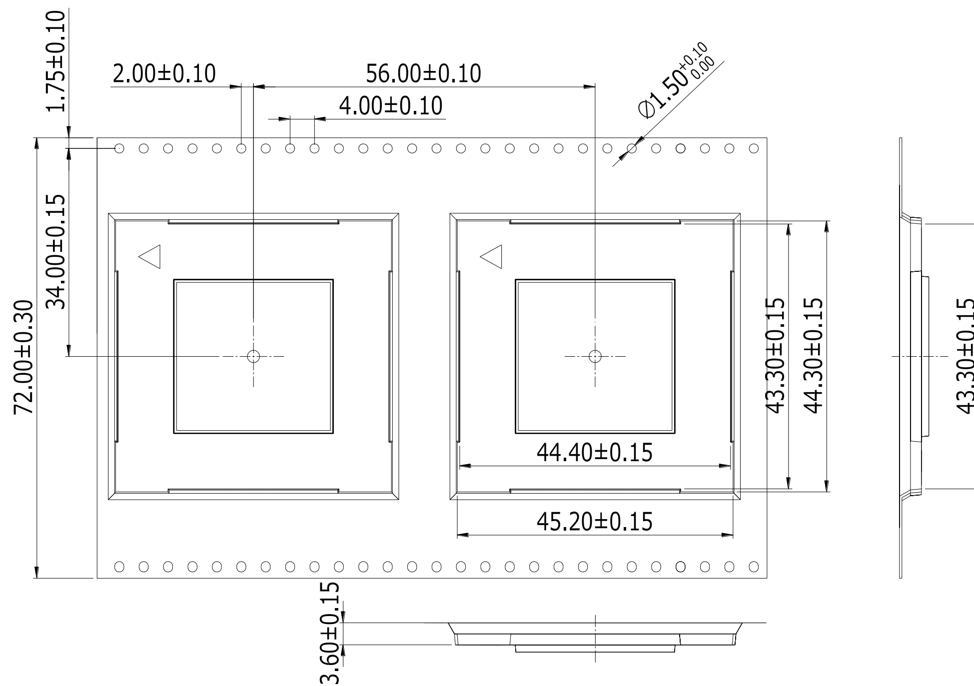

Figure 47: Tape Dimensions

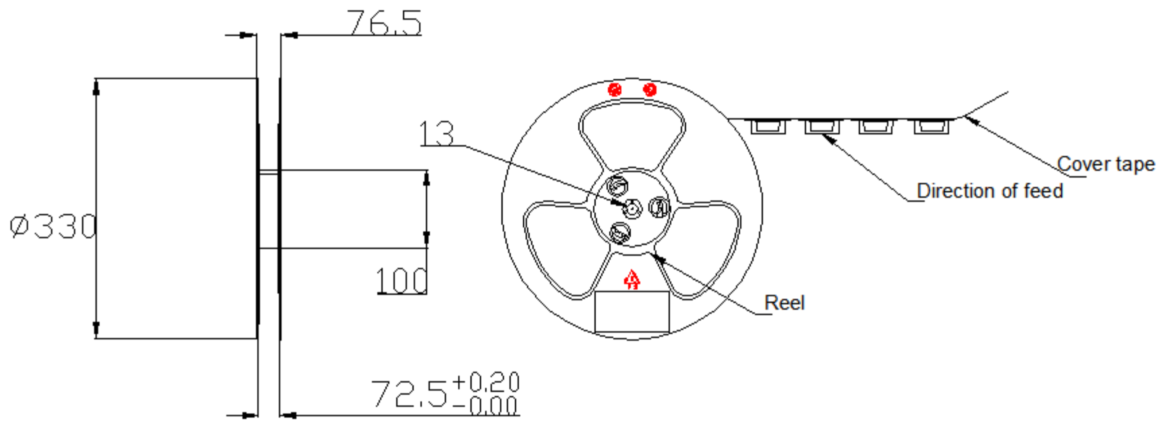

Figure 48: Reel Dimensions

Table 47: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 200 pcs	Minimum Package × 4 = 800 pcs
SC606T series	200	Size: 398 mm × 383 mm × 83 mm N.W: 1.92 kg G.W: 3.67 kg	Size: 420 mm × 350 mm × 405 mm N.W: 8.18 kg G.W: 15.18 kg

10 Appendix References

Table 48: Related Documents

Document Name
[1] Quectel_Smart_EVB-G2_User_Guide
[2] Quectel_SC606T_Series_Reference_Design
[3] Quectel_SC606T_Series_GPIO_Configuration
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_Secondary_SMT_User_Guide

Table 49: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
BLE	Bluetooth Low Energy
bps	Bits per Second
BR	Basic Rate
CA	Carrier Aggregation
CS	Coding Scheme
CSD	Circuit Switched Data
CSI	Channel State Information
CTS	Clear to Send
DIP	Dual In-line Package

DL	Downlink
DRX	Discontinuous Reception
DSP	Digital Signal Processor
ECM	Electret Condenser Microphone
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EGSM	Extended GSM900 band (includes standard GSM900 band)
ERM	Eccentric Rotating Mass
eSCO	Extended Synchronous Connection Oriented
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FEM	Front-End Module
FM	Frequency Modulation
FR	Full Rate
GLONASS	Globalnaya Navigazionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GPU	Graphics Processing Unit
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Down Link Packet Access
HSPA	High Speed Packet Access
IQ	Inphase and Quadrature
ISP	Image Signal Processing
LCC	Leadless Chip Carrier (package)

LCD	Liquid Crystal Display
LCM	LCD Module
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LRA	Linear Resonant Actuator
LTE-TDD	Long-Term Evolution Time-Division Duplex
MAC	Medium Access Control
MCS	Modulation and Coding Scheme
MEMS	Micro-Electro-Mechanical System
MIMO	Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
MO	Mobile Originated/Origination
MP	Megapixel
MT	Mobile Terminal/Termination
OTG	On-The-Go
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PHY	Physical
PMI	Power Management Interface
PMU	Power Management Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency

RGB	Red-Green-Blue
RH	Relative Humidity
RHCP	Right Hand Circularly Polarized
RTC	Real Time Clock
RTS	Request to Send
Rx	Receive
SCO	Synchronous Connection Oriented
SMS	Short Message Service
SPI	Serial Peripheral Interface
STA	Station
TDD	Time Division Distortion
TE	Terminal Equipment
TP	Touch Panel
TX	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
(U)SIM	(Universal) Subscriber Identity Module
V_I	Voltage Input
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
Vmax	Maximum Voltage Value
Vmin	Minimum Voltage Value
Vnom	Nominal Voltage Value
V_O	Voltage Output

V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WLED	White Light-Emitting Diode
WUXGA	Widescreen Ultra Extended Graphics Array