

RoHS Compliant

8GB DDR3 SDRAM 1.35V UDIMM

Product Specifications

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Version 1.4



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General Description

Apacer **D12.18211N.001** is a 1024M x 64 DDR3 SDRAM (Synchronous DRAM) DIMM. This high-density memory module consists of 16 pieces 512M x 8 bits DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM. The module is a 240-pins memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
D12.18211N.001	14.9 GB/sec	1866 Mbps	933 MHz	CL13

Density	Organization	Component	Rank
8GB	1024M x 64	512M x8*16	2

Key Parameters

MT/s	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	Unit
Grade	-CL7	-CL9	-CL11	-CL13	
tCK (min)	1.875	1.5	1.25	1.071	ns
CAS latency	7	9	11	13	tCK
tRCD (min)	13.125	13.5	13.75	13.91	ns
tRP (min)	13.125	13.5	13.75	13.91	ns
tRAS (min)	37.5	36	35	34	ns
tRC (min)	50.625	49.5	48.75	47.91	ns
CL-tRCD-tRP	7-7-7	9-9-9	11-11-11	13-13-13	tCK

Specifications:

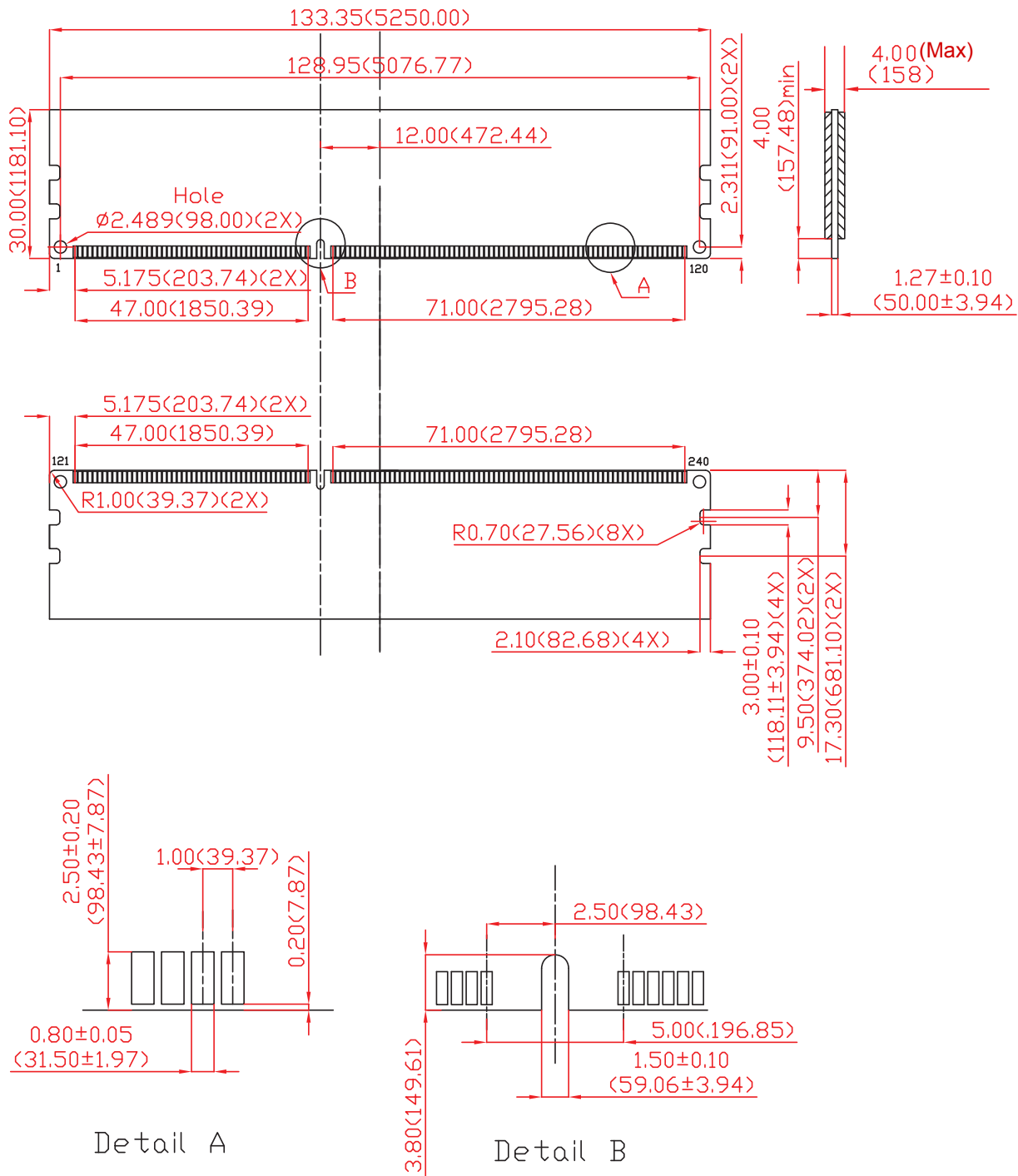
- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 1024 words x 64 bits, 2 ranks
- ◆ Integrating 16 pieces of 4G bits DDR3 SDRAM sealed FBGA
- ◆ Package: 240-pin socket type dual in-line memory module (DIMM)
- ◆ PCB: height 30.0 mm, lead pitch 1.0 mm (pin), lead-free (RoHS compliant)
- ◆ Power supply VDD: 1.35V (+0.1V ~ -0.067V)
- ◆ Backward compatible to VDD = VDDQ = 1.5V $\pm$ 0.075V
-Supports DDR3L devices to be backward compatible in 1.5V applications
- ◆ Serial Presence Detect (SPD)
- ◆ Eight Internal banks for concurrent operation (Components)
- ◆ Interface: SSTL_13
- ◆ Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- ◆ /CAS Latency (CL): 6, 7, 8, 9, 10, 11, 13
- ◆ /CAS Write Latency (CWL): 5, 6, 7, 8, 9
- ◆ Supports auto pre-charge option for each burst access
- ◆ Supports auto-refresh/self-refresh
- ◆ Refresh cycles: 7.8 μ s at 0°C $\leq$ TC $\leq$ +85°C

Features:

- ◆ Double-data-rate architecture: 2 data transfers per clock cycle
- ◆ The high-speed data transfer is realized by the 8-bits prefetch pipelined architecture.
- ◆ Bi-directional differential data strobe (DQS and /DQS) is transmitted / received with data for capturing data at the receiver
- ◆ DQS: edge-aligned with data for read; center aligned with data for write
- ◆ Differential clock inputs (CK and /CK)
- ◆ DLL aligns DQ and DQS transitions with CK transitions
- ◆ Data mask (DM) for writing data
- ◆ Posted /CAS by programmable additive latency for enhanced command and data bus efficiency
- ◆ On-Die-Termination (ODT) for improved signal quality: Synchronous ODT/Dynamic ODT/Asynchronous ODT
- ◆ Multi-Purpose Register (MPR) for temperature read out
- ◆ ZQ calibration for DQ drive and ODT
- ◆ Programmable Partial Array Self-Refresh (PASR)
- ◆ /Reset pin for power-up sequence and reset function
- ◆ SRT range: normal/extended, auto/manual self-refresh
- ◆ Programmable output driver impedance control
- ◆ Commands entered at each positive clock input, while data and data mask are referenced to both edges of DQS

Mechanical Drawing

Unit: mm



(All dimensions are in millimeters with $\pm 0.15\text{mm}$ tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
0.9	08/28/2012	Official release	
1.0	08/29/2012	release	
1.1	07/23/2013	Changed headquarters address	
1.2	05/08/2015	Updated Mechanical Drawing	
1.3	03/15/2017	Add Environmental Requirements	
1.4	09/04/2017	Remove TOPR (Operating Temperature (ambient))	

Global Presence

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