Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 240320C TMH-PW-N

2,6” TFT

Product Specification ***Ver.: 0***

11.02.2011

Revise Records

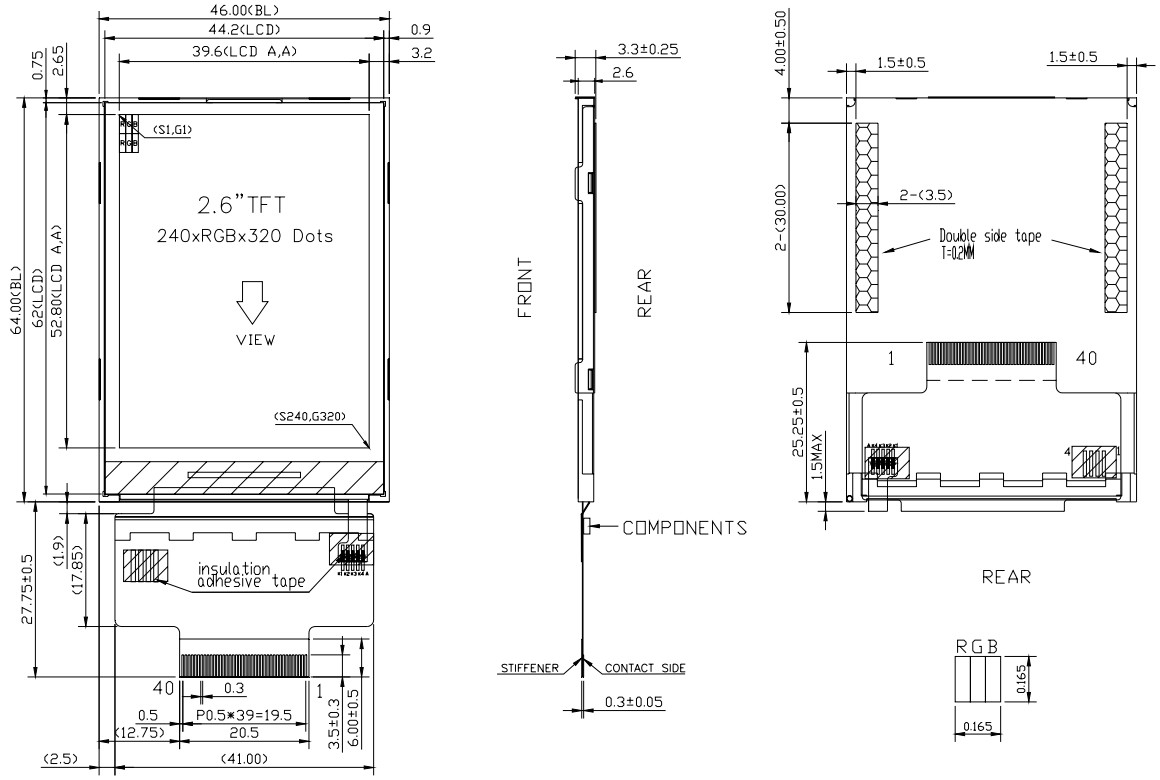
Rev.	Date	Contents	Written	Approved
0	11.02.2011	Preliminary Specification	CL	MH

Special Notes

Note1.	
Note2.	
Note3.	
Note4.	
Note5.	

CONTENT

1. LCM DRAWING



2. GENERAL DESCRIPTION

MAIN TECHNICS：	TFT, Negative Transmissive
DISPLAY CONTENT：	240 x RGB x 320, GRAPHIC
DISPLAY TYPE：	262k
DRIVER METHOD：	1/320 DUTY
VIEWING DIRECTION：	12:00
CONTROLLER:	R61580 (Renesas)
BACKLIGHT：	LED, Lightguide, White
OPERATING TEMPERATURE：	-20°C to +70°C
STORAGE TEMPERATURE：	-30°C to +80°C
INTERFACE:	SPI and 8080 Series MPU, 8/16-bit
REFERENCE DOCUMENTS:	R61580 datasheet

3. MECHANICAL SPECIFICATIONS

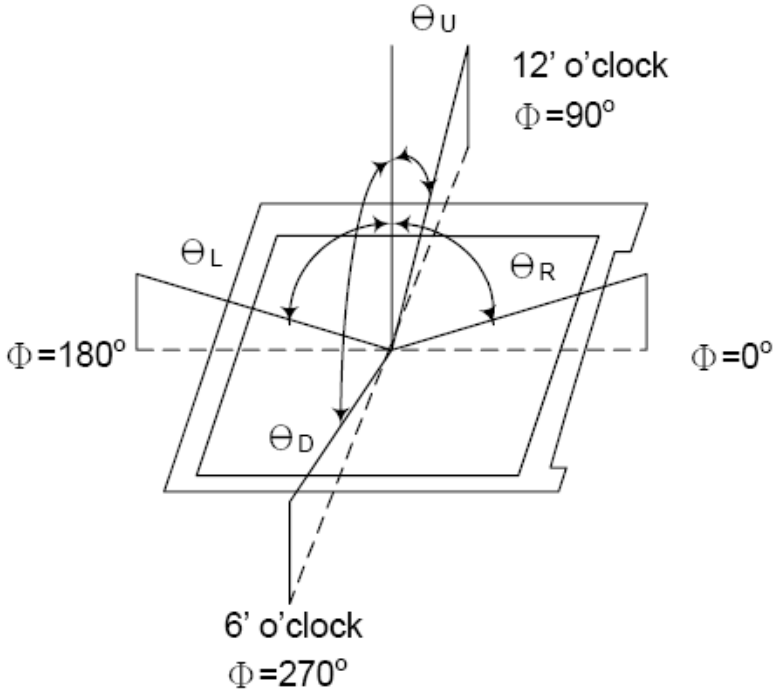
ITEM	CONTENT	UNIT
NUMBER OF PIXELS	**240 x RGB x 320**	**PIXEL**
MODULE DIMENSION	**46.00 x 91.75 x 3.30**	**mm**
ACTIVE AREA	**39.60 x 52.80**	**mm**
PIXEL SIZE	**0.165 x 0.165**	**mm**

4. ELECTRO-OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (without Polarizer)		T(%)	–	–	14.7	–	–	
Contrast Ratio		CR	Θ=0 Normal viewing angle – –	400	500	–	–	(1)(2)
Response time	Rising	T_R		–	2	4	msec	(1)(3)
	Falling	T_F		–	6	12		
Color gamut		S(%)			60		%	
Color chromaticity (CIE1931)	White	W_x		0.288	0.308	0.328		(1)(4) CF glass (C-light)
		Wy		0.305	0.325	0.345		
	Red	Rx		0.610	0.630	0.650		
		Ry		0.317	0.337	0.357		
	Green	Gx		0.264	0.284	0.304		
		Gy		0.523	0.543	0.563		
	Blue	Bx		0.123	0.143	0.163		
		By		0.100	0.120	0.140		
Viewing angle	Hor.	Θ_L	CR>10	35	45	–		
		Θ_R		35	45	–		
	Ver.	Θ_U		35	45	–		
		Θ_D		10	20	–		
Optima View Direction		12 O'clock						(5)

Measuring Equipment

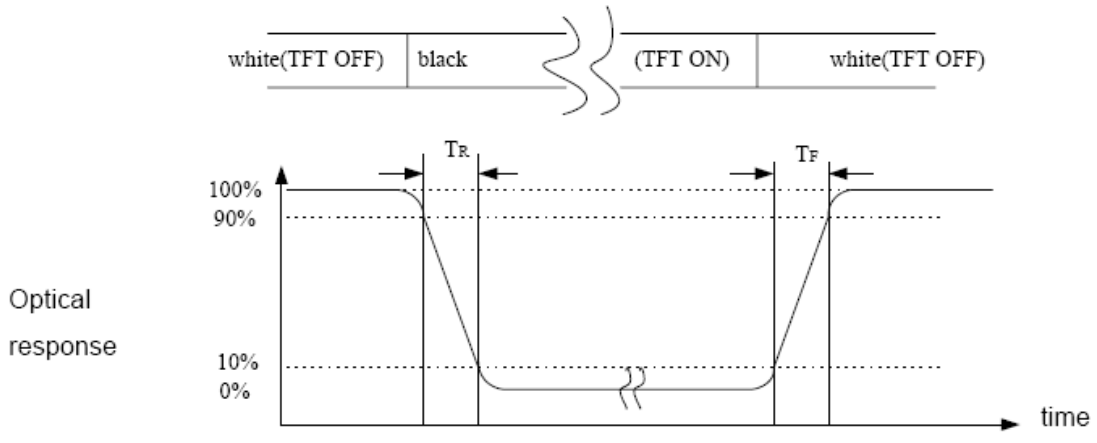
Note (1) Definition of Viewing Angle :



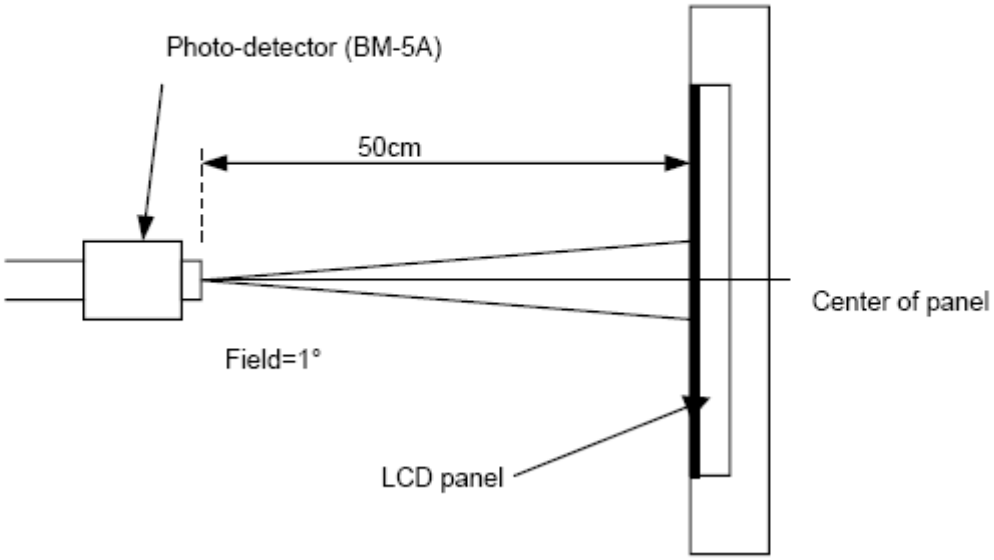
Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

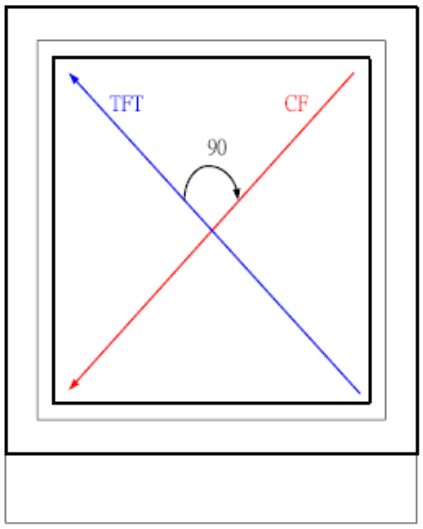
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup

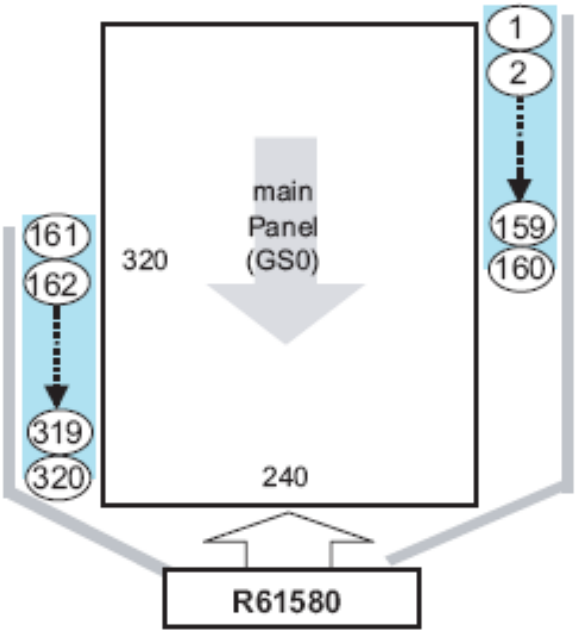


Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.



TFT Face up

5. BLOCK DIAGRAM



6. ELECTRONIC CHARACTERISTICS

6.1 MAXIMUM VALUES

ITEM	SYMBOL	STANDARD VALUE		UNIT
		MIN	MAX	
Logic supply voltage	V_{DD}	-0.3	+4.6	V
Operating Temperature	Top	-20	+70	°C
Storage Temperature	Tst	-30	+80	°C

6.2 DC CHARACTERISTICS

DC Characteristics 1 (VCC= 2.50V~3.30V, IOVCC=1.65V~3.30V, Ta=-40C~+85C)

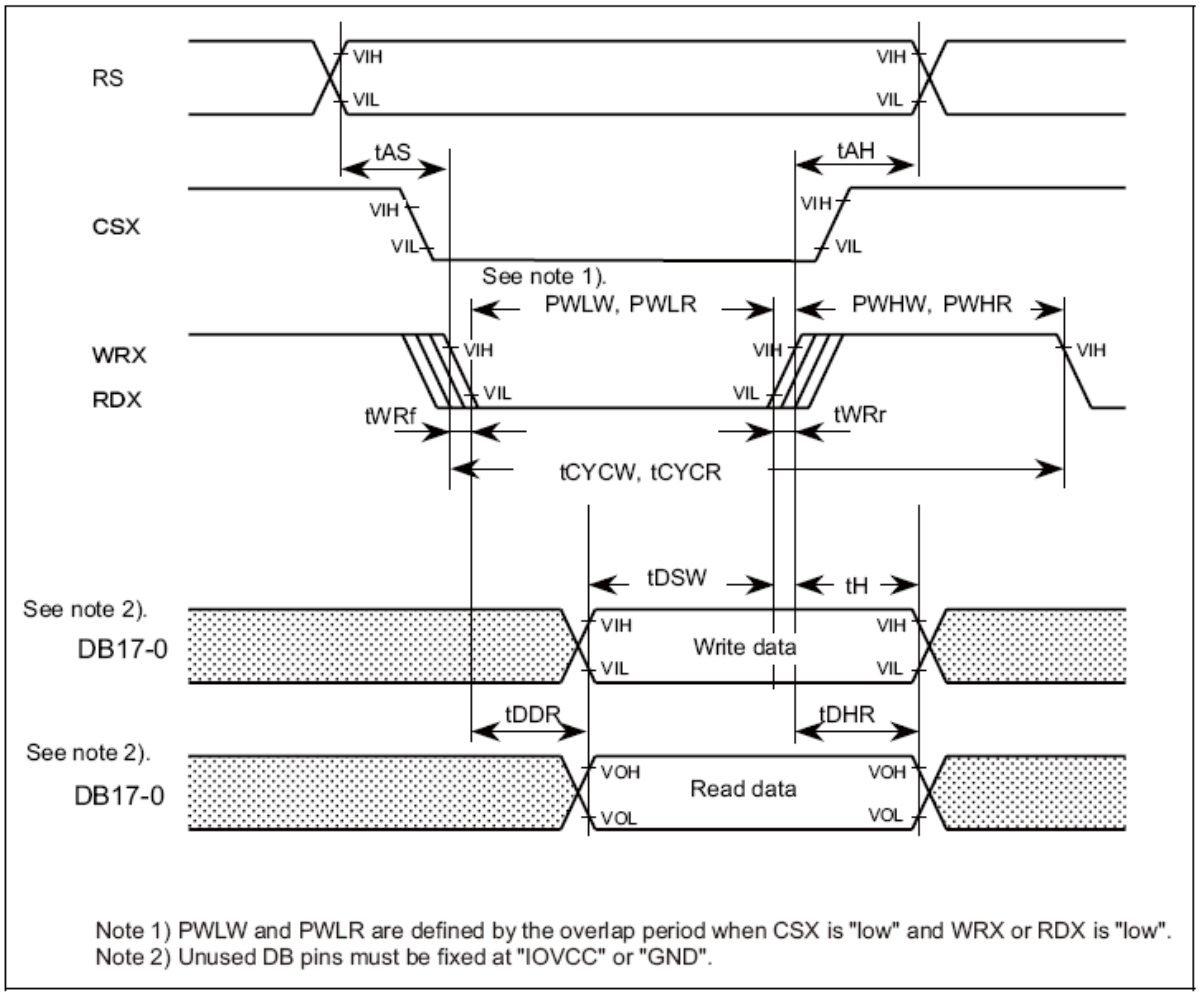
Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input "High" level voltage 1 Except RESETX pin	V_{IH1}	V	IOVCC=1.65V～3.30V	0.80× IOVCC	—	IOVCC	2, 3
Input "Low" level voltage 1 Except RESETX pin	V_{IL1}	V	IOVCC=1.65V～3.30V	-0.3	—	0.20× IOVCC	2, 3
Input "High" level voltage 2 RESETX pin	V_{IH2}	V	IOVCC=1.65V～3.30V	0.90× IOVCC	—	IOVCC	2, 3
Input "Low" level voltage 2 RESETX pin	V_{IL2}	V	IOVCC=1.65V～3.30V	-0.3	—	0.10× IOVCC	2, 3
Output "High" level voltage 1 (DB0-17, FMARK)	V_{OH}	V	IOVCC=1.65V～3.30V, IOH=-0.1mA	0.8× IOVCC	—	—	2
Output "Low" level voltage 1 (DB0-17, FMARK)	V_{OL}	V	IOVCC=1.65V～3.30V, IOL=0.1mA	—	—	0.20× IOVCC	2
Input/Output leakage current	I_{LI}	µA	Vin=0～IOVCC	-1	—	1	4
Current consumption ((IOVCC-GND) + (VCC-GND)) Normal operation (260-k color, display operation)	I_{OP1}	MA	fosc=678kHz (320 line drive), IOVCC=VCC=3.00V, fFLM=70Hz, Ta=25℃, Frame memory data: 18'h000000, BLCON=0, See below for other information	—	0.6	**TBD**	5
Current consumption ((IOVCC-GND) + (VCC-GND)) Normal operation (260-k color, display operation), BLC ON	I_{OP1}	mA	fosc=678kHz (320 line drive), IOVCC=VCC=3.00V, fFLM=70Hz, Ta=25℃, Frame memory data: 18'h000000, BLCON=1, See below for other information	—	0.8	**TBD**	5
Current consumption ((IOVCC-GND) + (VCC-GND)) 8-color mode (64 line partial display operation)	I_{op2}	µA	fosc=678kHz (64 line partial display operation), IOVCC=VCC=3.00V, fFLM=40Hz, Ta=25℃, Frame memory data: 18h'000000, BLCON=0, See below for other information	—	140	—	5
Current consumption ((IOVCC-GND) + (VCC-GND)) Deep standby mode	I_{DST}	µA	IOVCC=VCC=3.00V, Ta=25℃	—	0.1	**TBD**	5

DC Characteristics 2: Step-up circuit characteristics

Item		Unit	Test condition	Min.	Typ.	Max.	Note
Step-up output voltage	DDVDH	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25℃, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h3, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, No load on the panel, Iload1=-3 [mA]	4.8	5.1	-	
	VGH	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25℃, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h3, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload2=-100[uA], No load on the panel	14.4	15.1	-	
	VGL	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25℃, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h3, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload3=+100[uA], No load on the panel	-	-10.0	-9.6	
	VCL	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25℃, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h3, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload4=+200[uA], No load on the panel	-	-2.55	-2.4	

6.3 TIMING CHARACTERISTICS

80-System Bus Interface



Note 1) PWLW and PWLR are defined by the overlap period when CSX is "low" and WRX or RDX is "low".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".

80-System Bus Interface Timing Characteristics (9-/8-bit Interface)

Table 104 (IOVCC=1.65V ~ 3.30V) (T.B.D.)

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	Figure A	70	–	–
	Read	t_{CYCR}	ns	Figure A	450	–	–
Write low-level pulse width		PW_{LW}	ns	Figure A	30	–	–
Read low-level pulse width		PW_{LR}	ns	Figure A	170	–	–
Write high-level pulse width		PW_{HW}	ns	Figure A	25	–	–
Read high-level pulse width		PW_{HR}	ns	Figure A	250	–	–
Write / Read rise/ fall time		t_{WRr}, $_{WRf}$	ns	Figure A	–	–	25
Setup time	Write (RS to CSX, WRX)	t_{AS}	ns	Figure A	0	–	–
	Read (RS to CSX, RDX)		ns	Figure A	10	–	–
Address hold time		t_{AH}	ns	Figure A	2	–	–
Write data setup time		t_{DSW}	ns	Figure A	25	–	–
Write data hold time		t_H	ns	Figure A	10	–	–
Read data delay time		t_{DDR}	ns	Figure A	–	–	150
Read data hold time		t_{DHR}	ns	Figure A	5	–	–

Note: The above values are target values. They are subject to change.

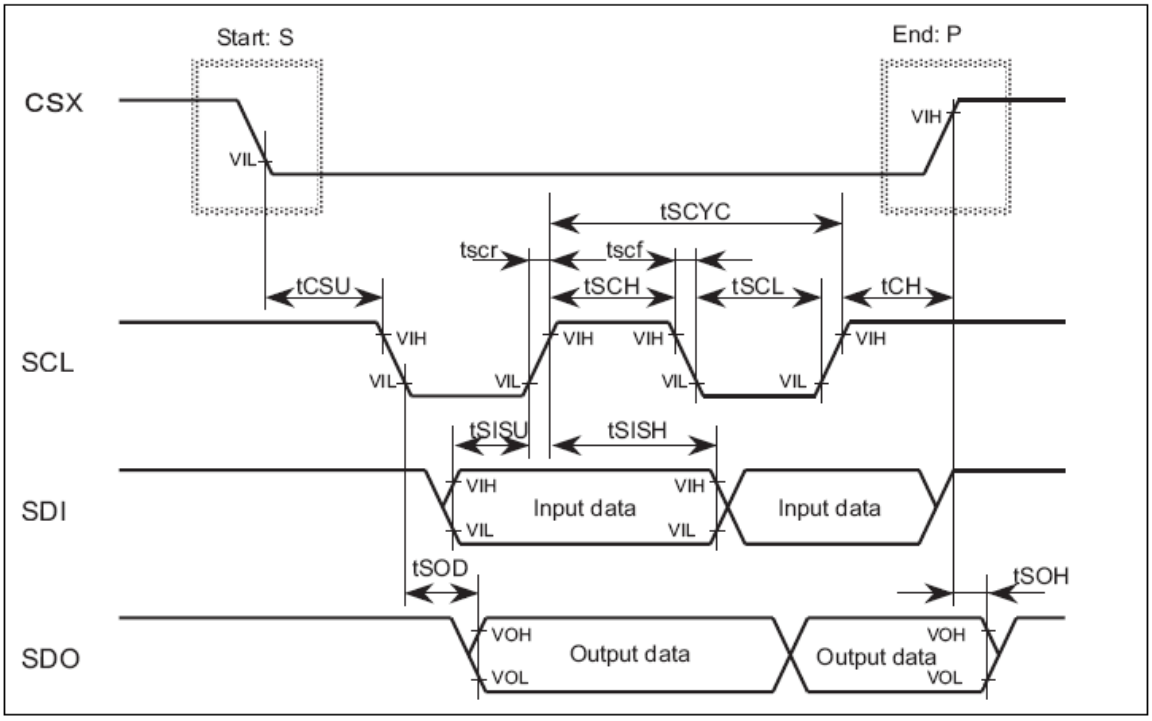
80-System Bus Interface Timing Characteristics (18-/16-bit Interface)

Table 103 (IOVCC=1.65V ~ 3.30V) (T.B.D.)

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	Figure A	75	-	-
	Read	t_{CYCR}	ns	Figure A	450	-	-
Write low-level pulse width		PW_{LW}	ns	Figure A	40	-	-
Read low-level pulse width		PW_{LR}	ns	Figure A	170	-	-
Write high-level pulse width		PW_{HW}	ns	Figure A	25	-	-
Read high-level pulse width		PW_{HR}	ns	Figure A	250	-	-
Write / Read rise/ fall time		t_{WRr}, $_{WRf}$	ns	Figure A	-	-	25
Setup time	Write (RS to CSX, WRX)	t_{AS}	ns	Figure A	0	-	-
	Read (RS to CSX, RDX)		ns	Figure A	10	-	-
Address hold time		t_{AH}	ns	Figure A	2	-	-
Write data setup time		t_{DSW}	ns	Figure A	25	-	-
Write data hold time		t_H	ns	Figure A	10	-	-
Read data delay time		t_{DDR}	ns	Figure A	-	-	150
Read data hold time		t_{DHR}	ns	Figure A	5	-	-

Note: The above values are target values. They are subject to change.

Clock Synchronous Serial Interface



Clock Synchronous Serial Interface Timing Characteristics

Table 105 (IOVCC=1.65V ~ 3.30V) (T.B.D.)

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (receive)	t_{SCYC}	ns	Figure B	100	–	20,000
	Read (transmit)	t_{SCYC}	ns	Figure B	350	–	20,000
Serial clock high-level width	Write (receive)	t_{SCH}	ns	Figure B	40	–	–
	Read (transmit)	t_{SCH}	ns	Figure B	150	–	–
Serial clock low-level width	Write (receive)	t_{SCL}	ns	Figure B	40	–	–
	Read (transmit)	t_{SCL}	ns	Figure B	150	–	–
Serial clock rise/fall time		t_{SCr}, t_{SCf}	ns	Figure B	–	–	20
Chip select setup time		t_{CSU}	ns	Figure B	20	–	–
Chip select hold time		t_{CH}	ns	Figure B	60	–	–
Serial input data setup time		t_{SISU}	ns	Figure B	30	–	–
Serial input data hold time		t_{SISH}	ns	Figure B	30	–	–
Serial output data delay time		t_{SOD}	ns	Figure B	–	–	130
Serial output data hold time		t_{SOH}	ns	Figure B	5	–	–

Note: The above values are target values. They are subject to change.

7. PIN DESCRIPTION

Pin No.	Symbol	Description
1	NC	NC
2	LEDA	Backlight LED anode
3	LEDK1	Backlight LED cathode(K1)
4	LEDK2	Backlight LED cathode(K2)
5	LEDK3	Backlight LED cathode(K3)
6	LEDK4	Backlight LED cathode(K4)
7	IM0	Select the MPU system interface mode
8	IM1	
9	IM2	
10	/RESET	L: initialization is executed
11-18	DB[17:10]	Data bus
19-26	DB[8:1]	Data bus
27	SDO	SPI interface output pin
28	SDI	SPI interface input pin
29	/RD	I80 system:Serves as a read signal and reads data at the low level
30	/WR/SCL	I80 system:Serves as a write signal and writes data at the risong edge SPI Mode:Synchronizing clock signal in SPI mode
31	RS	L:Command;H:display data
32	/CS	L:Chip Selected H:Chip Unselected
33	VCC	I/O interface supply voltage
34	GND	Ground
35	VCI	Analog power supply voltage
36	NC	NC
37	NC	NC
38	NC	NC
39	NC	NC
40	NC	NC

	8bit DB[17:10]	16bit DB[17:10],DB[8:1]	SPI
IM0	1	0	0
IM1	1	1	0
IM2	0	0	1

8. INSTRUCTION DESCRIPTION

●R61580 Instruction List

Major category		Minor category		Upper Code								Lower Code								Note
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
–	Index	—	Index	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID21	ID0	
0*	Display Control	00h	Device Code Read	ALMID1[7]	ALMID1[6]	ALMID1[5]	ALMID1[4]	ALMID1[3]	ALMID1[2]	ALMID1[1]	ALMID1[0]	ALMID0[7]	ALMID0[6]	ALMID0[5]	ALMID0[4]	ALMID0[3]	ALMID0[2]	ALMID0[1]	ALMID0[0]	
			(Default)	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	
		01h	Driver Output Control						SM		SS									
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		02h	LCD Driving Wave Control							BC0									NW[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		03h	Entry Mode	TRIREG	DFM		BGR					ORG		I/D[1]	I/D[0]	AM				
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	
		07h	Display Control 1				PTDE				BASEE					COL				
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		08h	Display Control 2	FP0[7]	FP0[6]	FP0[5]	FP0[4]	FP0[3]	FP0[2]	FP0[1]	FP0[0]	BP0[7]	BP0[6]	BP0[5]	BP0[4]	BP0[3]	BP0[2]	BP0[1]	BP0[0]	
			(Default)	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	
		09h	Display Control 3						PTS[2]	PTS[1]	PTS[0]			PTG		ISC[3]	ISC[2]	ISC[1]	ISC[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
		0Ah	Display Control 4													FMARKOE	FMI[2]	FMI[1]	FMI[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Ch	External Display Interface Control 1		ENC[2]	ENC[1]	ENC[0]				RM			DM[1]	DM[0]			RIM[1]	RIM[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Dh	Frame Marker Position								FMP[8]	FMP[7]	FMP[6]	FMP[5]	FMP[4]	FMP[3]	FMP[2]	FMP[1]	FMP[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Eh	VCOM Low Power Control											VEM[1]	VEM[0]					
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Fh	External Display Interface Control 2												VSPL	HSPL		EPL	DPL	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1*	Power Control	10h	Power Control 1						BT[2]	BT[1]	BT[0]			AP[1]	AP[0]		DSTB			
			(Default)	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	
		11h	Power Control 2						DC1[2]	DC1[1]	DC1[0]		DC0[2]	DC0[1]	DC0[0]		VC[2]	VC[1]	VC[0]	
			(Default)	0	0	0	0	0	0	1	0	0	0	1	1	0	1	1	1	
		12h	Power Control 3				VRH[0]				VCMR	1		PSON	PON	VRH[4]	VRH[3]	VRH[2]	VRH[1]	
			(Default)	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	
		13h	Power Control 4				VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]									
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
2*	Frame Memory Access Control	20h	Frame Memory Address Set (Horizontal Address)									AD[7]	AD[6]	AD[5]	AD[4]	AD[3]	AD[2]	AD[1]	AD[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		21h	Frame Memory Address Set (Vertical Address)								AD[16]	AD[15]	AD[14]	AD[13]	AD[12]	AD[11]	AD[10]	AD[9]	AD[8]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		22h	Frame Memory Data Write/Read	Frame memory write data WD[17:0] are transferred via different data bus in different interface operations.																
	NVM Write Control	28h	NVM Data Read 1									ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
		29h	NVM Data Read 2										VCM1[6]	VCM1[5]	VCM1[4]	VCM1[3]	VCM1[2]	VCM1[1]	VCM1[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
		2Ah	NVM Data Read 3									VCMSEL	VCM2[6]	VCM2[5]	VCM2[4]	VCM2[3]	VCM2[2]	VCM2[1]	VCM2[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
3*	Gamma Control	30h	Gamma Control 1				PR0P01[4]	PR0P01[3]	PR0P01[2]	PR0P01[1]	PR0P01[0]				PR0P00[4]	PR0P00[3]	PR0P00[2]	PR0P00[1]	PR0P00[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		31h	Gamma Control 2	PR0P04[3]	PR0P04[2]	PR0P04[1]	PR0P04[0]	PR0P03[3]	PR0P03[2]	PR0P03[1]	PR0P03[0]				PR0P02[4]	PR0P02[3]	PR0P02[2]	PR0P02[1]	PR0P02[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		32h	Gamma Control 3				PR0P06[4]	PR0P06[3]	PR0P06[2]	PR0P06[1]	PR0P06[0]					PR0P05[3]	PR0P05[2]	PR0P05[1]	PR0P05[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		33h	Gamma Control 4				PR0P08[4]	PR0P08[3]	PR0P08[2]	PR0P08[1]	PR0P08[0]				PR0P07[4]	PR0P07[3]	PR0P07[2]	PR0P07[1]	PR0P07[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		34h	Gamma Control 5			PIR0P3[1]	PIR0P3[0]			PIR0P2[1]	PIR0P2[0]			PIR0P1[1]	PIR0P1[0]			PIR0P0[1]	PIR0P0[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		35h	Gamma Control 6				PR0N01[4]	PR0N01[3]	PR0N01[2]	PR0N01[1]	PR0N01[0]				PR0N00[4]	PR0N00[3]	PR0N00[2]	PR0N00[1]	PR0N00[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		36h	Gamma Control 7	PR0N04[3]	PR0N04[2]	PR0N04[1]	PR0N04[0]	PR0N03[3]	PR0N03[2]	PR0N03[1]	PR0N03[0]				PR0N02[4]	PR0N02[3]	PR0N02[2]	PR0N02[1]	PR0N02[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		37h	Gamma Control 8				PR0N06[4]	PR0N06[3]	PR0N06[2]	PR0N06[1]	PR0N06[0]					PR0N05[3]	PR0N05[2]	PR0N05[1]	PR0N05[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		38h	Gamma Control 9				PR0N08[4]	PR0N08[3]	PR0N08[2]	PR0N08[1]	PR0N08[0]				PR0N07[4]	PR0N07[3]	PR0N07[2]	PR0N07[1]	PR0N07[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		39h	Gamma Control 10			PIR0N3[1]	PIR0N3[0]			PIR0N2[1]	PIR0N2[0]			PIR0N1[1]	PIR0N1[0]			PIR0N0[1]	PIR0N0[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
5*	Window Address Control	50h	Window Horizontal Frame Memory Address (Start Address)									HSA[7]	HSA[6]	HSA[5]	HSA[4]	HSA[3]	HSA[2]	HSA[1]	HSA[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		51h	Window Horizontal Frame Memory Address (End Address)									HEA[7]	HEA[6]	HEA[5]	HEA[4]	HEA[3]	HEA[2]	HEA[1]	HEA[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	
		52h	Window Vertical Frame Memory Address (Start Address)								VSA[8]	VSA[7]	VSA[6]	VSA[5]	VSA[4]	VSA[3]	VSA[2]	VSA[1]	VSA[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		53h	Window Vertical Frame Memory Address (End Address)								VEA[8]	VEA[7]	VEA[6]	VEA[5]	VEA[4]	VEA[3]	VEA[2]	VEA[1]	VEA[0]	
			(Default)	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	
6*	Base Image Display Control	60h	Driver Output Control	GS		NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]			SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]	
			(Default)	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	
		61h	Base Image Display Control														NDL	VSSON	INVON	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		6Ah	Vertical Scroll Control								VL[8]	VL[7]	VL[6]	VL[5]	VL[4]	VL[3]	VL[2]	VL[1]	VL[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
8*	Partial Display Control	80h	Partial Image Display Position								PTDP[8]	PTDP[7]	PTDP[6]	PTDP[5]	PTDP[4]	PTDP[3]	PTDP[2]	PTDP[1]	PTDP[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		81h	Partial Image Frame Memory Address (Start Line Address)								PTSA[8]	PTSA[7]	PTSA[6]	PTSA[5]	PTSA[4]	PTSA[3]	PTSA[2]	PTSA[1]	PTSA[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		82h	Partial Image Frame Memory Address (End Line Address)								PTEA[8]	PTEA[7]	PTEA[6]	PTEA[5]	PTEA[4]	PTEA[3]	PTEA[2]	PTEA[1]	PTEA[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

9*	Panel Interface Control	90h	Panel Interface Control 1							DIVE[1]	DIVE[0]				RTN[4]	RTN[3]	RTN[2]	RTN[1]	RTN[0]
			(Default)	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1
		91h	Panel Interface Control 1-1													SPCW[3]	SPCW[2]	SPCW[1]	SPCW[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		92h	Panel Interface Control 2						NOWI[2]	NOWI[1]	NOWI[0]								
			(Default)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		93h	Panel Interface Control 3						VEQWI[2]	VEQWI[1]	VEQWI[0]						MCPI[2]	MCPI[1]	MCPI[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		94h	Panel Interface Control 4														SDTI[2]	SDTI[1]	SDTI[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		95h	Panel Interface Control 5							DIVE[1]	DIVE[0]			RTNE[5]	RTNE[4]	RTNE[3]	RTNE[2]	RTNE[1]	RTNE[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
		96h	Panel Interface Control 5-1													SPCWE[3]	SPCWE[2]	SPCWE[1]	SPCWE[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		97h	Panel Interface Control 6						NOWE[2]	NOWE[1]	NOWE[0]								
			(Default)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		98h	Panel Interface Control 7						VEQWE[2]	VEQWE[1]	VEQWE[0]						MCPE[2]	MCPE[1]	MCPE[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		99h	Panel Interface Control 8														SDTE[2]	SDTE[1]	SDTE[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		9Ch	Panel Interface Control 9										PCDIVH[2]	PCDIVH[1]	PCDIVH[0]		PCDIVL[2]	PCDIVL[1]	PCDIVL[0]
			(Default)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1
A*	NVM Control	A0h	NVM Control 1									FTT		OP[1]	OP[0]			NVAD[1]	NVAD[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A1h	NVM Control 2	ED[15]	ED[14]	ED[13]	ED[12]	ED[11]	ED[10]	ED[9]	ED[8]	ED[7]	ED[6]	ED[5]	ED[4]	ED[3]	ED[2]	ED[1]	ED[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A3h	NVM Control 3											VERIFLGER	VERIFLGWR	RTY RTL [3]	RTY RTL [2]	RTY RTL [1]	RTY RTL [0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A4h	NVM Control 4																CALB
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C*	Back Light Control	C0h	Back Light Control 1															BLCM	BLCON
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		C1h													THREW0[4]	THREW0[3]	THREW0[2]	THREW0[1]	THREW0[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		C2h													THREW1[4]	THREW1[3]	THREW1[2]	THREW1[1]	THREW1[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		C3h												ULMTW0[5]	ULMTW0[4]	ULMTW0[3]	ULMTW0[2]	ULMTW0[1]	ULMTW0[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
		C4h												ULMTW1[5]	ULMTW1[4]	ULMTW1[3]	ULMTW1[2]	ULMTW1[1]	ULMTW1[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
		C5h												LLMTW0[5]	LLMTW0[4]	LLMTW0[3]	LLMTW0[2]	LLMTW0[1]	LLMTW0[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
		C6h												LLMTW1[5]	LLMTW1[4]	LLMTW1[3]	LLMTW1[2]	LLMTW1[1]	LLMTW1[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
		C7h														PITCHW[3]	PITCHW[2]	PITCHW[1]	PITCHW[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
		C8h													CGAPW[4]	CGAPW[3]	CGAPW[2]	CGAPW[1]	CGAPW[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
		C9h													COEFK0[4]	COEFK0[3]	COEFK0[2]	COEFK0[1]	COEFK0[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
		CAh													COEFK1[4]	COEFK1[3]	COEFK1[2]	COEFK1[1]	COEFK1[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
		CBh										TBLMIN[7]	TBLMIN[6]	TBLMIN[5]	TBLMIN[4]	TBLMIN[3]	TBLMIN[2]	TBLMIN[1]	TBLMIN[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		CCh										TBL0[7]	TBL0[6]	TBL0[5]	TBL0[4]	TBL0[3]	TBL0[2]	TBL0[1]	TBL0[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
		CDh										TBL1[7]	TBL1[6]	TBL1[5]	TBL1[4]	TBL1[3]	TBL1[2]	TBL1[1]	TBL1[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
		CEh										TBL2[7]	TBL2[6]	TBL2[5]	TBL2[4]	TBL2[3]	TBL2[2]	TBL2[1]	TBL2[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
		CFh										TBL3[7]	TBL3[6]	TBL3[5]	TBL3[4]	TBL3[3]	TBL3[2]	TBL3[1]	TBL3[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1
D*		D0h										TBL4[7]	TBL4[6]	TBL4[5]	TBL4[4]	TBL4[3]	TBL4[2]	TBL4[1]	TBL4[0]
			(Default)	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0
		D1h										TBL5[7]	TBL5[6]	TBL5[5]	TBL5[4]	TBL5[3]	TBL5[2]	TBL5[1]	TBL5[0]
			(Default)	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1
		D2h										TBL6[7]	TBL6[6]	TBL6[5]	TBL6[4]	TBL6[3]	TBL6[2]	TBL6[1]	TBL6[0]
			(Default)	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0
		D3h										TBL7[7]	TBL7[6]	TBL7[5]	TBL7[4]	TBL7[3]	TBL7[2]	TBL7[1]	TBL7[0]
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		D5h	Back Light Control 2																PWMON
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		D6h										BDCV[7]	BDCV[6]	BDCV[5]	BDCV[4]	BDCV[3]	BDCV[2]	BDCV[1]	BDCV[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		D7h										PWMDIV[7]	PWMDIV[6]	PWMDIV[5]	PWMDIV[4]	PWMDIV[3]	PWMDIV[2]	PWMDIV[1]	PWMDIV[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
		D8h													PWMWM	LEDPWME	LEDPWMPOL		DIMON
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DAh	Back Light Control 3									RDPWM[7]	RDPWM[6]	RDPWM[5]	RDPWM[4]	RDPWM[3]	RDPWM[2]	RDPWM[1]	RDPWM[0]
			(Default)									0	0	0	0	0	0	0	0

9. BACKLIGHT PARAMETERS

9.1 ABSOLUTE MAXIMUM RATINGS

(Unless specified, The Ambient temperature Ta=25°C)

Item	Symbol	Condition	Rating	Unit
Operating temperature range	Topr		-20~+70	^{0}C
Storage temperature range	Tst		-30~+80	^{0}C

9.2 ELECTRICAL/OPTLCAL CHARACTERISTICS

(Unless specified, The Ambient temperature Ta=25°C)

Item	Symbol	min	typ	max	Unit	Condition
Forward Voltage	Vf	3.0	3.2	3.4	V	If=60mA
Luminance	Lv	3000			cd/m^2	If=60mA
color coordinate	X	0.26		0.30		If=60 mA
	Y	0.26		0.30		

10. Product Quality & Reliability

10.1 Standard for Quality Test

10.1.1 Inspection :
Before delivering, the supplier should take the following tests, and affirm the quality of product.

10.1.2 Electro-Optical Characteristics:
According to the individual specification to test the product.

10.1.3 Test of Appearance Characteristics:
According to the individual specification to test the product.

10.1.4 Test of Reliability Characteristics:
According to the definition of reliability on the specification for testing products.

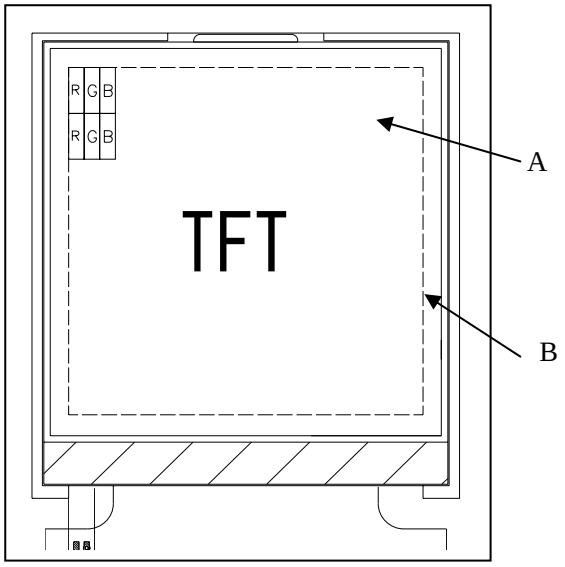
10.1.5 Delivery Test:
Before delivering, the supplier should take the delivery test.
A. Test method: According to GB/2828,General Inspection Level take a single time.
B. The defects classify of AQL as following:
Major defect: AQL=0.25
Minor defect: AQL=1.0
Total defects: AQL=1.0

10.2 Standard for inspection

10.2.1 Manner of appearance test:
a. The test must be under a 40W fluorescent light, and the distance of view must be at 30~35 cm.
b. When test the model of transmissive product must add the reflective plate.
c. The test direction is base on about around 45° of vertical line.

10.2.2 Definition of area: A B

A Area : Viewing area.
B Area : Out of viewing area.(Outside viewing area)

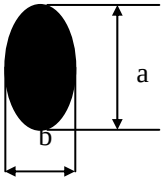


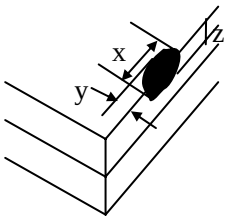
10.2.3 Basic principle:

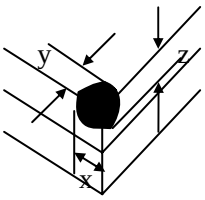
A. In principle the defect out of Area A should be acceptable if the defect does not affect assemblage and the quality of productions.
B. If defects that can not describe clearly, acceptable samples will be the standard.
C. The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.
D. Must add new item on time when it is necessary.

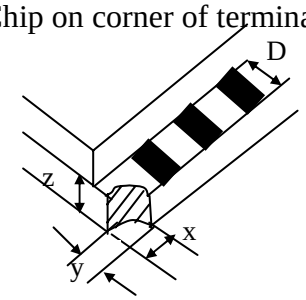
10.2.4 Standard of inspection

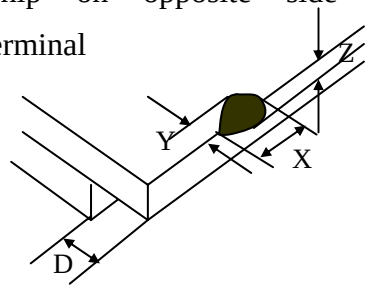
Defect	Inspect item	Criteria
1 Minor	Scratch and fold on polarizer. Scratch on glass. Glass fiber etc. （by bare eyes，defect outside A area is acceptable）	1) width ≤ 0.02 mm length ignore acceptable 2) 0.02 mm<width≤0.05 mm length≤3 mm two are acceptable 3) width>0.05 mm reject

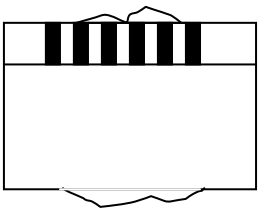
Defect	Inspect item		Criteria
2 Minor	Chip on glass(round type) Chip on polarizer(round type) Air bubble between polarizer and glass  Φ=(a + b)/2		Φ≤0.1mm acceptable 0.1<Φ≤0.2mm two are acceptable 1.The distance between any two dots should be more than 5mm. 2.Defect outside A area is acceptable. 3.If the air bubble is black, it can be judged as black spot.

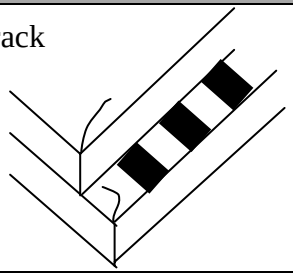
Defect	Inspect item		Criteria
3 Minor	Chip out  x: length y: width z: thickness		x≤3 mm z≤t y≤1/3 s reject t: glass thickness. S: distance between glass edge and inside of edge sealing

Defect	Inspect item		Criteria
4 Minor	Chip on corner of neat edge  X: length Y: width S: width of edge sealing		x≤3 mm y≤3 mm z≤t acceptable any chip exposes the silver dot reject

Defect	Inspect item	Criteria
5 Minor	Chip on corner of terminal edge  D: terminal length	x<0.3 mm or y<0.3 mm ignore x≤3 mm y<D two are acceptable

Defect	Inspect item	Criteria
6 Minor	Chip on opposite side of terminal  	a≥80mm，x≥7mm reject a<80mm， x>5mm reject y>1/2D reject z>1/2t，y>1/4D reject D: terminal length

Defect	Inspect item	Criteria
7 Minor	Cutting/breaking defect (flare) 	According to the dimension of drawing

Defect	Inspect item	Criteria
8 Minor	Crack 	Any crack trend to extend reject

Defect	Inspect item		Criteria
9 Major	Liquid leakage, open sealant		reject

Defect	Inspect item		Criteria
10 Minor	Rainbow		According to samples

Defect	Inspect item		Criteria
11 Major	FPC、TCP、FLEX are broken or not connected firmly		reject

Defect	Inspect item		Criteria
12 Minor	The component on PCB or FPC is missing ,soldered unfirmly or bridged		reject

Defect	Inspect item		Criteria
13 Minor	The soldering tin is not enough		The height that soldering tin covers the bump of component is 1/2 less than the height of bump reject

Defect	Inspect item		Criteria
14 Minor	The soldering tin overflows		The soldering tin covers whole bump reject

Defect	Inspect item		Criteria
15 Minor	The component is broken		reject

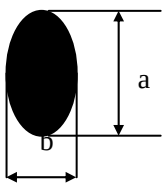
Defect	Inspect item	Criteria
16 Minor	The shape of pinouts is not the same as that in the criterion	It makes the LCM work badly reject

Defect	Inspect item	Criteria
17 Minor	The pinout is broken	reject

Defect	Inspect item	Criteria
18 Minor	The frame is scratched visibly	Length ignore Width >0.5mm reject

Defect	Inspect item	Criteria
19 Minor	The frame is rusted (accumulation)	When the shape is as dot,reference to defect 23 When the shape is as line,reference to defect 24

Defect	Inspect item	Criteria
20 Minor	Scratch and fold on touchpanel. （by bare eyes ,defect outside A area is acceptable）	1) width≤0.02 mm acceptable 2) 0.02 mm<width≤0.05 mm length≤5 mm two are acceptable 3) width>0.05 mm reject

Defect	Inspect item	Criteria
21 Minor	Black & white dots on touchpanel (round type) Air bubble on touchpanel Φ=(a + b)/2 	1) Φ≤0.1 mm acceptable 2) 0.1<Φ≤0.3 mm three are acceptable 3) Φ>0.3 mm reject 1.The distance between any two dots should be more than 5mm. 2.Defect outside A area is acceptable. 3.If the air bubble is black, it can be judged as black spot.

Defect	Inspect item		Criteria
22 Minor	Touchpanel warps		According to the dimension of drawing.

Defect	Inspect item		Criteria
23 Minor	Dirty on rear of touchpanel		It's visible at condition of30±5 cm, 45°

10.3 RELIABILITY

Item	Condition	Criterion
High temperature operation	**70°C， 96 hrs**	**-Cosmetic defects are not allowed after the test(Polarizer change is exceptional)** **-Contrast ratio change over 50% of initial value should not be happened** **-The current consumption should be below double of initial value** **-Brightness decrease should be lower than 50% of initial value**
Low temperature operation	**-20°C， 96 hrs**	
Moisture storage	**60°C，90%RH, 96 hrs**	
High temperature storage	**80°C， 96 hrs**	
Low temperature storage	**-30°C， 96 hrs**	
Thermal shock	**-30°C (30 minute)** **25°C (5 minute)** **80°C (30 minute)** **CYCLES: 10**	
LIFE TIME	**50,000 hours, 25±10°C, 45±20% RH**	

11. PRECAUTIONS IN USING

11.1 Liquid crystal display (LCD)

The LCD panel is made up of glass, organic fluid and polarizer. When handling, please pay attention to the following items:

1) Keep the operation and storage temperature of the LCD within the range specified in the LCD specification. Otherwise, excessive temperature and humidity would cause polarization degradation, bubble generation or polarizer peel-off.
2) Prevent it from mechanical shock by dropping it from a high place, etc.
3) Don't contact, push or rub the exposed polarizers with anything harder than HB pencil lead.
4) Avoid using chemicals such as acetone, toluene, ethanol and isoropylalcohol to clean the front/rear polarizers and reflectors, which will cause damage to them.
5) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause deformation or color fading. The LCM is assembled and adjusted with a high degree of precision.
6) Do not put or attach anything on the display area. Avoid touching the display area with bare hand.

11.2 Precaution for handling LCD modules

The LCM is assembled and adjusted with a high degree of precision, do not applying excessive shocks to it or making any alterations or modifications to it, the following precautions should be taken when handing.

1) Do not drop, bend or twist the module.
2) Do not alter or making any modification on the shape of the metal frame.
3) Do not change the shape, the pattern wiring or add any extra hole on the PCB.
4) Do not modify or touch the zebra rubber strip(conductive rubber) with another object.
5) Do not change the positions of components on the PCB.

11.3 Eletro-static discharge control

Careful attention should be paid to control the electrostatic discharge of the modules, since the modules contain no. of CMOS LSI.

1) Make sure you are grounded properly when remove the module from its antistatic bag. Be sure that the module and have the same electric potential.
2) Only properly grounded soldering iron should be used.
3) Modules should be stored in antistatic bag or other containers resistant to static after remove from its original package.
4) When using the electric screw-driver is used, make sure the screw driver had been ground potentiality to minimize the transmission of EM wave produced by commutator sparks.
5) In order to reduce the generation of static electricity, a relative humidity of 50-60% is recommended.

11.4 Precaution for soldering

1) Soldering should apply to I/O terminals only.
2) Soldering temperature is 280°C+(-)10°C.
3) Soldering time 3-4 seconds.
4) Eutectic solder (rosin flux filled) should be used.
5) If soldering flux is used, be sure to remove any remaining flux after finishing the soldering operation and LCD surface should be covered during soldering to prevent any damage to flux spatters.
6) When remove the lead wires from the I/O terminals, use proper de-soldering methods, e.g. suction type de-soldering irons. Do not repeat wiring by soldering more than three times at the pads and plated though holes may be damaged.

11.5 Precaution for operation

1) Adjust liquid crystal driving voltage (Vo) to varies viewing angle and obtain the contrast.
2) Vo should be kept in proper range stated in the specification. Excess voltage will shorten the LCD life.
3) Response time is greatly delayed at low temperature. It will recover when go back to normal temperature.
4) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore it should be used under the relative condition of 50% RH.

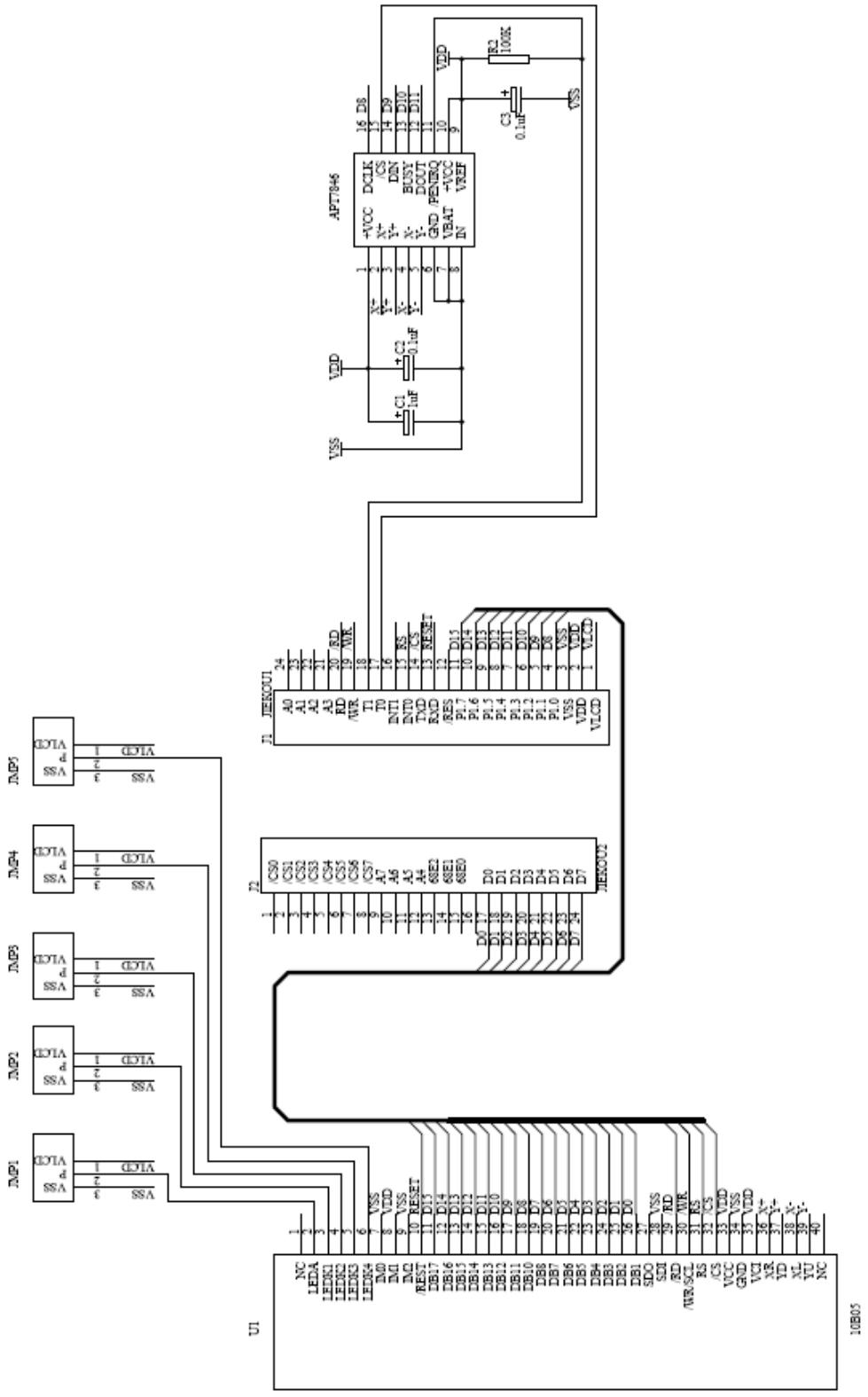
11.6 Storage

When long term storage is required, following precautions are necessary:

1) Storage them in a sealed polyethylene bag (antistatic), seal the opening, and store it where it is not subjected to direct sunshine, or to the light of fluorescent lamp. If properly sealed, there is no need for desiccant.
2) Store them in the temperature range of -30°C~80°C and at low humidity is recommended.

12. APPLICATION

12.1 REFERENCE CIRCUIT



12.2 APPENDIX

INITIALIZATION FOR REFERENCE (MPU: AT89C512):

```
void    LCD_Init()
{
LCD_CtrlWrite(0x00);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x00);LCD_DataWrite(0x0000);
delay(100);
LCD_CtrlWrite(0x00);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x00);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x00);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x00);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0xA4);LCD_DataWrite(0x0001);
delay(100);
LCD_CtrlWrite(0x60);LCD_DataWrite(0xA700);
LCD_CtrlWrite(0x08);LCD_DataWrite(0x0808);
/*********************************************/
//Gamma Setting:
LCD_CtrlWrite(0x30);LCD_DataWrite(0x0203);
LCD_CtrlWrite(0x31);LCD_DataWrite(0x080F);
LCD_CtrlWrite(0x32);LCD_DataWrite(0x0401);
LCD_CtrlWrite(0x33);LCD_DataWrite(0x050B);
LCD_CtrlWrite(0x34);LCD_DataWrite(0x3330);
LCD_CtrlWrite(0x35);LCD_DataWrite(0x0B05);
LCD_CtrlWrite(0x36);LCD_DataWrite(0x0005);
LCD_CtrlWrite(0x37);LCD_DataWrite(0x0F08);
LCD_CtrlWrite(0x38);LCD_DataWrite(0x0302);
LCD_CtrlWrite(0x39);LCD_DataWrite(0x3033);
/*********************************************/
//Power Setting:
LCD_CtrlWrite(0x90);LCD_DataWrite(0x0018);//80Hz
LCD_CtrlWrite(0x10);LCD_DataWrite(0x0530);//BT,AP
LCD_CtrlWrite(0x11);LCD_DataWrite(0x0237);//DC1,DC0,VC
LCD_CtrlWrite(0x12);LCD_DataWrite(0x01BF);
LCD_CtrlWrite(0x13);LCD_DataWrite(0x1000);//VCOM
delay(200);
/*********************************************/
LCD_CtrlWrite(0x01);LCD_DataWrite(0x0100);
LCD_CtrlWrite(0x02);LCD_DataWrite(0x0200);
LCD_CtrlWrite(0x03);LCD_DataWrite(0x1030);
LCD_CtrlWrite(0x09);LCD_DataWrite(0x0001);
LCD_CtrlWrite(0x0A);LCD_DataWrite(0x0008);
LCD_CtrlWrite(0x0C);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x0D);LCD_DataWrite(0xD000);
LCD_CtrlWrite(0x0E);LCD_DataWrite(0x0030);
LCD_CtrlWrite(0x0F);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x20);LCD_DataWrite(0x0000);//H Start
LCD_CtrlWrite(0x21);LCD_DataWrite(0x0000);//V Start
LCD_CtrlWrite(0x29);LCD_DataWrite(0x002E);
LCD_CtrlWrite(0x50);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x51);LCD_DataWrite(0x00EF);
LCD_CtrlWrite(0x52);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x53);LCD_DataWrite(0x013F);
LCD_CtrlWrite(0x61);LCD_DataWrite(0x0001);
LCD_CtrlWrite(0x6A);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x80);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x81);LCD_DataWrite(0x0000);
LCD_CtrlWrite(0x82);LCD_DataWrite(0x005F);
LCD_CtrlWrite(0x93);LCD_DataWrite(0x0701);
/*********************************************/
LCD_CtrlWrite(0x07);LCD_DataWrite(0x0100);
delay(100);
}
```