DISPLAY Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 135240B VMH-PW-N

1,14“ TFT

Product Specification **Ver.: 2**

13.03.2024

REVISION HISTORY:				
Rev	Date	Description	Written By	Approved By
1.0	28.02.2024	New Release	YCW	LSB
2.0	13.03.2024	1) Item 3.0 Remove logo in module drawing; 2) Item 10.0: Add backlight life time; 3) Item 16.0: correct the datecoding rule.	YCW	LSB

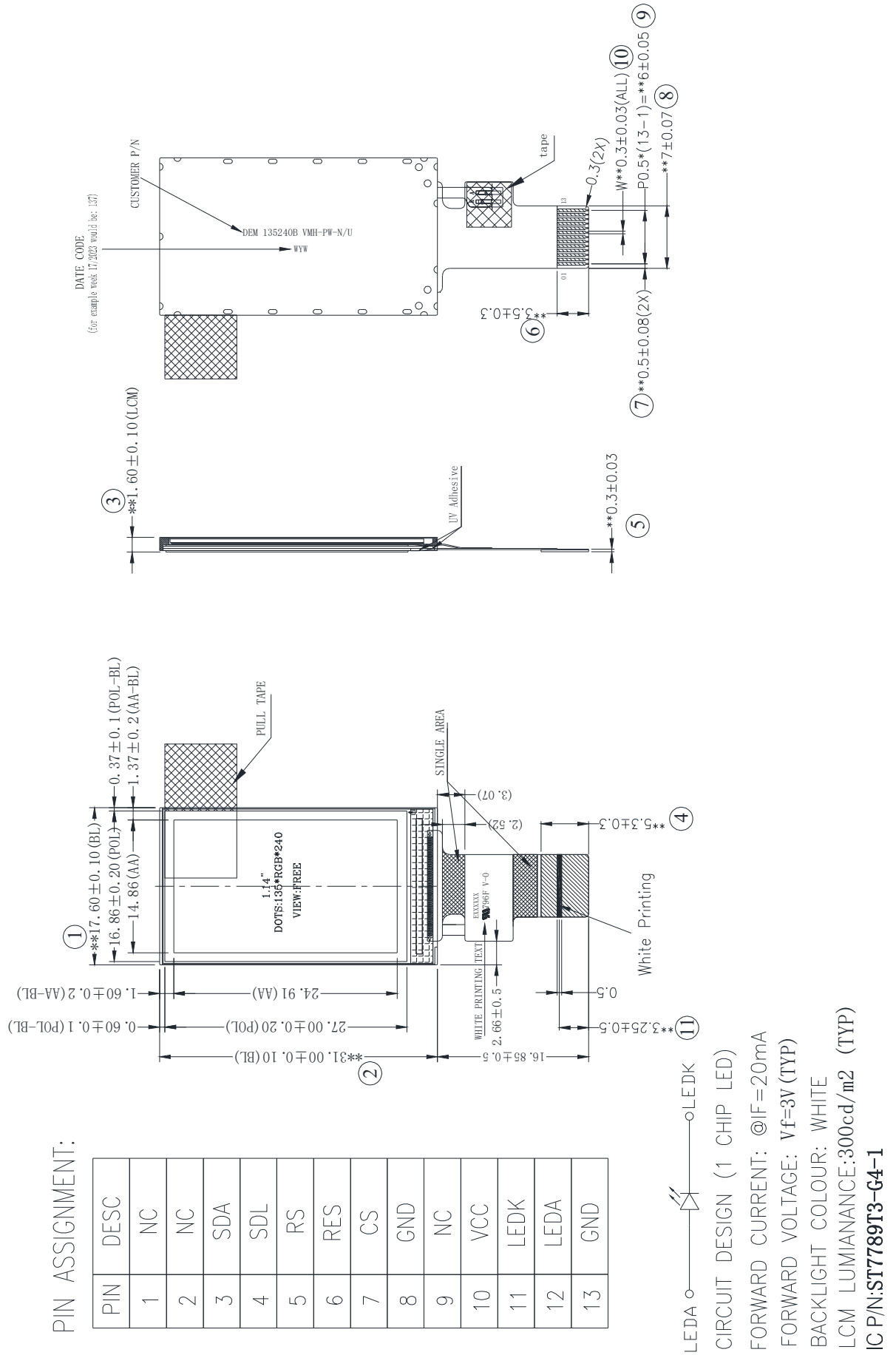
CONTENTS

1.0 GENERAL SPECIFICATION

Item	Contents	Unit
Display Mode	1.14” TFT Transmissive / IPS Normally black	-
Module Outer Dimension	17.60 x 31.00 x 1.60 (Excluded FPC length)	mm
Pixel Size	0.1101 x 0.1038	mm
Effective Display Area	14.86 x 24.91	mm
Number of Dots	135 RGB x 240	dots
Viewing Direction	Free	O’ clock
Pixel Arrangement	RGB Stripe	-
Backlight	LED	-
Driver IC	ST7789T3-G4-1	-
Interface Type	4-line SPI	-
Number Of Colors	262 K	-
Operating Temperature	-20 ~ 70	°C
Storage Temperature	-30 ~ 80	°C

Remarks: Normal operating condition is temperature 15~35°C, humidity 45%~75%RH, atmospheric pressure 86~106kPa.

2.0 OUTLINE DRAWING



PIN ASSIGNMENT:

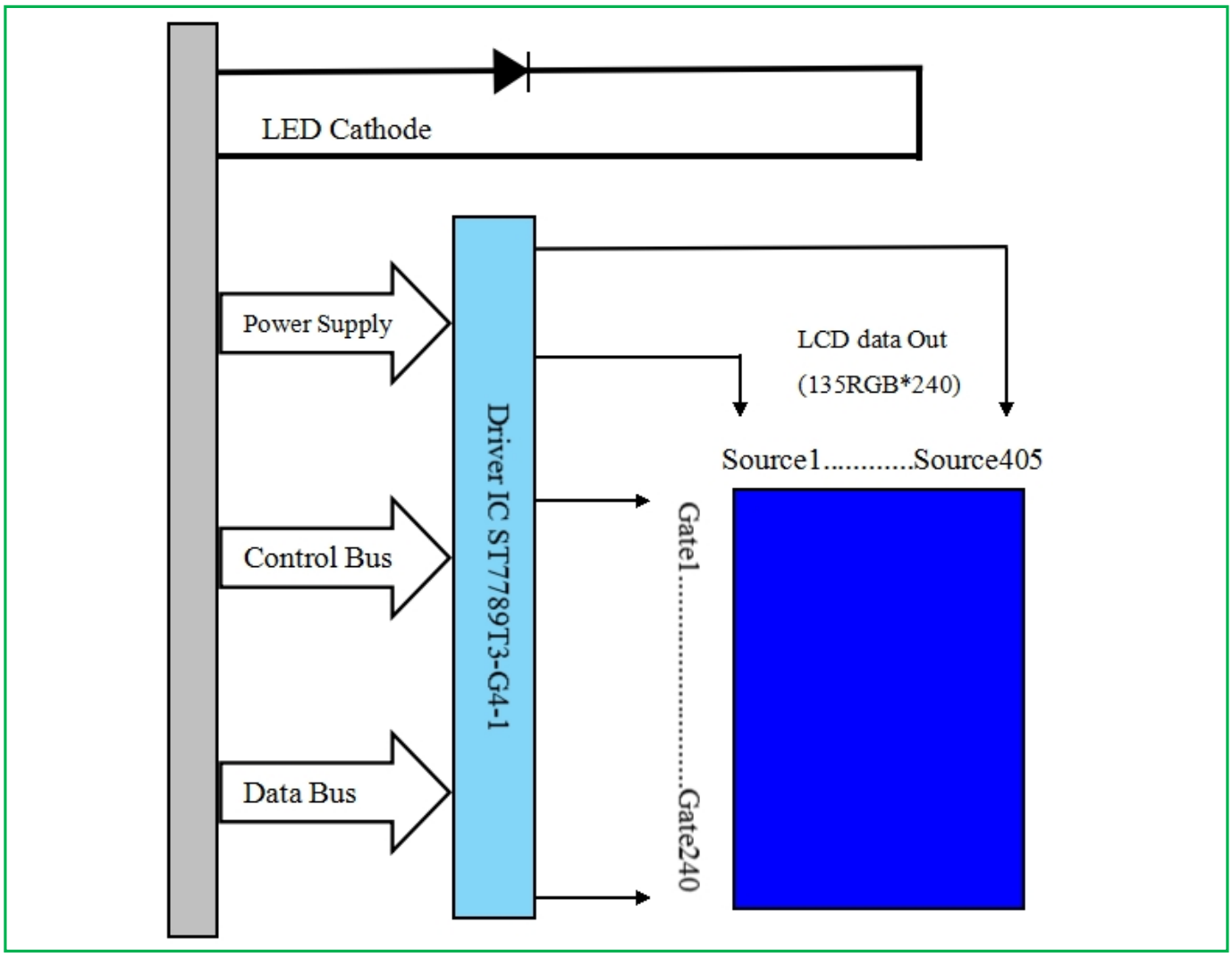
PIN	DESC
1	NC
2	NC
3	SDA
4	SDL
5	RS
6	RES
7	CS
8	GND
9	NC
10	VCC
11	LEDK
12	LEDA
13	GND

CIRCUIT DESIGN (1 CHIP LED)
FORWARD CURRENT: @IF=20mA
FORWARD VOLTAGE: Vf=3V(TYP)
BACKLIGHT COLOUR: WHITE
LCM LUMIANANCE:300cd/m2 (TYP)
IC P/N:**ST7789T3-G4-1**

3.0 INTERFACE PIN DESCRIPTION

Pin No.	Symbol	Pin Description
1	NC	No connection.
2	NC	No connection.
3	SDA	SPI DATA IN
4	SDL	SPI CLOCK
5	RS	Display data/command selection pin in 4-line serial interface
6	RES	This signal will reset the device and it must be applied to properly initialize the chip
7	CS	Chip selection pin
8	GND	Ground
9	NC	No connection.
10	VCC	Power support
11	LEDK	LED backlight cathode.
12	KEDA	LED backlight anode.
13	GND	Ground

4.0 BLOCK DIAGRAM



5.0 OPERATING PRINCIPLE & DRIVING METHOD

5.1 Please refer to ST75789T3 (V1.1) IC data sheet.

5.2 Instruction Description (based on IC spec ver as stated in 6.1 where the product is designed). This instruction description is for reference only. Customer is encouraged to always refer to the latest IC specification when developing application system platform.

9.1 System Function Command Table 1

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	0	0		
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	MY	MX	MV	ML	RGB	MH	0	0		-
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		-
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0		-
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	TEON	TEM	0	0	0	0	0	0		-
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	0	↑	1	-	0	0	1	0	0	0	0	1	(26h)	Display inversion on
	1	↑	1	-	0	0	0	0	GC3	GC2	GC1	GC0		
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0≦ XS≦ X
	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	1	↑	1		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start: S≦ XE≦ X
	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0≦ YS≦ Y
	1	↑	1		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
	1	↑	1		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start: S≦ YE≦ Y
	1	↑	1		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial sart/end address set
	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address: (0, 1,2, ..P)
	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0, 1,2, 3, , P)
	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Vertical scrolling definition
	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	1	-	-	-	-	-	-	-	-	TEM		
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0		-
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8		
	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0		Interface format
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRDC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)	Memory read continue
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
TESCAN	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0		
RDTESCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)	Get scanline
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	-	-	-	-	-	-	N9	N8		
	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0		
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)	Write display brightness
	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)	Read display brightness value
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL display
	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0		
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL value dsiplay
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRCACE	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)	Write content adaptive brightness control and Color enhancemnet
	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0		
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)	Read content adaptive brightness control
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	CECTRL	0	0	0	0	C1	C0		
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)	Write CABC minimum brightness
	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)	Read CABC minimum brightness
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	(68h)	Read Automatic Brightness Control Self-Diagnostic Result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

9.2 System Function Command Table 2

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RAMCTRL	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	RAM Control
	1	↑	1	-	0	0	0	RM	0	0	DM1	DM0		
	1	↑	1	-	1	1	EPF1	EPF0	ENDIAN	RIM	MDT1	MDT0		
RGBCTRL	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	RGB Control
	1	↑	1	-	WO	RCM1	RCM0	0	VSPL	HSPL	DPL	EPL		
	1	↑	1	-	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0		
	1	↑	1	-	0	0	0	HBP4	HBP3	HBP2	HBP1	HBP0		
PORCTRL	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	Porch control
	1	↑	1	-	0	BPA6	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0		
	1	↑	1	-	0	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0		
	1	↑	1	-	0	0	0	0	0	0	0	PSEN		
	1	↑	1		BPB3	BPB2	BPB1	BPB0	FPB3	FPB2	FPB1	FPB0		
	1	↑	1		BPC3	BPC2	BPC1	BPC0	FPC3	FPC2	FPC1	FPC0		
FRCTRL1	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	Frame Rate Control 1
	1	↑	1	-	0	0	0	FRSEN	0	0	DIV1	DIV0		
	1	↑	1	-	NLB2	NLB1	NLB0	RTNB4	RTNB3	RTNB2	RTNB1	RTNB0		
	1	↑	1	-	NLC2	NLC1	NLC0	RTNC4	RTNC3	RTNC2	RTNC1	RTNC0		
PARCTRL	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	Partial mode Control
	1	↑	1	-	NDL	0	0	PTGISC	ISC3	ISC2	ISC1	ISC0		
GCTRL	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)	Gate control
	1	↑	1	-	0	VGHS2	VGHS1	VGHS0	0	VGLS2	VGLS1	VGLS0		
GTADJ	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)	Gate on timing adjustment
	1	↑	1	-	0	0	1	0	1	0	1	0		
	1	↑	1	-	0	0	1	0	1	0	1	1		
	1	↑	1	-	0	0	GTA5	GTA4	GTA3	GTA2	GTA1	GTA0		
	1	↑	1	-	GOFR3	GOFR2	GOFR1	GOFR0	GOF3	GOF2	GOF1	GOF0		
DGMEN	0	↑	1	-	1	0	1	1	1	0	1	0	(BAh)	Digital Gamma Enable
	1	↑	1	-	0	0	0	0	0	DGMEN	0	0		
VCOMS	0	↑	1	-	1	0	1	1	1	0	1	1	(BBh)	VCOMS Setting
	1	↑	1	-	0	0	VCOMS5	VCOMS4	VCOMS3	VCOMS2	VCOMS1	VCOMS0		
LCMCTRL	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	LCM Control
	1	↑	1	-	0	XMY	XBGR	XINV	XMX	XMH	XMV	XGS		

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
IDSET	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	ID Setting
	1	↑	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
	1	↑	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
VDVVRHEN	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	VDV and VRH Command Enable
	1	↑	1	-	0	0	0	0	0	0	0	CMDEN		
	1	↑	1	-	1	1	1	1	1	1	1	1		
VRHS	0	↑	1		1	1	0	0	0	0	1	1	(C3h)	VRH Set
	1	↑	1		0	0	VRHS5	VRHS4	VRHS3	VRHS2	VRHS1	VRHS0		
VDVSET	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	VDV Setting
	1	↑	1	-	0	0	VDVS5	VDVS4	VDVS3	VDVS2	VDVS1	VDVS0		
VCMOFSET	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOMS Offset Set
	1	↑	1	-	0	0	VCMOFS5	VCMOFS4	VCMOFS3	VCMOFS2	VCMOFS1	VCMOFS0		
FRCTR2	0	↑	1		1	1	0	0	0	1	1	0	(C6h)	FR Control 2
	1	↑	1		NLA2	NLA1	NLA0	RTNA4	RTNA3	RTNA2	RTNA1	RTNA0		
CABCCTRL	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	CABC Control
	1	↑	1	-	0	0	0	0	LEDONREV	DPOFPWM	PWMFIX	PWMPOL		
REGSEL1	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)	Register value selection1
	1	↑	1	-	0	0	0	0	1	0	0	0		
REGSEL2	0	↑	1	-	1	1	0	0	1	0	1	0	(CAh)	Register value selection2
	1	↑	1	-	0	0	0	0	1	1	1	1		
PWMFRSEL	0	↑	1	-	1	1	0	0	1	1	0	0	(CCh)	PWM Frequency Selection
	1	↑	1	-	0	0	CS2	CS1	CS0	CLK2	CLK1	CLK0		
PWCTRL1	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)	Power Control 1
	1	↑	1	-	1	0	1	0	0	1	0	0		
	1	↑	1	-	AVDD1	AVDD0	AVCL1	AVCL0	0	0	VDS1	VDS0		
VAPVANEN	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Enable VAP/VAN signal output
	1	↑	1	-	0	1	0	0	1	1	0	0		

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
CMD2EN	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	Command 2 Enable
	1	↑	1	-	0	1	0	1	1	0	1	0	(5Ah)	
	1	↑	1	-	0	1	1	0	1	0	0	1	(69h)	
	1	↑	1	-	0	0	0	0	0	0	1	0	(02h)	
	1	↑	1	-	0	0	0	0	0	0	0	EN		
PVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Positive Voltage Gamma Control
	1	↑	1	-	V63P3	V63P2	V63P1	V63P0	V0P3	V0P2	V0P1	V0P0		
	1	↑	1	-	0	0	V1P5	V1P4	V1P3	V1P2	V1P1	V1P0		
	1	↑	1	-	0	0	V2P5	V2P4	V2P3	V2P2	V2P1	V2P0		
	1	↑	1	-	0	0	0	V4P4	V4P3	V4P2	V4P1	V4P0		
	1	↑	1	-	0	0	0	V6P4	V6P3	V6P2	V6P1	V6P0		
	1	↑	1	-	0	0	J0P1	J0P0	V13P3	V13P2	V13P1	V13P0		
	1	↑	1	-	0	V20P6	V20P5	V20P4	V20P3	V20P2	V20P1	V20P0		
	1	↑	1	-	0	V36P2	V36P1	V36P0	0	V27P2	V27P1	V27P0		
	1	↑	1	-	0	V43P6	V43P5	V43P4	V43P3	V43P2	V43P1	V43P0		
	1	↑	1	-	0	0	J1P1	J1P0	V50P3	V50P2	V50P1	V50P0		
	1	↑	1	-	0	0	0	V57P4	V57P3	V57P2	V57P1	V57P0		
	1	↑	1	-	0	0	0	V59P4	V59P3	V59P2	V59P1	V59P0		
	1	↑	1	-	0	0	V61P5	V61P4	V61P3	V61P2	V61P1	V61P0		
	1	↑	1	-	0	0	V62P5	V62P4	V62P3	V62P2	V62P1	V62P0		
NVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Negative Voltage Gamma Control
	1	↑	1	-	V63N3	V63N2	V63N1	V63N0	V0N3	V0N2	V0N1	V0N0		
	1	↑	1	-	0	0	V1N5	V1N4	V1N3	V1N2	V1N1	V1N0		
	1	↑	1	-	0	0	V2N5	V2N4	V2N3	V2N2	V2N1	V2N0		
	1	↑	1	-	0	0	0	V4N4	V4N3	V4N2	V4N1	V4N0		
	1	↑	1	-	0	0	0	V6N4	V6N3	V6N2	V6N1	V6N0		
	1	↑	1	-	0	0	J0N1	J0N0	V13N3	V13N2	V13N1	V13N0		
	1	↑	1		0	V20N6	V20N5	V20N4	V20N3	V20N2	V20N1	V20N0		
	1	↑	1		0	V36N2	V36N1	V36N0	0	V27N2	V27N1	V27N0		

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1		0	V43N6	V43N5	V43N4	V43N3	V43N2	V43N1	V43N0		
	1	↑	1		0	0	J1N1	J1N0	V50N3	V50N2	V50N1	V50N0		
	1	↑	1		0	0	0	V57N4	V57N3	V57N2	V57N1	V57N0		
	1	↑	1		0	0	0	V59N4	V59N3	V59N2	V59N1	V59N0		
	1	↑	1		0	0	V61N5	V61N4	V61N3	V61N2	V61N1	V61N0		
	1	↑	1		0	0	V62N5	V62N4	V62N3	V62N2	V62N1	V62N0		
DGMLUTR	0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)	Digital Gamma Look-up Table for Red
	1	↑	1	-	DGM_LUT_R00[7:0]									
	1	↑	1	-	DGM_LUT_R01[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_R30[7:0]									
	1	↑	1	-	DGM_LUT_R31[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_R62[7:0]									
	1	↑	1	-	DGM_LUT_R63[7:0]									
DGMLUTB	0	↑	1	-	1	1	1	0	0	0	1	1	(E3h)	Digital Gamma Look-up Table for Blue
	1	↑	1	-	DGM_LUT_B00[7:0]									
	1	↑	1	-	DGM_LUT_B01[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_B30[7:0]									
	1	↑	1	-	DGM_LUT_B31[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_B62[7:0]									
	1	↑	1	-	DGM_LUT_B63[7:0]									
GATECTRL	0	↑	1	-	1	1	1	0	0	1	0	0	(E4h)	Gate control
	1	↑	1	-	0	0	NL5	NL4	NL3	NL2	NL1	NL0		
	1	↑	1	-	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0		
	1	↑	1	-	0	0	0	TMG	0	SM	0	GS		
SPI2EN	0	↑	1	-	1	1	1	0	0	1	1	1	(E7h)	SPI2

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	-	0	0	0	SPI2EN	0	0	0	SPIRD		enable
PWCTRL2	0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)	Power
	1	↑	1	-	1	0	SBCLK1	SBCLK0	0	0	STP14CK1	STP14CK0		Control 2
EQCTRL	0	↑	1	-	1	1	1	0	1	0	0	1	(E9h)	
	1	↑	1	-	0	0	0	SEQ4	SEQ3	SEQ2	SEQ1	SEQ0		Equalize
	1	↑	1	-	0	0	0	SPRET4	SPRET3	SPRET2	SPRET1	SPRET0		Time
	1	↑	1	-	0	0	0	0	GEQ3	GEQ2	GEQ1	GEQ0		Control
PROMCTRL	0	↑	1	-	1	1	1	0	1	1	0	0	(ECh)	Program
	1	↑	1	-	0	0	0	0	0	0	0	1		Control
PROMEN	0	↑	1	-	1	1	1	1	1	0	1	0	(FAh)	
	1	↑	1	-	0	1	0	1	1	0	1	0		Program
	1	↑	1	-	0	1	1	0	1	0	0	1		Mode
	1	↑	1	-	1	1	1	0	1	1	1	0		Enable
	1	↑	1	-	0	0	0	0	0	PROMEN	0	0		
NVMSET	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)	
	1	↑	1	-	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0		NVM
	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Setting
PROMACT	0	↑	1	-	1	1	1	1	1	1	1	0	(FEh)	
	1	↑	1	-	0	0	0	1	1	0	0	1		Program
	1	↑	1	-	1	0	1	0	0	1	0	1		Action

5.3 Recommended initial codes

```
void Init_LCM()
{
        Write_command(0x11);

        Delayms(120);

        Write_command(0x36);
        Write_data(0x00);

        Write_command(0x3A);
        Write_data(0x05);

        Write_command(0xB2);
        Write_data(0x1F);
        Write_data(0x1F);
        Write_data(0x00);
        Write_data(0x33);
        Write_data(0x33);

        Write_command(0xB7);
        Write_data(0x65);

        Write_command(0xBB);
        Write_data(0x28);

        Write_command(0xC0);
        Write_data(0x2C);

        Write_command(0xC2);
        Write_data(0x01);

        Write_command(0xC3);
        Write_data(0x13);

        Write_command(0xC4);
        Write_data(0x20);

        Write_command(0xC6);
        Write_data(0x05);       //90Hz
```

```
Write_command(0xD0);
Write_data(0xA4);
Write_data(0xA1);

Write_command(0xD6);
Write_data(0xA1);

Write_command(0xE0);
Write_data(0xF0);
Write_data(0x05);
Write_data(0x0B);
Write_data(0x09);
Write_data(0x08);
Write_data(0x15);
Write_data(0x30);
Write_data(0x44);
Write_data(0x47);
Write_data(0x05);
Write_data(0x10);
Write_data(0x11);
Write_data(0x2D);
Write_data(0x34);

Write_command(0xE1);
Write_data(0xF0);
Write_data(0x08);
Write_data(0x0D);
Write_data(0x0A);
Write_data(0x09);
Write_data(0x07);
Write_data(0x2F);
Write_data(0x33);
Write_data(0x47);
Write_data(0x38);
Write_data(0x13);
Write_data(0x15);
Write_data(0x2F);
Write_data(0x35);

Write_command(0xE4);
Write_data(0x22);
```

```
        Write_data(0x00);
        Write_data(0x00);

        Write_command(0x21);

        Write_command(0x29);

        Write_command(0x2A);      //Column Address Set
        Write_data(0x00);
        Write_data(0x34);
        Write_data(0x00);
        Write_data(0xBF);

        Write_command(0x2B);      //Row Address Set
        Write_data(0x00);
        Write_data(0x28);
        Write_data(0x01);
        Write_data(0x17);

        Write_command(0x2C);
    }
```

Notes:

1) These initial codes are only for reference, Customer should optimize above setting according to the display pattern and application used.
2) Customer is advised to refer to “General Handling Precaution of LCD Modules” section in this product specification regarding the operating precaution of LCD modules, when optimizing the display initialization setting.
3) DISPLAY Elektronik GmbH will use above initial code for production testing by default. Customer is advised to highlight to DISPLAY Elektronik GmbH in case that initial code setting in customer application is different with above initial code. Reason is to ensure DISPLAY Elektronik GmbH testing is in-line with customer application as close as possible for good quality control.

5.4 Power On/Off Sequence

VDDI and VDD can be applied in any order.

In CABC function application, VDDI power on need delay 5ms after VDD has been supplied.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

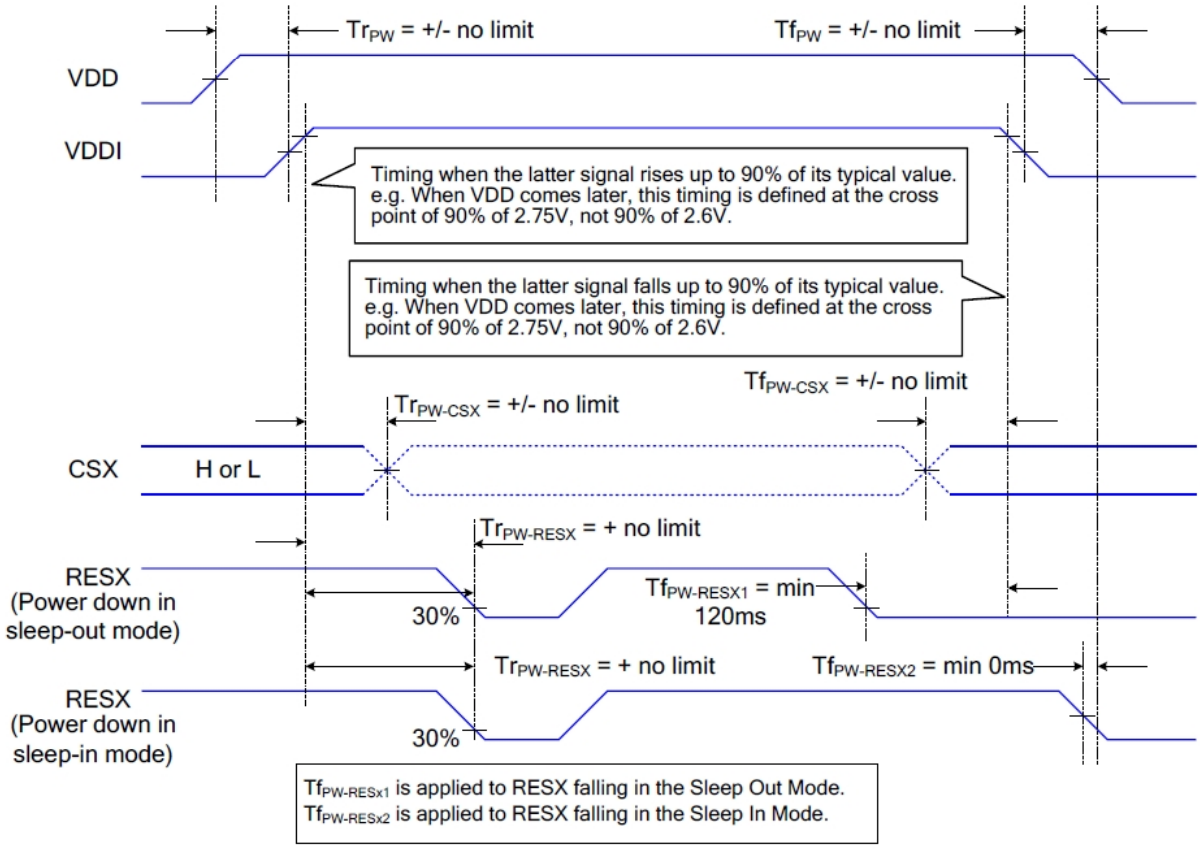
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



8.16.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

5.5 Timing Characteristics

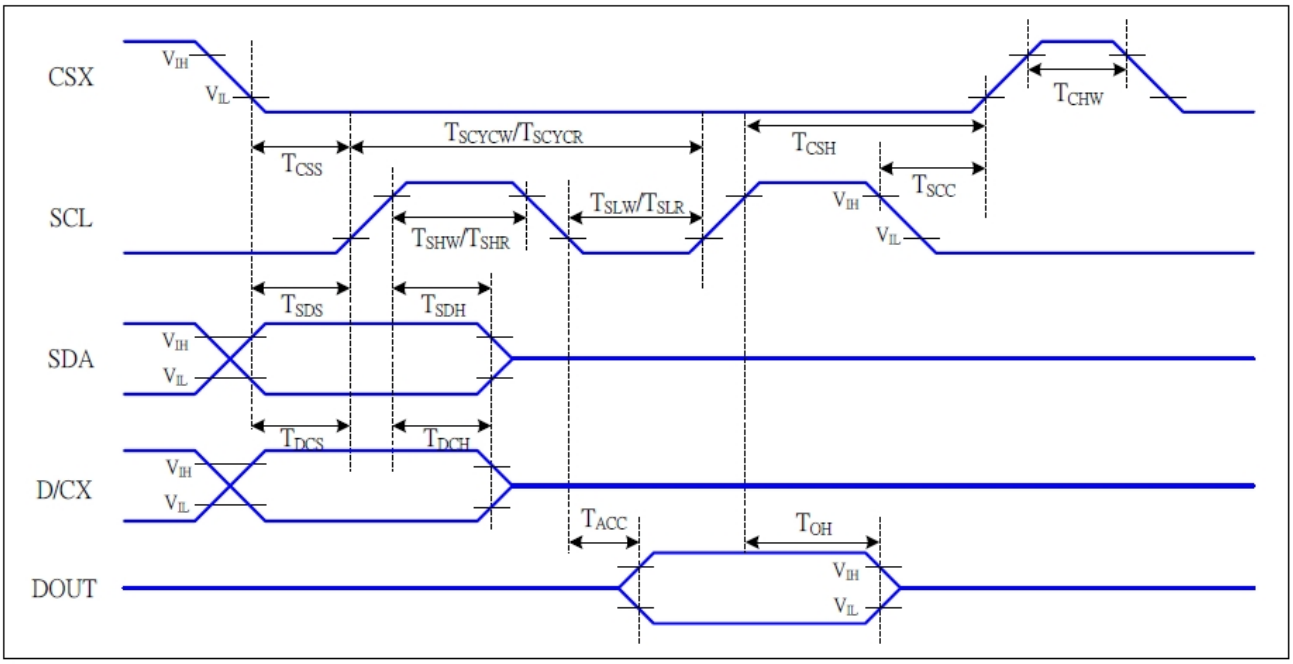


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	15	50	ns	

Table 6 4-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

Note2: In the read sequence of serial interface, the 500nsec delay time is needed between read command and first read clock.

5.6 Reset Timing

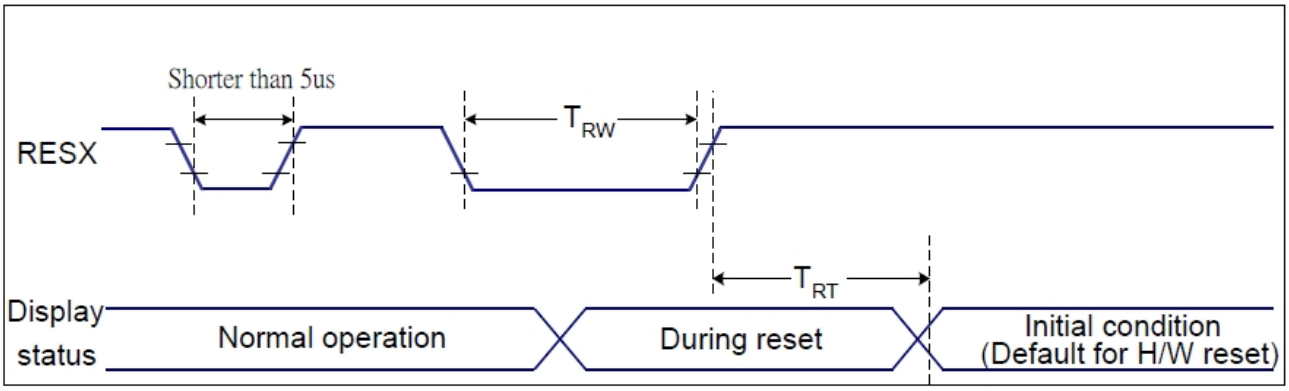


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

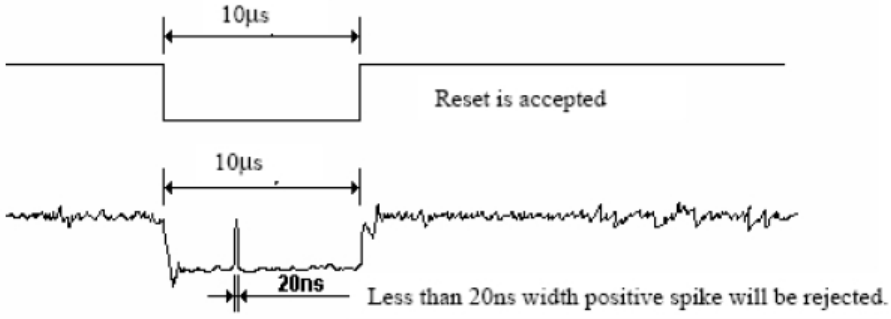
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6.0 ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply Voltage for Logic	V_{CC}	-0.3	-	4.6	V	-
Driver Supply Voltage	VGH-VGL	-0.3	-	30.0	V	-
Input Voltage	V_{IN}	-0.3	-	V_{CC}+0.5	V	-
Absolute maximum Forward Current	If_m	-	-	24	mA	-
Peak Forward Current	If_p	-	-	48	mA	1 msec plus , 1/10 duty cycle
Reverse Voltage	V_r	-	-	5	V	-
Power Dissipation	P_d	-	-	52.8	mW	-

Remarks: It is a normal characteristics that display may show some transitional optical imperfection when display is continuously running at extreme low and high temperature limit. Such transitional imperfection will disappear and resume back to normal characteristics within 24 hours when temperature returns back to room temperature. This transitional imperfection has no impact on display functionality and reliability for its nominal usage state as stated at item 1.0.

7.0 ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{SS} = 0 V, VCC=2.8V)

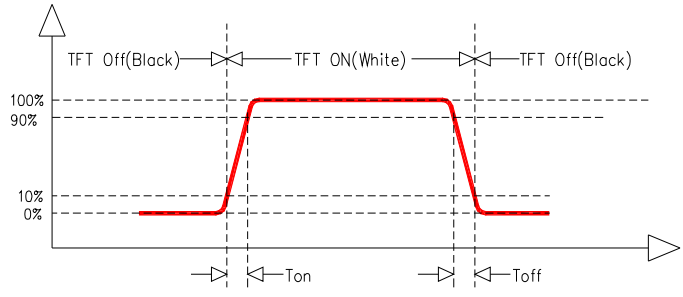
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
System Voltage	V_{CC}	-	2.4	2.8	3.3	V
Gate On Power	VGH	-	-	14.5	-	V
Gate Off Power	VGL	-	-	-10.43	-	V
Vcom	Vcom	-	-2	-1	0	V
Logic High Input Voltage	V_{IH}	-	0.7V_{CC}	-	V_{CC}	V
Logic Low Input Voltage	V_{IL}	-	VSS	-	0.3V_{CC}	V
Logic High Output Voltage	V_{OH}	IOH=-1.0mA	0.8V_{CC}	-	V_{CC}	V
Logic Low Output Voltage	V_{OL}	IOL= +1.0mA	VSS		0.2V_{CC}	V
LCM Supply Current	I_{LCM}	-	-	7.0	10.5	mA

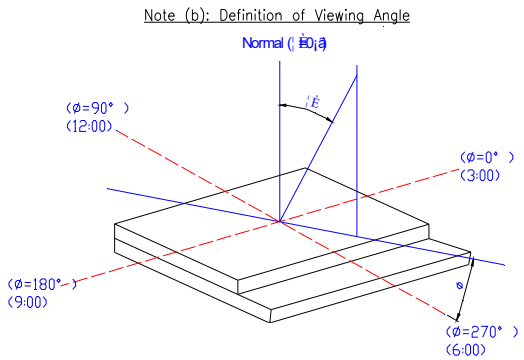
8.0 ELECTRO-OPTICAL CHARACTERISTICS

No	Item		Symbol	Measuring Conditions		Min.	Typ.	Max.	Unit	Remark
1	Response Time		Tr+Tf	25 °C		--	30	35	ms	Note (a)
2	Viewing Angle (CR ≥ 10)		θ	ϕ = 0°	25 °C	70	80	--	Deg	Note (b)
			θ	ϕ =180°	25 °C	70	80	--		
			θ	ϕ = 90°	25 °C	70	80	--		
			θ	ϕ =270°	25 °C	70	80	--		
3	Contrast Ratio		CR	θ = 0° ϕ = 0°	25 °C	640	800	--	--	Note (c)
4	Brightness on LCM		L_{LCM}	θ = 0° ϕ = 0°	25 °C	280	300	--	cd/m^2	Note (d)
5	Uniformity on LCM		Δ	θ = 0° ϕ = 0°	25 °C	80	-	-	%	1) Aperture:1°,9 Point 2)Average= min/max*100%
5	Color Chromaticity (CIE1931)	Red	Rx	θ = ϕ = 0°		0.528	0.578	0.628	-	-
			Ry			0.293	0.343	0.393	-	-
		Green	Gx			0.329	0.379	0.429	-	-
			Gy			0.531	0.581	0.631	-	-
		Blue	Bx			0.11	0.16	0.21	-	-
			By			0.064	0.114	0.164	-	-
		White	Wx			0.278	0.328	0.378	-	-
			Wy			0.298	0.348	0.398	-	-
6	NTSC			50%						-

Remarks:
1) EOC data above is measured using CS2000(viewing angle) and Admesy MSE+20MM(response time);
2) Brightness data is measured using photometer CA310.

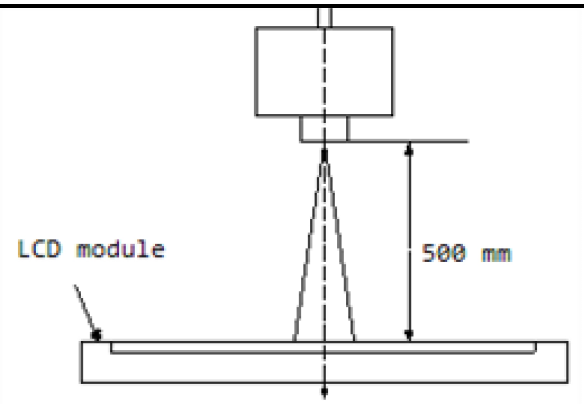
Note (a): Definition of Response Time





Note (c): Definition of Contrast Ratio
CR = Brightness at all pixels "White" / Brightness at all pixels "Black"
Note (d): After stabilizing and leaving the panel alone at a given temperature for 30 min, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the back-light. This should be measured in the center of screen.
Environment condition: Ta=25±2°C, Backlight On condition: If=140mA

measuring setup as below figure:



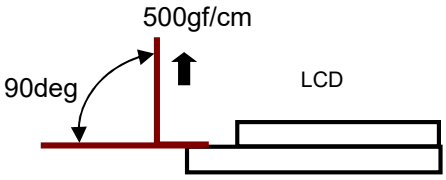
9.0 BACKLIGHT SPECIFICATION

Item	Symbol	Min	Typ	Max	Unit	Condition
Forward Voltage	Vf	2.8	3	3.3	V	If=20mA, T=25ºC
Number of LED	-		1		Piece	-
LED Lifetime	-		30000		Hour	1) Ta=25±5 □, RH=60%± 10%; If=20mA/LED 2) No other interference, Such as Current, Voltage suddenly rise, Electrostatic shock, etc. 3)Life time definition:the time when the LED luminous intensity attenuation to 50% at the beginning of the luminous intensity of time)

Remarks: Brightness data is measured using photometer Topcon BM-7A.

10.0 RELIABILITY SPECIFICATION

10.1 Reliability Test Conditions

No	Test Item	Test Conditions
1	High Temperature Storage	80°C, 240hrs
2	High Temperature Operation	70°C, 240hrs
3	Low Temperature Storage	-30°C, 240hrs
4	Low Temperature Operation	-20°C, 240hrs
5	High Temperature Humidity Operation	60°C, 90%RH, 240hrs
6	Temperature Cycling Storage	80°C/30min, -30°C/30min (transition time: 30min) : 10 cycles
7	Drop Test (on packaging)	Full packing, 100cm free fall (6 sides, 1 corner, 3 edges)
8	FPC peeling test	Peeling Degree: 90 deg. Peeling force specification ⩾ 500 gf/cm (only for ACF, without reinforcement tape and silicone).  Peeling speed: 50mm/min Qty: 3 PCS

Remarks:
1) For operation test, above specification is applicable when test pattern is changing during entire operation test.
2) Inspections after reliability tests are performed when the display temperature resumes back to room temperature.
3) It is a normal characteristic that some display abnormality can be seen during reliability test. If the display abnormality can recover as normal condition within 24 hours at room temperature, there is no permanent destruction over the display. The display still possesses its functionality and considered as acceptable after reliability tests.
4) For any life time simulation, normal use life time is defined as working in normal operating condition at 25°C and 60%RH. MTBF simulation is used for life time estimation. Acceleration at high temperature or high temperature high humidity (as stated above) is used in MTBF simulation with respect to normal use operating condition.

10.2 Failure Judgment Criteria

After the reliability tests above, test sample shall be let return to room temperature and humidity for at least 4 hours before final tests are carried out.

Item	Acceptance Criteria
Electrical Characteristic	No electrical short and open. Increase in current consumption is less than 2 times of initial value.
Mechanical Characteristic	Within mechanical and drawing specification
Optical Characteristic	Within appearance standard as specified in this specification. Contrast ratio change & ON-transmission value shall not less than 50% of initial value.

11.0 QUALITY SPECIFICATION

11.1 Acceptable Quality Level (AQL)

Each lot should satisfy the quality level defined as follows:

a) Inspection method: MIL-STD-105E Level II normal one time sampling

b) AQL level

Category	AQL	Definition
Major	0.65%	Functional defective as product
Minor	1.0%	Satisfy all functions as product but not satisfy cosmetic standard

11.2 Conditions of Inspection

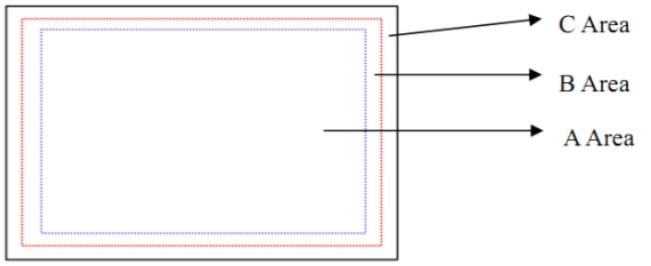
a) Inspection equipments: inspection and testing equipment used by the company.

b) Inspection illumination: function illumination<200Lux;Appearance illumination is 600~1000Lux.

c) Inspection distance: about 30+/-5cm between the observer's eyes and the LCD.

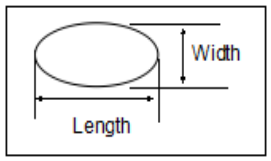
d) Inspection angle: normal inspection angle is +/-45°from LCD.

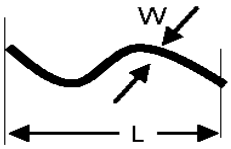
e) Inspection environment:normal temperature(18～27□)and normal humidity(50~85%RH).



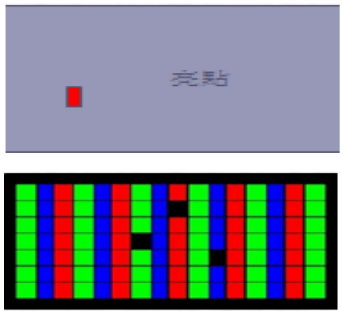
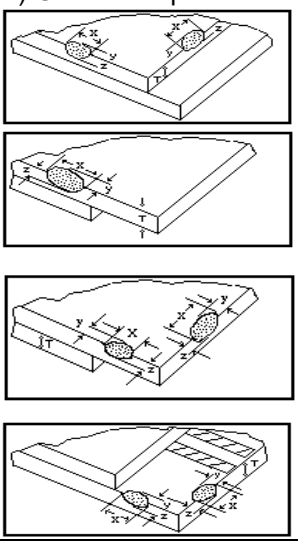
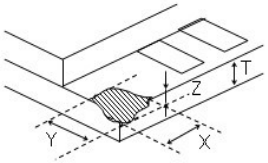
A: Active display area (AA area)
B: Viewing area (VA area)
C: Out of Viewing area

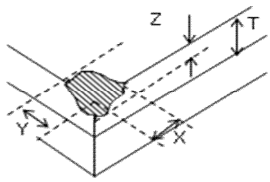
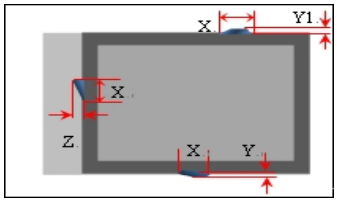
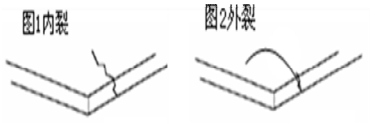
11.3 Acceptance Criteria (DISPLAY Elektronik GmbH internal standard: IS-QC-050(E) A0)

<table>
<tr><th>Item</th><th colspan="5">Acceptance/Rejection Criteria</th><th>Classification</th><th>Method</th></tr>
<tr><td rowspan="7">Spot、Foreign Particle，Dirt under POL or TP</td><td rowspan="6"> 

D=(Length+Width)/2</td><td>Size(mm)</td><td>A area</td><td>B area</td><td>C area</td><td rowspan="6">Minor</td><td rowspan="6">Visual
(Scale magnifying glass)</td></tr>
<tr><td>D≤0.15mm</td><td colspan="3">Unlimited.
Accumulation of small optical defect shall be less than 10dots in 5mm*5mm area.</td></tr>
<tr><td>0.15mm＜D≤0.25mm</td><td>2</td><td>3</td><td rowspan="4">Unlimited.</td></tr>
<tr><td>0.25mm＜D≤0.35mm</td><td>2</td><td>3</td></tr>
<tr><td>0.35mm＜D≤0.5mm</td><td>1</td><td>2</td></tr>
<tr><td>D＞0.5mm</td><td>0</td><td>0</td></tr>
<tr><td colspan="5">2 defect distance ≤5mm, the total number of defects is ≤5.</td></tr>
<tr><td rowspan="4">Line defect: foreign or Scratch</td><td rowspan="4"> 

Note: 2 defect distance ≤5mm</td><td>Size(mm)</td><td>A area</td><td>B area</td><td>C area</td><td rowspan="4">Minor</td><td rowspan="4">Visual
(Scale magnifying glass)</td></tr>
<tr><td>W≤0.05mm, L≤10mm</td><td>2</td><td>2</td><td rowspan="3">Unlimited.</td></tr>
<tr><td>0.05mm≤W≤0.08mm, L≤10mm</td><td>1</td><td>2</td></tr>
<tr><td>0.08mm≤W≤0.1mm L≤15mm</td><td>1</td><td>1</td></tr>
</table>

<table>
<tr><th>Item</th><th>Acceptance/Rejection Criteria</th><th>Classification</th><th>Method</th></tr>
<tr><td></td><td>0.1mm≤W≤0.2mm, L＞15mm | 0 | 0</td><td></td><td></td></tr>
<tr><td>Light dot
Dark dot
Definition</td><td>1) Pixel definition: Pixel is made of three sub-pixels (Red + Green +Blue)
2) Dot definition: Dot is a sub-pixel (Red or Green or Blue)
3) Light / Dark dot definition: A sub-pixel is on or off when the function testing.
Light dot: appears in dark picture usually.
Dark dot: appears in R\G\B color picture or the white picture usually.
4). Adjacent dot definition: Adjacent dot is made of two or three sub-pixels(R+G or G+B or B+R or R+G+B);</td><td>Minor</td><td>Visual
(Scale magnifying glass）</td></tr>
<tr><td>Bright dot/dark dot</td><td>
<table>
<tr><th>Defect</th><th>Acc No.</th></tr>
<tr><td>light dot</td><td>2</td></tr>
<tr><td>light dot two-connection</td><td>1</td></tr>
<tr><td>dark dot</td><td>5</td></tr>
<tr><td>dark dot two-connection</td><td>1</td></tr>
<tr><td>Total</td><td>≤5</td></tr>
</table>

</td><td>Minor</td><td>Visual
(Scale magnifying glass)</td></tr>
<tr><td>Mura</td><td>Mura which cannot be seen by ND 3 % is acceptable.</td><td>Minor</td><td>Visual</td></tr>
<tr><td>Chip-out</td><td>A) General chip-out

<table>
<tr><th>X(mm)</th><th>Y(mm)</th><th>Z(mm)</th><th>Acc No.</th></tr>
<tr><td>X≤2.0</td><td>Y≤0.3</td><td>Z≤T/2</td><td>2</td></tr>
<tr><td>2.0＜X≤5.0</td><td>0.3＜Y≤0.5</td><td>Z≤T/2</td><td>1</td></tr>
<tr><td>X＞5.0</td><td>Y＞0.5</td><td></td><td>0</td></tr>
</table>
Note: 1)Chip-out reach sealing ring is unacceptable.
2)Chip-out extend into the field of view is unacceptable(VA)
3)Chip-out on ITO electrode and affect bonding is unacceptable.</td><td>Minor</td><td>Visual
(Scale magnifying glass)</td></tr>
<tr><td></td><td>B) Chip-out at corner

<table>
<tr><th>X (mm)</th><th>Y (mm)</th><th>Z (mm)</th><th>Acc No.</th></tr>
<tr><td>X≤1.0</td><td>Y≤1.0</td><td>Z≤T</td><td>2</td></tr>
<tr><td>1.0＜X≤2.0</td><td>1.0＜Y≤2.0 And X+Y≤3.0</td><td>Z≤T</td><td>1</td></tr>
<tr><td>X＞2.0</td><td>Y＞2.0</td><td>Z≤T</td><td>0</td></tr>
</table>
Chip-out on ITO electrode is</td><td>Minor</td><td>Visual
(Scale magnifying glass)</td></tr>
</table>

<table>
<tr><th>Item</th><th colspan="2">Acceptance/Rejection Criteria</th><th>Classification</th><th>Method</th></tr>
<tr><td></td><td>  </td><td>unacceptable.</td><td></td><td></td></tr>
<tr><td></td><td>C) Glass bur
  </td><td><table><tr><th>X(mm)</th><th>Y(mm)</th><th>Z(mm)</th></tr><tr><td>Unlimited</td><td colspan="2">The dimension shall meet the specification in the drawing.</td></tr></table>Not affect the assembly.</td><td>Minor</td><td>Visual
(Scale magnifying glass)</td></tr>
<tr><td></td><td>D) Crack
  </td><td>1) Progressive internal crack cannot be acceptable.
2) The external crack, the glass can be removed. After removing, follow the glass damage&chip standard. Also there should be no removable glass residue.</td><td></td><td>Visual
(Scale magnifying glass)</td></tr>
</table>

For inspection specifications not covered, refer to the following inspection criteria.

Defect Project		Criteria for determination	Defect category
FPC defective	FPC crease	Crease influence functional performance is not allowed	Minor defect
	FPC damaged	NG	Serious defect
	FPC open circuit and short circuit	NG	Serious defect
	FPC cold soldering	NG	Serious defect
	FPC component offset and short circuit	NG	Serious defect
	Less or more FPC components	NG	Serious defect
TP&CG defective	white spots, puncture wounds, foreign bodies	As determined by the specification of the dots and lines	Minor defect
defective BLU	BL is not lit	NG	Serious defect
	BLU can't light-on	NG	Serious defect
	BL incoming material scratch	Judged as a linear defect	Minor defect
	BL foreign body	Determined by point or line defects	Minor defect
defective LCD	LCD LC Leakage	NG	Serious defect
Functional defect	No display	NG	Serious defect
	Display abnormal	NG	Serious defect
	Over Current	NG	Serious defect
	Horizontal Line	NG	Serious defect
	Vertical Bar	NG	Serious defect

	The cross hairs are missing	NG	Serious defect
Poor packaging	Packing quantity discrepancies	NG	Serious defect
	Packaging does not match the drawing	NG	Minor defect

12.0 ENVIRONMENTAL SPECIFICATION

This product is designed, manufactured and compliant to below RoHS standard:

1. Cadmium and Cadmium Compounds Less than 100ppm
2. Hexavalent Chromium Compounds Less than 1000ppm
3. Lead and Lead Compounds Less than 1000ppm
4. Mercury and Mercury Compounds Less than 1000ppm
5. Polybrominated Biphenyls (PBBs) Less than 1000ppm
6. Polybrominated Diphenyl ethers (PBDEs) Less than 1000ppm
7. Butyl benzyl phthalate (BBP) Less than 1000ppm
8. Bis (2-ethylhexyl)phthalate (DEHP) Less than 1000ppm
9. Dibutyl phthalate (DBP) Less than 1000ppm
10. Diisobutyl phthalate(DIBP) Less than 1000ppm

13.0 GENERAL PRECAUTIONS FOR USING LCD MODULES

Handling Precaution

- No strong mechanical shock. LCD may be broken because it is made out of glass.
- Do not work on PCB. PCB may be cracked or damaged.
- Do not bend or process metal bezel positioning tab. LCD maybe shifted and LCD-PCB interconnection may be damaged,
- Do not scratch. Polarizer is soft material and can be easily scratched.
- Liquid crystal may leak when LCD/LCM is broken. Please wash your hands if you touch the liquid crystal.
- Wear gloves when handling LCD/LCM to avoid damage to LCD/LCM. Please do not touch electrodes with bare hands to avoid any contamination on connection.

Soldering Precaution on LCD/LCM

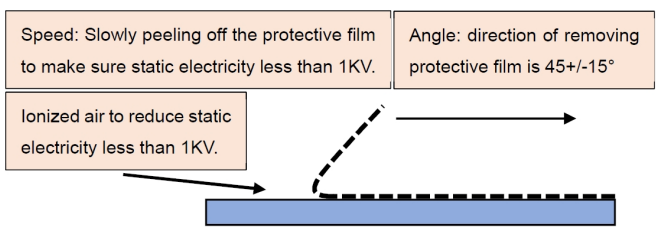
- Use soldering iron with proper grounding and no AC leakage.
- Temperature at tip of soldering iron: 330±10°C
- Type of solder: lead-free solder with resin flux fill.
- Soldering time: < 3sec.
- Soldering on LCD/LCM I/O terminal only.
- Do not apply force on the LCD metal pin when soldering. Metal pin connection to LCD terminal will be damaged or loosen by this external force under soldering temperature.
- Do not solder and de-solder for more than 3 times because metal pin connection or soldering pads will be damaged.

Operation Precautions

- Viewing angle can be adjusted by varying driving voltage, V_0 or Vop.
- Display performance may vary or show abnormal electro-optical performance when viewed at angle beyond the specified viewing angle range.
- Display color may change under extreme temperature. This is not destructive symptom and display color will resume back to normal when temperature goes back to normal temperature.
- Driving voltage shall be kept within the specified range as stated in this product specification. Over-voltage may shorten the LCD/LCM lifetime.
- No DC voltage to LCD/LCM. Electrical characteristics and reliability of LCD/LCM will deteriorate under DC. Please control the DC content in application driving circuit.
- Avoid using the same display pattern for long time (continuous ON segment). It is a normal phenomena observed for passive driven display where image retention is observed when LCD is displayed with same pattern over 1 hour under temperature > 55°C. Customer is advised to design application software where display pattern will be changed from time to time, or using the N-line inversion function comes with the display driver IC.
- If the LCM is using master-slave configuration, customer is strongly recommended to use external Vo.
- If the LCM comes with MTP/OTP function, customer is recommended to use this MTP/OTP function for the best optical performance.
- Full reliability tests are advised to be launched after 10 days of manufacturing date.

Static Electricity

- Avoid static electricity. Please have proper ESD control and ground the human body and any electrical tools when assembling the LCD/LCM.
- Static electricity will be generated when peeling the protective film. It is a normal behavior that LCD/LCM will response to the static charges generated and will resume back to normal condition slowly. Peeling off the protective film in a correct way is very important to reduce the static electricity and its influence on LCD/LCM. It's recommended that the static electricity is controlled less than 1KV by using ion fan and peeling off protective film slowly and in 45° angle, etc.



FPC cleanness

- If ACF bonding is applied at customer side between FPC and PCB, cleaning on FPC and PCB bonding area (just before bonding) is a must to reduce risk of bonding reliability (eg bonding delamination/spring back phenomenon, low pull strength etc)

Long-term Storage Conditions

- Store LCD/LCM in dark area and keep LCD/LCM away from direct sunlight and fluorescent light.
- Store LCD/LCM under temperature range of 0~35°C and room humidity of 50~60%RH.
- Possible Vop adjustment might be needed at customer side after prolong storage over 1 year from date of manufacturing.