

RoHS Compliant

4GB REGISTERED DDR4 DIMM

Industrial / Halogen free

Product Specifications

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Version 0.5



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General Description

Apacer **D52.23184S.002** is a 512Mx72 DDR4 SDRAM (Synchronous DRAM) ECC Registered DIMM. This high-density memory module consists of 9 pieces 512M x 8 bits DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 288-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
D52.23184S.002	21.3 GB/sec	2666 Mbps	1333 MHz	CL19

Density	Organization	Component	Rank
4GB	512M x 72	512M x8*9	1

Key Parameters

MT/s	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
Grade	-CL13	-CL15	-CL17	-CL19	
tCK (min)	1.07	0.93	0.83	0.75	ns
CAS latency	13	15	17	19	tCK
tRCD (min)	13.92	14.06	14.16	14.25	ns
tRP (min)	13.92	14.06	14.16	14.25	ns
tRAS (min)	34	33	32	32	ns
tRC (min)	47.92	47.05	46.16	46.25	ns
CL-tRCD-tRP	13-13-13	15-15-15	17-17-17	19-19-19	tCK

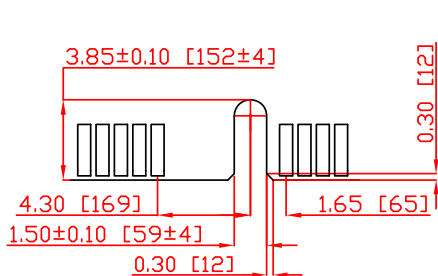
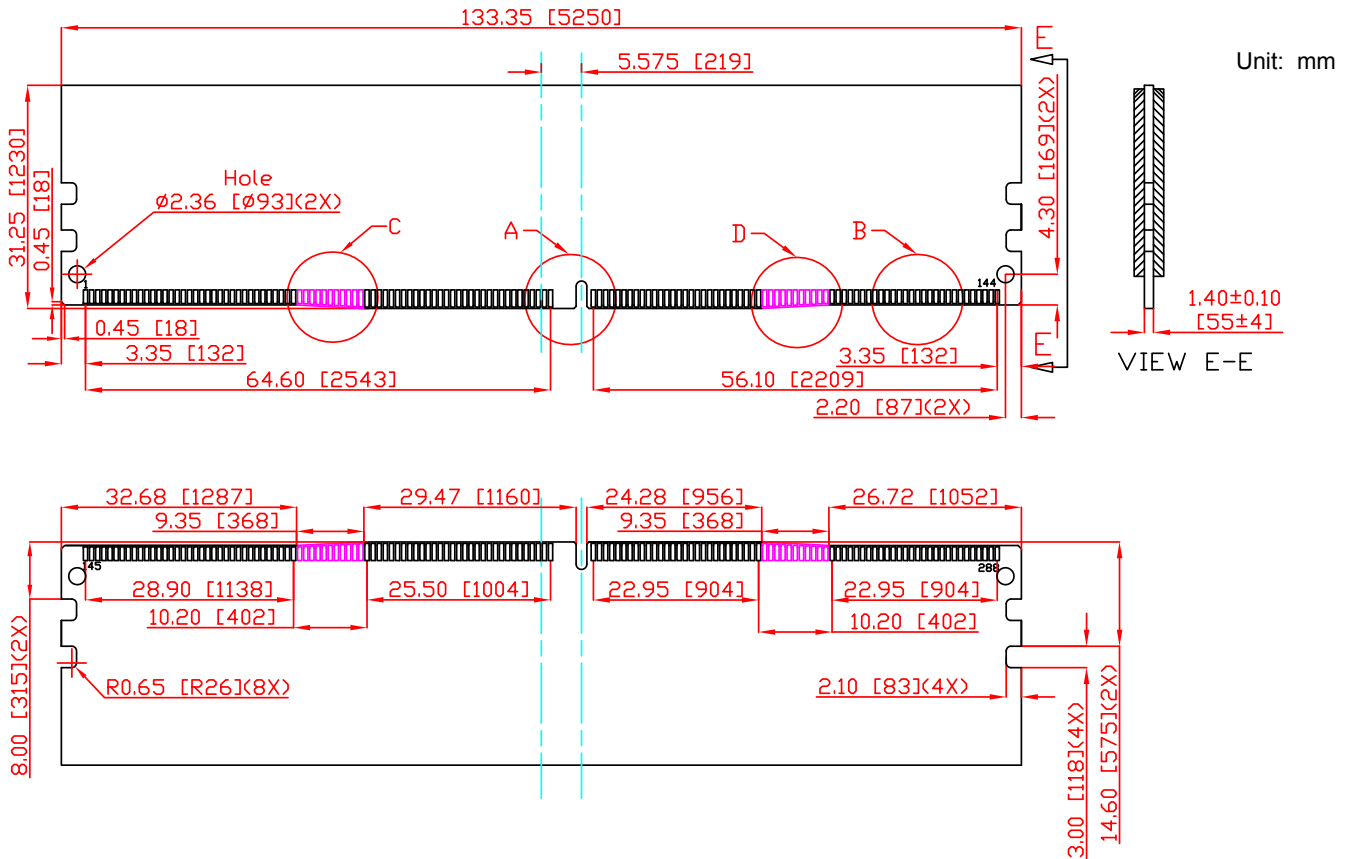
Specifications:

- ◆ Support ECC error detection and correction
- ◆ On-DIMM thermal sensor : Yes
- ◆ Organization: 512 words x 72 bits, 1 rank
- ◆ Integrating 9 pieces of 4G bits DDR4 SDRAM sealed FBGA
- ◆ Package: 288-pin socket type dual in-line memory module (REG DIMM)
- ◆ PCB: height 31.25 mm, lead pitch 0.85 mm (pin),
- ◆ Serial Presence Detect (SPD)
- ◆ Power Supply: VDD=1.2V (1.14V to 1.26V)
- ◆ VDDQ = 1.2V (1.14V to 1.26V)
- ◆ VPP = 2.5V (2.375V to 2.75V)
- ◆ VDDSPD = 2.2V to 3.6V
- ◆ 16 internal banks
- ◆ CAS Latency (CL): 10, 11, 12, 13, 14, 15,16,17,18,19,20
- ◆ CAS Write Latency (CWL): 14,18
- ◆ Support Industrial Temp (-40°C~95°C)
 - tREFI 7.8us at -40 °C ≤ TCASE ≤ 85°C
 - tREFI 3.9us at 85 °C < TCASE ≤ 95°C
- ◆ Lead-free (RoHS compliant)
- ◆ Halogen free
- ◆ PCB: 30μ inch gold finger

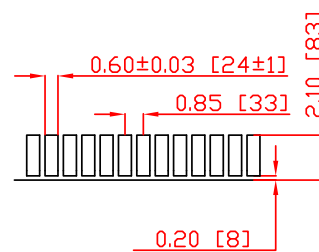
Features:

- ◆ Functionality and operations comply with the DDR4 SDRAM datasheet
- ◆ Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- ◆ Bi-Directional Differential Data Strobe
- ◆ 8 bit pre-fetch
- ◆ Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- ◆ Supports ECC error correction and detection
- ◆ Per DRAM Addressability is supported
- ◆ Internal Vref DQ level generation is available
- ◆ Write CRC is supported at all speed grades
- ◆ DBI (Data Bus Inversion) is supported(x8)
- ◆ CA parity (Command/Address Parity) mode is supported

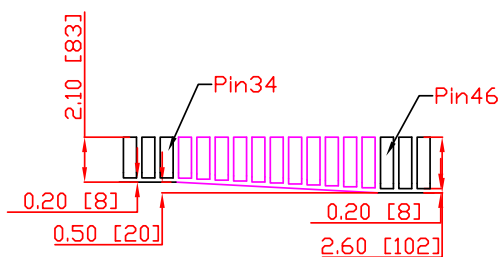
Mechanical Drawing



Detail A

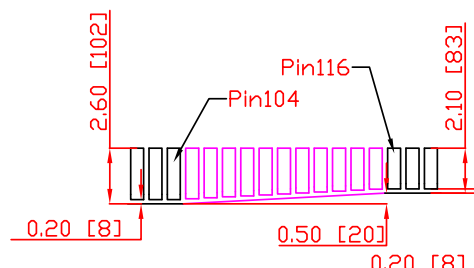


Detail B



Detail C

30μ inch gold finger



Detail D

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
0.1	5/5/2014	Initial release	
0.2	11/2/2015	Updated VDDSPD	
0.3	03/15/2017	Add Environmental Requirements	
0.4	09/04/2017	Remove TOPR (Operating Temperature (ambient))	
0.5	07/23/2020	Updated DRAM Component Operating Temperature Range	

Global Presence

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