RoHS Compliant

32GB DDR4 SDRAM UDIMM Halogen free

Product Specifications

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Version 0.4

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General Description

Apacer **D12.2730HS.001** is a 4096M x 64 DDR4 SDRAM (Synchronous DRAM) DIMM. This high-density memory module consists of 16 pieces 2048M x 8 bits DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 288-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
D12.2730HS.001	25.6 GB/sec	3200 Mbps	1600 MHz	CL22

Density	Organization	Component	Rank
32GB	4096M x 64	2048M x8*16	2

Key Parameters

MT/s	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
Grade	-CL17	-CL19	-CL21	-CL22	
tCK (min)	0.83	0.75	0.68	0.62	ns
CAS latency	17	19	21	22	tCK
tRCD (min)	14.16	14.25	14.32	13.75	ns
tRP (min)	14.16	14.25	14.32	13.75	ns
tRAS (min)	32	32	32	32	ns
tRC (min)	46.16	46.25	46.32	45.75	ns
CL-tRCD-tRP	17-17-17	19-19-19	21-21-21	22-22-22	tCK

Specifications:

- On-DIMM thermal sensor : No
- Organization: 4096 words x 64 bits, 2 ranks
- Integrating 16 pieces of 16G bits DDR4 SDRAM sealed FBGA
- Package: 288-pin socket type dual in-line memory module (DIMM)
- PCB: height 31.25 mm, lead pitch 0.85 mm (pin),
- Serial Presence Detect (SPD)
- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP = 2.5V (2.375V to 2.75V)
- VDDSPD = 2.2V to 3.6V
- 16 internal banks
- CAS Latency (CL): 10, 11, 12, 13, 14, 15,16,17,18,19, 20, 21, 22,24
- CAS Write Latency (CWL): 16,20
- Average refresh period

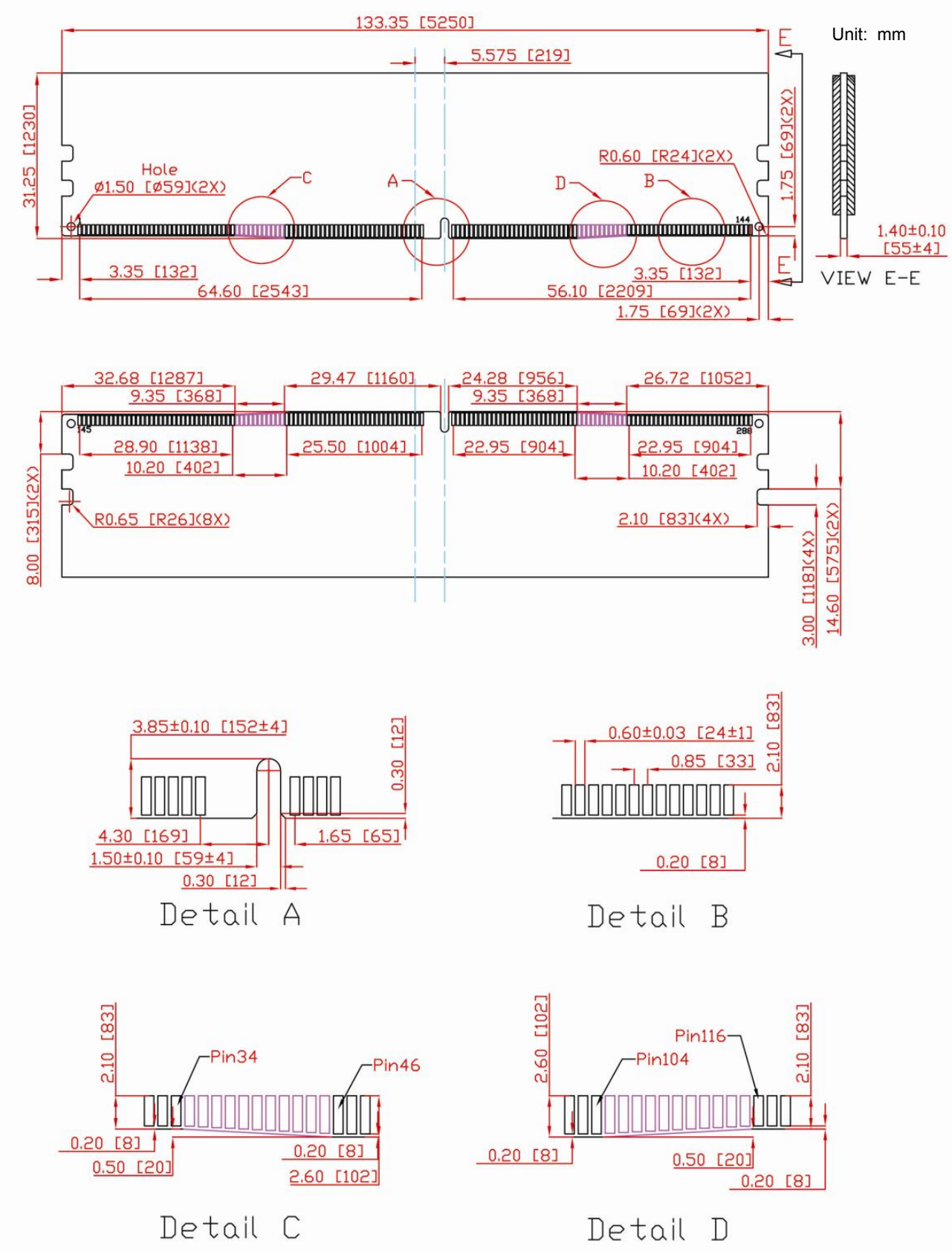
  7.8us at 0°C $\leqq$ TC $\leqq$ 85°C

  3.9us at 85°C $\leqq$ TC $\leqq$ 95°C
- Lead-free (RoHS compliant)
- Halogen free

Features:

- Functionality and operations comply with the DDR4 SDRAM datasheet
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported(x8)
- CA parity (Command/Address Parity) mode is supported

Mechanical Drawing



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
0.1	5/5/2014	Initial release	
0.2	11/2/2015	Updated VDDSPD	
0.3	03/15/2017	Add Environmental Requirements	
0.4	09/04/2017	Remove TOPR (Operating Temperature (ambient))	

Global Presence

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