Datasheet

APM32S103x8xB

Arm® Cortex®-M3 based 32-bit MCU

Version: V1.3

1. Product characteristics

Core

- 32-bit Arm® Cortex®-M3 core
- Up to 96MHz working frequency

On-chip memory

- Flash：128KB
- SRAM：36KB

Clock

- HSECLK: 4~16MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- LSICLK: 40KHz RC oscillator supported
- PLL: Phase locked loop, 2~16 times of frequency supported

Reset and power management

- V_{DD} range: 2.0～3.6V
- V_{DDA} range: 2.0～3.6V
- V_{BAT} range of backup domain power supply: 1.8V～3.6V
- Power-on/power-down reset (POR/PDR) supported
- Programmable power supply voltage detector supported

Low-power mode

- Sleep, stop and standby modes supported

DMA

- One 7-channel DMA

Debugging interface

- JTAG
- SWD

I/O

- Up to 80 I/Os
- All I/Os can be mapped to external interrup vector
- Up to 60 FT input I/Os

Communication peripherals

- 2 I2C interfaces (1Mbit/s), all of which support SMBus/PMBus
- 3 USART, support ISO7816, LIN and IrDA functions
- 2 SPI, maximum transmission speed 18Mbps
- 1 QSPI, support single - and four-wire access to Flash
- 2 CAN
- 1 USBD

Analog peripherals

- 2 12-bit ADCs

Timer

- 1 16-bit advanced timers TMR1 that can provide 7-channel PWM output, support dead time generation and braking input functions
- 3 16-bit general-purpose timers TMR2/3/4, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
- 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
- 1 24-bit autodecrement SysTick Timer

RTC

- Support calendar functions

84Bytes backup register

CRC computing unit

FPU

96-bit unique device ID

Catalog

2. Product information

See the following table for APM32S103x8xB product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32S103x8xB Series Chips

Product		**APM32S103x8xB**				
Model		TBU6	C8T6	CBT6	RBT6	VBT6
Package		QFN36	LQFP48		LQFP64	LQFP100
Core and maximum working frequency		Arm® 32-bit Cortex®-M3@96MHz				
Operating voltage		2.0~3.6V				
Flash(KB)		128	64	128		
SRAM(KB)		36				
GPIOs		26	37		51	80
Communication interface	USART	2	3			
	SPI	1	2			
	QSPI	0				1
	I2C	1	2			
	USBD	1				
	CAN	2				
Timer	16-bit advanced	1				
	16-bit general	3				
	System tick timer	1				
	Watchdog	2				
Real-time clock		1				
12-bit ADC	Unit	2				
	External channel	10			16	
	Internal channel	2				
Operating temperature		Ambient temperature：-40°C to 85°C/-40℃ to 105℃ Junction temperature：-40°C to 105°C/-40°C to 125°C				

Note: Different models of APM32S103x8xB series have different operating temperatures. For details, see the ordering information table in Chapter 8.

3. Pin information

3.1. Pin distribution

Figure 1 Distribution Diagram of APM32S103x8xB Series LQFP100 Pins

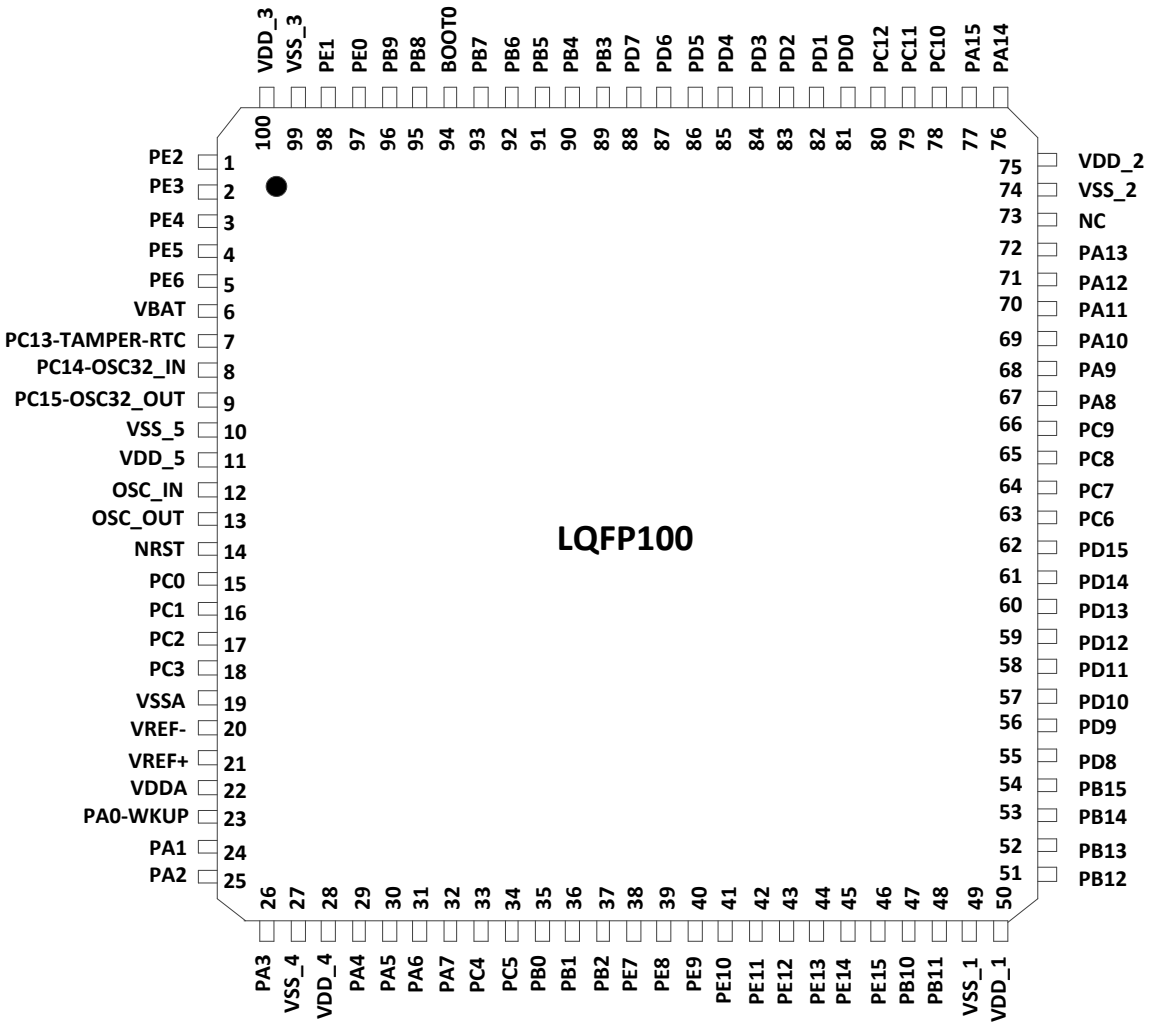


Figure 2 Distribution Diagram of APM32S103x8xB Series LQFP48 Pins

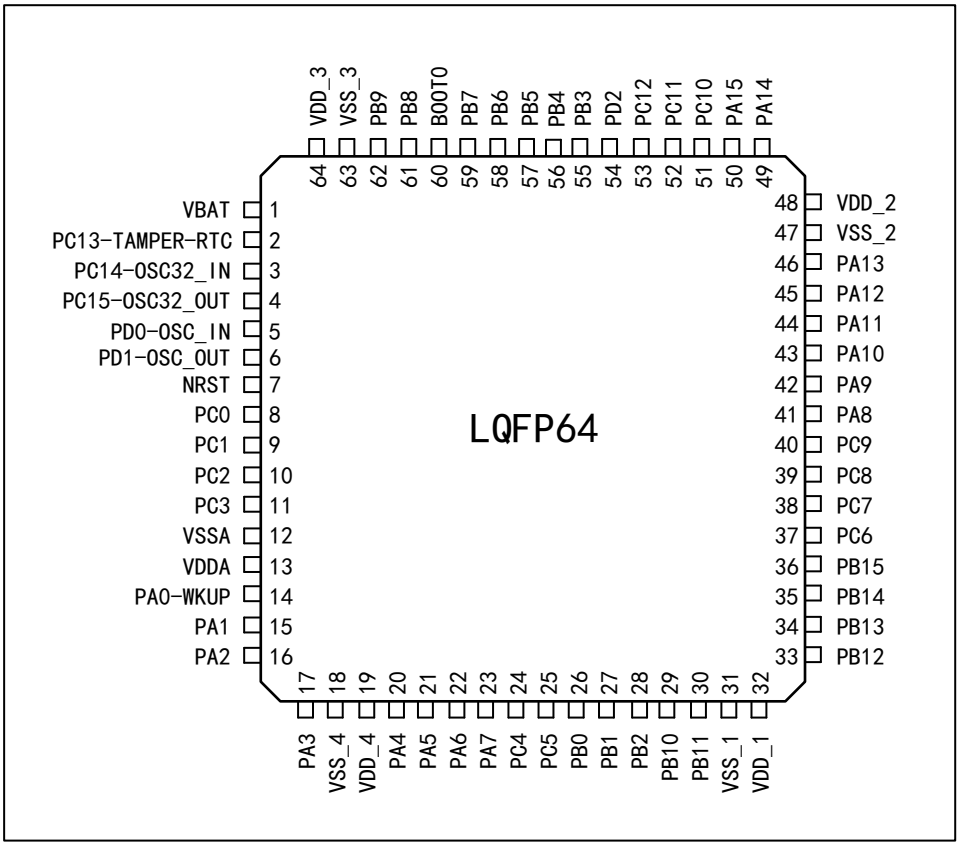


Figure 3 Distribution Diagram of APM32S103x8xB Series LQFP48 Pins

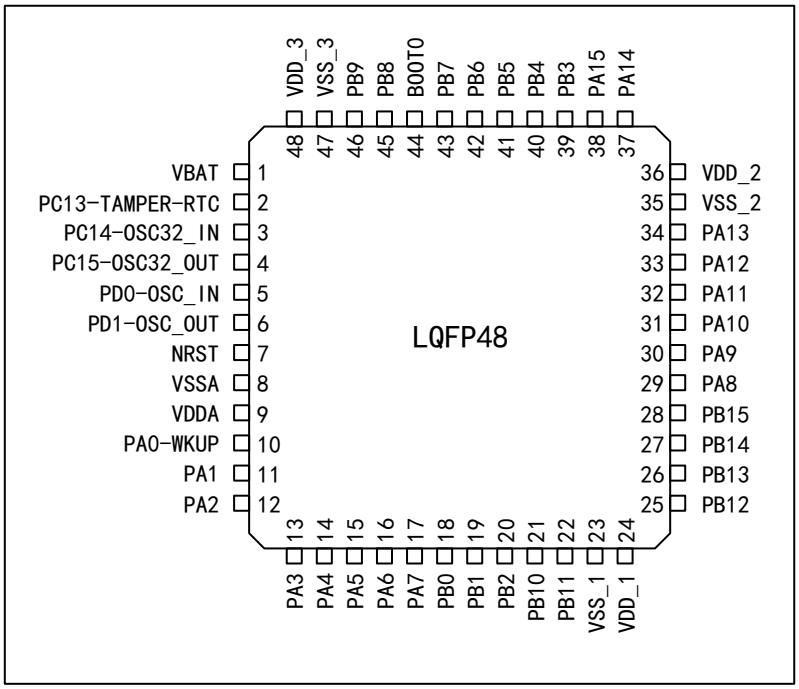
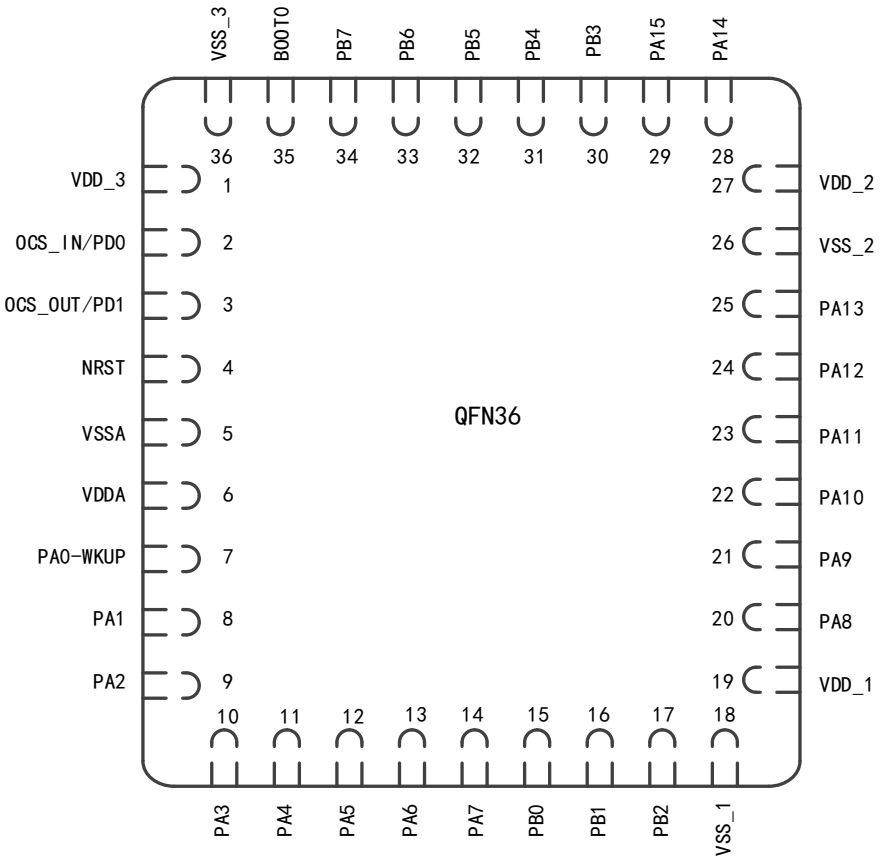


Figure 4 Distribution Diagram of APM32S103x8xB Series QFN36 Pins



3.2. Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	5T	FT I/O
	5Tf	FT I/O, FM+ function
	STDA	I/O with 3.3 V tolerance, directly connected to ADC
	STD	I/O with 3.3 V tolerance
	B	Dedicated Boot0 pin
	RST	Bidirectional reset pin with built-in weak pull-up resistor

Name		Abbreviation	Definition
Note		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	
	Remap	Select this function through AFIO remapping register	

Table 3 Description of APM32S103x8xB by Pin Number

Pin Name	Pins				Type	I/O level	Main functions	Alternate functions	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Remap
PE2	-	-	1	-	I/O	5T	PE2	TRACECK	-
PE3	-	-	2	-	I/O	5T	PE3	TRACED0	-
PE4	-	-	3	-	I/O	5T	PE4	TRACED1	-
PE5	-	-	4	-	I/O	5T	PE5	TRACED2	-
PE6	-	-	5	-	I/O	5T	PE6	TRACED3	-
V_{BAT}	1	1	6	-	P	-	V_{BAT}	-	-
PC13- TAMPER-RTC	2	2	7	-	I/O	-	PC13(1)	TAMPER-RTC	-
PC14- OSC32_IN	3	3	8	-	I/O	-	PC14(1)	OSC32_IN	-
PC15- OSC32_OUT	4	4	9	-	I/O	-	PC15(1)	OSC32_OUT	-
V_{SS_5}	-	-	10	-	P	-	V_{SS_5}	-	-
V_{DD_5}	-	-	11	-	P	-	V_{DD_5}	-	-
OSC_IN	5	5	12	2	I	-	OSC_IN	-	PD0(2)
OSC_OUT	6	6	13	3	O	-	OSC_OUT	-	PD1(2)
NRST	7	7	14	4	I/O	-	NRST	-	-
PC0	-	8	15	-	I/O	-	PC0	ADC12_IN10	-
PC1	-	9	16	-	I/O	-	PC1	ADC12_IN11	-
PC2	-	10	17	-	I/O	-	PC2	ADC12_IN12	-
PC3	-	11	18	-	I/O	-	PC3	ADC12_IN13	-
V_{SSA}	8	12	19	5	P	-	V_{SSA}	-	-
V_{REF-}	-	-	20	-	P	-	V_{REF-}	-	-
V_{REF+}	-	-	21	-	P	-	V_{REF}+	-	-
V_{DDA}	9	13	22	6	P	-	V_{DDA}	-	-
PA0-WKUP	10	14	23	7	I/O	-	PA0	WKUP/ USART2_CTS/ ADC12_IN0/ TMR2_CH1_ETR	-

Pin Name	Pins				Type	I/O level	Main functions	Alternate functions	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Remap
PA1	11	15	24	8	I/O	-	PA1	USART2_RTS/ ADC12_IN1/ TMR2_CH2	-
PA2	12	16	25	9	I/O	-	PA2	USART2_TX/ ADC12_IN2/ TMR2_CH3	-
PA3	13	17	26	10	I/O	-	PA3	USART2_RX/ ADC12_IN3/ TMR2_CH4	-
V_{SS_4}	-	18	27	-	P	-	V_{SS_4}	-	-
V_{DD_4}	-	19	28	-	P	-	V_{DD_4}	-	-
PA4	14	20	29	11	I/O	-	PA4	SPI1_NSS/ USART2_CK/ ADC12_IN4	-
PA5	15	21	30	12	I/O	-	PA5	SPI1_SCK/ ADC12_IN5	-
PA6	16	22	31	13	I/O		PA6	SPI1_MISO/ ADC12_IN6/ TMR3_CH1	TMR1_BKIN
PA7	17	23	32	14	I/O		PA7	SPI1_MOSI/ ADC12_IN7/ TMR3_CH2	TMR1_CH1N
PC4	-	24	33	-	I/O	-	PC4	ADC12_IN14	-
PC5	-	25	34	-	I/O	-	PC5	ADC12_IN15	-
PB0	18	26	35	15	I/O	-	PB0	ADC12_IN8/ TMR3_CH3	TMR1_CH2N
PB1	19	27	36	16	I/O	-	PB1	ADC12_IN9/ TMR3_CH4	TMR1_CH3N
PB2	20	28	37	17	I/O	5T	PB2/BOOT1	-	-
PE7	-	-	38	-	I/O	5T	PE7	-	TMR1_ETR
PE8	-	-	39	-	I/O	5T	PE8	-	TMR1_CH1N
PE9	-	-	40	-	I/O	5T	PE9	-	TMR1_CH1
PE10	-	-	41	-	I/O	5T	PE10	-	TMR1_CH2N
PE11	-	-	42	-	I/O	5T	PE11	-	TMR1_CH2
PE12	-	-	43	-	I/O	5T	PE12	-	TMR1_CH3N
PE13	-	-	44	-	I/O	5T	PE13	-	TMR1_CH3
PE14	-	-	45	-	I/O	5T	PE14	-	TMR1_CH4

Pin Name	Pins				Type	I/O level	Main functions	Alternate functions	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Remap
PE15	-	-	46	-	I/O	5T	PE15	-	TMR1_BKIN
PB10	21	29	47	-	I/O	5T	PB10	I2C2_SCL/ USART3_TX	TMR2_CH3
PB11	22	30	48	-	I/O	5T	PB11	I2C2_SDA/ USART3_RX	TMR2_CH4
V_{SS_1}	23	31	49	18	P	-	V_{SS_1}	-	-
V_{DD_1}	24	32	50	19	P	-	V_{DD_1}	-	-
PB12	25	33	51	-	I/O	5T	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK/ TMR1_BKIN/ CAN2_RX	
PB13	26	34	52	-	I/O	5T	PB13	SPI2_SCK/ USART3_CTS/ TMR1_CH1N/ QSPI_IO0/ CAN2_TX	
PB14	27	35	53	-	I/O	5T	PB14	SPI2_MISO/ USART3_RTS/ TMR1_CH2N/ QSPI_IO1	
PB15	28	36	54	-	I/O	5T	PB15	SPI2_MOSI/ TMR1_CH3N/ QSPI_IO2	-
PD8	-	-	55	-	I/O	5T	PD8	QSPI_IO3	USART3_TX
PD9	-	-	56	-	I/O	5T	PD9	-	USART3_RX
PD10	-	-	57	-	I/O	5T	PD10	QSPI_CLK	USART3_CK
PD11	-	-	58	-	I/O	5T	PD11	-	USART3_CTS
PD12	-	-	59	-	I/O	5T	PD12	QSPI_SS_N	TMR4_CH1/ USART3_RTS
PD13	-	-	60	-	I/O	5T	PD13	-	TMR4_CH2
PD14	-	-	61	-	I/O	5T	PD14	-	TMR4_CH3
PD15	-	-	62	-	I/O	5T	PD15	-	TMR4_CH4
PC6	-	37	63	-	I/O	5T	PC6	-	TMR3_CH1
PC7	-	38	64	-	I/O	5T	PC7	-	TMR3_CH2
PC8	-	39	65	-	I/O	5T	PC8	-	TMR3_CH3
PC9	-	40	66	-	I/O	5T	PC9	-	TMR3_CH4

Pin Name	Pins				Type	I/O level	Main functions	Alternate functions	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Remap
PA8	29	41	67	20	I/O	5T	PA8	USART1_CK/ TMR1_CH1/ MCO	-
PA9	30	42	68	21	I/O	5T	PA9	USART1_TX/ TMR1_CH2	-
PA10	31	43	69	22	I/O	5T	PA10	USART1_RX/ TMR1_CH3	-
PA11	32	44	70	23	I/O	5T	PA11	USART1_CTS/ USBD1DM/ USBD2DM CAN1_RX/ TMR1_CH4	-
PA12	33	45	71	24	I/O	5T	PA12	USART1_RTS/ USBD1DP/ USBD2DP CAN1_TX/ TMR1_ETR	-
PA13	34	46	72	25	I/O	5T	JTMS/ SWDIO	-	PA13
未连接	-	-	73	-	-	-	-	未连接	-
V_{SS_2}	35	47	74	26	P		V_{SS_2}	-	-
V_{DD_2}	36	48	75	27	P		V_{DD_2}	-	-
PA14	37	49	76	28	I/O	5T	JTCK/ SWCLK	-	PA14
PA15	38	50	77	29	I/O	5T	JTDI	-	TMR2_CH1_ETR/ PA15/ SPI1_NSS
PC10	-	51	78	-	I/O	5T	PC10	-	USART3_TX
PC11	-	52	79	-	I/O	5T	PC11	-	USART3_RX
PC12	-	53	80	-	I/O	5T	PC12	-	USART3_CK
PD0	-	-	81	2	I/O	5T	PD0	-	CAN1_RX
PD1	-	-	82	3	I/O	5T	PD1	-	CAN1_TX
PD2	-	54	83	-	I/O	5T	PD2	TMR3_ETR	-
PD3	-	-	84	-	I/O	5T	PD3	-	USART2_CTS
PD4	-	-	85	-	I/O	5T	PD4	-	USART2_RTS
PD5	-	-	86	-	I/O	5T	PD5	-	USART2_TX

Pin Name	Pins				Type	I/O level	Main functions	Alternate functions	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Remap
PD6	-	-	87	-	I/O	5T	PD6	-	USART2_RX
PD7	-	-	88	-	I/O	5T	PD7	-	USART2_CK
PB3	39	55	89	30	I/O	5T	JTDO	-	PB3/ TRACESWO/ TMR2_CH2/ SPI1_SCK
PB4	40	56	90	31	I/O	5T	NJTRST	-	PB4/ TMR3_CH1/ SPI1_MISO
PB5	41	57	91	32	I/O	-	PB5	I2C1_SMBAI	TMR3_CH2/ SPI1_MOSI/ CAN2_RX
PB6	42	58	92	33	I/O	5T	PB6	I2C1_SCL/ TMR4_CH1	USART1_TX/ CAN2_TX
PB7	43	59	93	34	I/O	5T	PB7	I2C1_SDA/ TMR4_CH2	USART1_RX
BOOT0	44	60	94	35	I	-	BOOT0	-	-
PB8	45	61	95	-	I/O	5T	PB8	TMR4_CH3	I2C1_SCL/ CAN1_RX
PB9	46	62	96	-	I/O	5T	PB9	TMR4_CH4	I2C1_SDA/ CAN1_TX
PE0	-	-	97	-	I/O	5T	PE0	TMR4_ETR	-
PE1	-	-	98	-	I/O	5T	PE1	-	-
V_{SS_3}	47	63	99	36	P	-	V_{SS_3}	-	-
V_{DD_3}	48	64	100	1	P	-	V_{DD_3}	-	-

Note:

(1) PC13, PC14 and PC15 are powered through the power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:

① The speed shall not exceed 2MHz when the heavy load is 30pF;

② Not used for current source (e.g. driving LED).

(2) For Pin 5 and Pin 6 of LQFP64 and LQFP48 package, the default configuration after the chip is reset is OSC_IN and OSC_OUT, the software can reset these two pins with PD0 and PD1 functions; for LQFP100 package, PD0 and PD1 are inherent function pins.

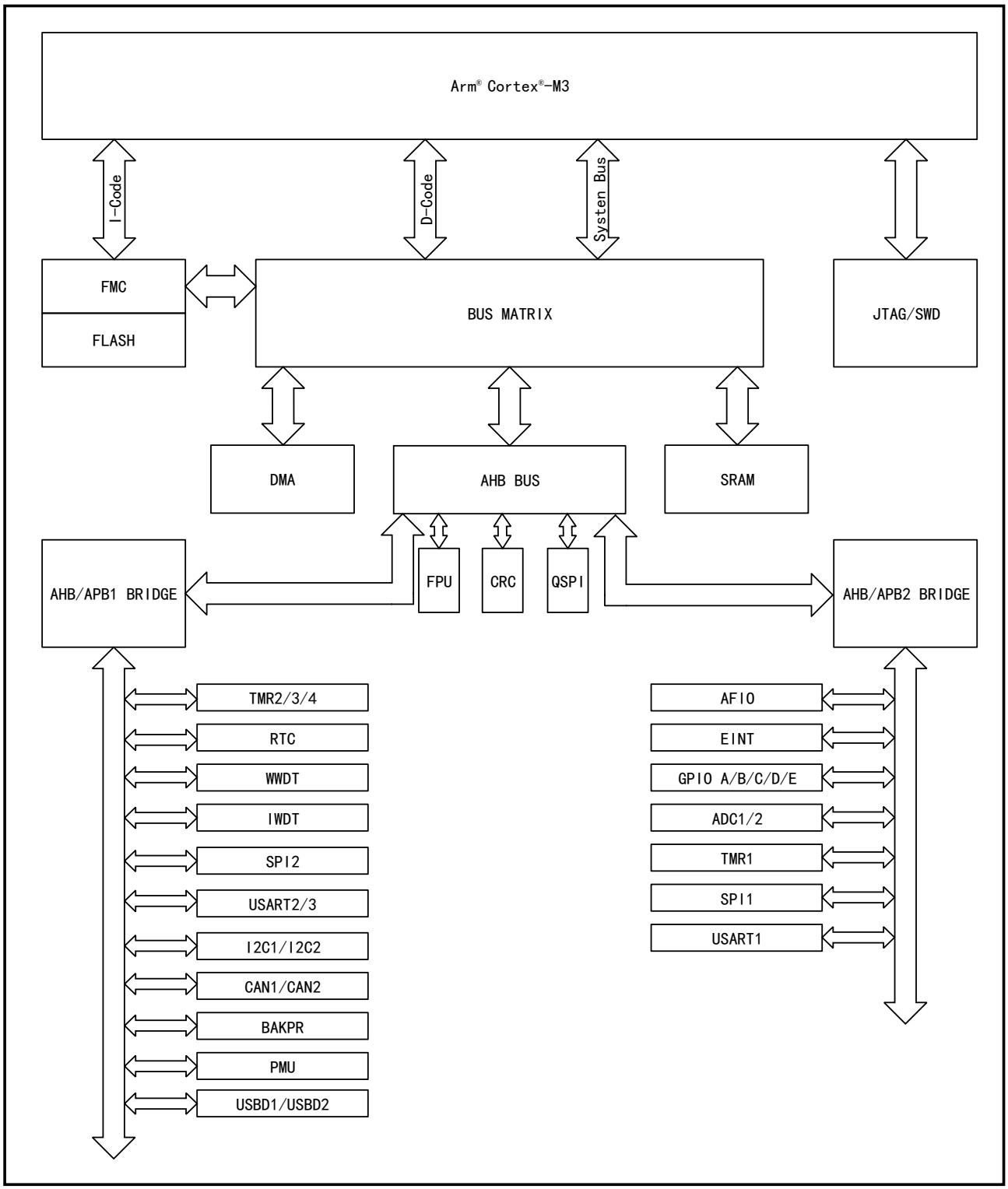
4. Functional description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32S103x8xB series products; for information about the Arm® Cortex®-M3 core, please refer to the Arm® Cortex®-M3 technical reference manual, which can be downloaded from Arm's website.

4.1. System architecture

4.1.1. System block diagram

Figure 5 APM32S103x8xB System Block Diagram



4.1.2. Address mapping

Table 4 APM32S103x8xB Storage Mapping Table

Region	Start Address	Peripheral Name
Code	0x0000 0000	Mapping area
Code	0x0800 0000	Flash
Code	0x0801 FFFF	Reserved
Code	0x1FFF F000	System Memory
Code	0x1FFF F800	Option Bytes
Code	0x1FFF F80F	Reserved
SRAM	0x2000 0000	SRAM
—	0x2000 4000	Reserved
APB1 bus	0x4000 0000	TMR2
APB1 bus	0x4000 0400	TMR3
APB1 bus	0x4000 0800	TMR4
APB1 bus	0x4000 0C00	Reserved
APB1 bus	0x4000 2800	RTC
APB1 bus	0x4000 2C00	WWDT
APB1 bus	0x4000 3000	IWDT
APB1 bus	0x4000 3400	Reserved
APB1 bus	0x4000 3800	SPI2
APB1 bus	0x4000 3C00	Reserved
APB1 bus	0x4000 4400	USART2
APB1 bus	0x4000 4800	USART3
APB1 bus	0x4000 4C00	Reserved
APB1 bus	0x4000 5400	I2C1
APB1 bus	0x4000 5800	I2C2
APB1 bus	0x4000 5C00	USBD1/ USBD2
APB1 bus	0x4000 6000	USBD/CAN SRAM
APB1 bus	0x4000 6400	CAN1

Region	Start Address	Peripheral Name
APB1 bus	0x4000 6800	CAN2
APB1 bus	0x4000 6C00	BAKPR
APB1 bus	0x4000 7000	PMU
—	0x4000 7400	Reserved
APB2 bus	0x4001 0000	AFIO
APB2 bus	0x4001 0400	EINT
APB2 bus	0x4001 0800	Port A
APB2 bus	0x4001 0C00	Port B
APB2 bus	0x4001 1000	Port C
APB2 bus	0x4001 1400	Port D
APB2 bus	0x4001 1800	Port E
APB2 bus	0x4001 1C00	Reserved
APB2 bus	0x4001 2400	ADC1
APB2 bus	0x4001 2800	ADC2
APB2 bus	0x4001 2C00	TMR1
APB2 bus	0x4001 3000	SPI1
APB2 bus	0x4001 3400	Reserved
APB2 bus	0x4001 3800	USART1
APB2 bus	0x4001 3C00	Reserved
AHB bus	0x4002 0000	DMA
AHB bus	0x4002 0400	Reserved
AHB bus	0x4002 1000	RCM
AHB bus	0x4002 1400	Reserved
AHB bus	0x4002 2000	Flash Interface
AHB bus	0x4002 2400	Reserved
AHB bus	0x4002 3000	CRC
AHB bus	0x4002 3400	Reserved
AHB bus	0x4002 4000	FPU

Region	Start Address	Peripheral Name
AHB bus	0x4002 4400	Reserved
AHB bus	0xA000 0000	QSPI
—	0xA000 2000	Reserved

4.1.3. Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

4.2. Core

The core of APM32S103x8xB is Arm® Cortex®-M3. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3. Interrupt controller

4.3.1. Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 47 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M3) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2. External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

4.4. On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

Table 5 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	128 KB	Store user programs and data.
SRAM	36 KB	CPU can access at 0 waiting cycle (read/write).
System memory area	2KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information

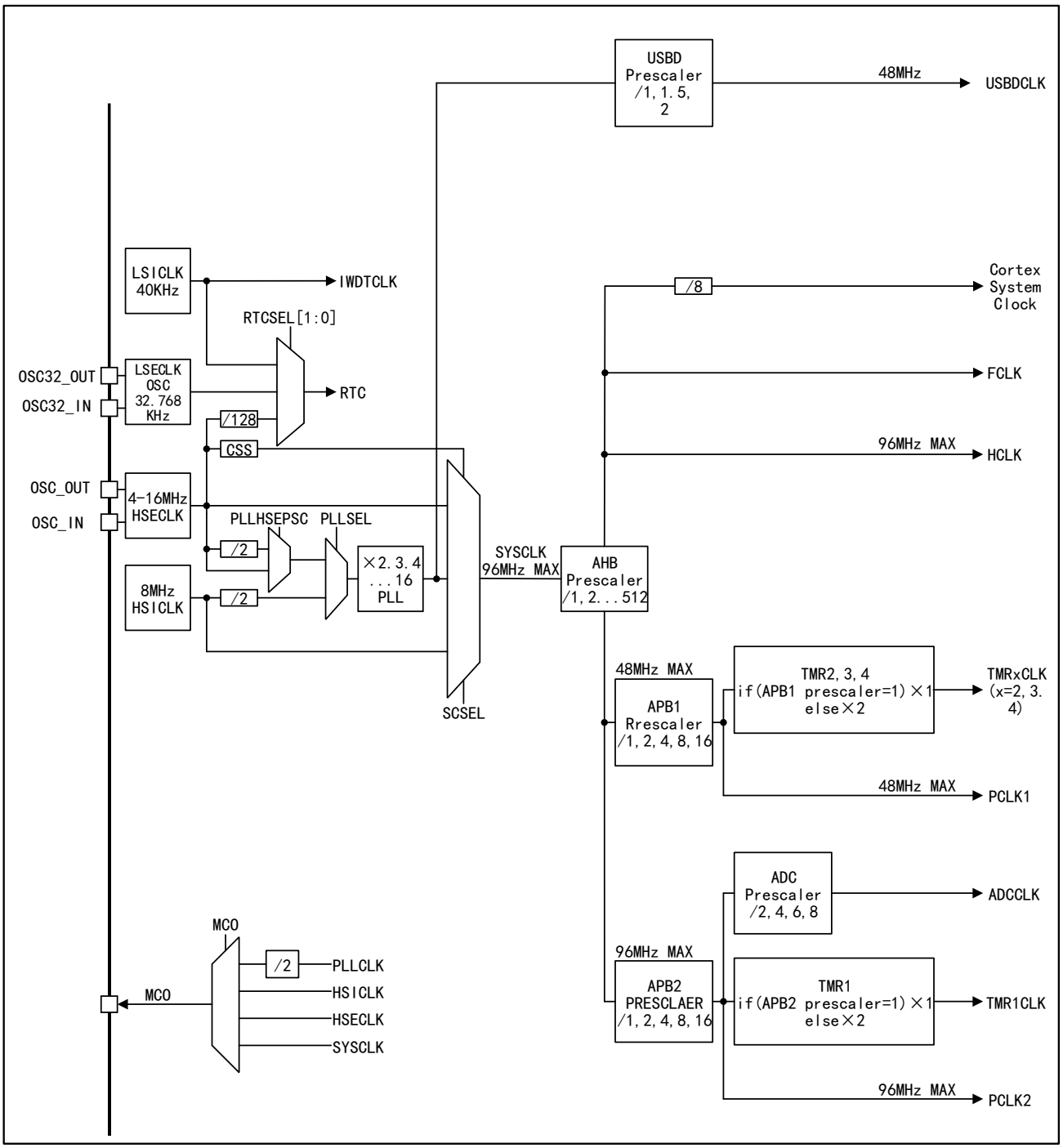
Memory	Maximum capacity	Function
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.5. Clock

4.5.1. Clock tree

Clock tree of APM32S103x8xB is shown in the figure below:

Figure 6 APM32S103x8xB Clock Tree



4.5.2. Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSICLK and LSICLK, and the external clock includes HSECLK and LSECLK, among which HSICLK is calibrated by the factory to ±1% accuracy.

4.5.3. System clock

HSICLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be one of HSICLK, and HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency dividing coefficient.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.4. Bus clock

AHB, APB1 and ABP2 are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency dividing coefficient. The maximum frequency of AHB and high-speed APB2 is 96MHz, and the maximum frequency of APB1 is 48MHz.

4.6. Power Supply and power management

4.6.1. Power supply scheme

Table 6 Power Supply Scheme

Name	Voltage range	Instruction
V_{DD}	2.0～3.6V	I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDA}/V_{SSA}	2.0～3.6V	Power supply of ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is used, V_{DDA} shall not be less than 2.4V; V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.
V_{BAT}	1.8～3.6V	When V_{DD} is closed, RTC, external 32KHz oscillator and backup register are supplied through internal power switch.

4.6.2. Voltage regulator

Table 7 Regulator Operating Mode

Name	Instruction
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3. Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7. Low-power mode

APM32S103x8xB supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 8 Low Power Consumption Mode

Mode	Instruction
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.5V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USBD.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.5V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8. DMA

1 built-in DMA; DMA supports 7 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" transfer of data (the memory includes Flash、SRAM)

4.9. GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input、output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.10. Communication peripherals

4.10.1. USART

Up to 3 USART in the chip. The USART1 interface can communicate at a rate of 4.5Mbit/s, while other USART interfaces can communicate at a rate of 2.25Mbit/s. All USART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; all the other USART can support DMA.

4.10.2. I2C

I2C1/2 both can work in multiple master modes or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

4.10.3. SPI

Two built-in SPIs (the quantity depends on the model), support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

4.10.4. QSPI

1 built-in QSPI special communication interface, which can connect external flash through single, double line or four line SPI mode, and supports 8-bit, 16 bit and 32-bit access. There are 8 bytes of transmit FIFO and 8 bytes of receive FIFO.

4.10.5. CAN

2 built-in CANs (CAN1 and CAN2 can be used at the same time), compatible with 2.0A and 2.0B (active) specification, and can communicate at a rate of up to 1Mbit/s. It can receive and send standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes and 2 receiving FIFO, 14 3-level adjustable filters.

4.10.6. USBD

The product embeds USBD modules (USBD1 and USBD2) compatible with full-speed USBD devices, which comply with the standard of full-speed USBD devices (12Mb/s), and the endpoints can be configured by software, and have standby/wake-up functions. The dedicated 48MHz clock for USBD is directly generated by internal PLL. When using the USBD function, the system clock can only be one of 48MHz, 72MHz, and 96MHz, which can obtain 48MHz required for USBD through 1 fractional frequency, 1.5 fractional frequency, and 2 fractional frequency respectively.

USBD1 and USBD2 share register address and pin interface, so only one of them can be used at the same time

4.11. Analog peripherals

4.11.1. ADC

2 built-in ADCs with 12-bit accuracy, up to 16 external channels and 2 internal channels for each ADC. The internal channels measure the temperature sensor voltage and reference voltage respectively. A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16 bit data register; they support analog watchdog, and DMA.

4.11.1.1. Temperature sensor

A temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

4.11.1.2. Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.12. Timer

1 built-in 16-bit advanced timers (TMR1), 3 general-purpose timers (TMR2/3/4), 1 independent

watchdog timer, 1 window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 9 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	**System tick timer**	**General-purpose timer**			**Advanced timer**
Timer name	Sys Tick Timer	TMR2	TMR3	TMR4	TMR1
Counter resolution	24-bit	16-bit			16-bit
Counter type	Down	Up, down, up/down			Up, down, up/down
Prescaler coefficient	-	Any integer between 1 and 65536			Any integer between 1 and 65536
General DMA request	-	OK			OK
Capture/Comparison channel	-	4			4
Complementary outputs	-	No			Yes
Pin characteristics	-	There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins			There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins, 3-pair complementary channel pins, 1-way channel (non-complementary channel) pins
Function Instruction	Special for real-time operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	Synchronization or event chaining function provided Timers in debug mode can be frozen. Can be used to generate PWM output Each timer has independent DMA request generation. It can handle incremental encoder signals			It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table 10 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler coefficient	Functional Description
Independent watchdog	12-bit	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.13. RTC

1 RTC is built in, and there are LSECLK signal input pins (OSC32_IN and OSC32_OUT) and 1 TAMP input signal detection pin (TAMP); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data are not lost in case of system resetting, software resetting and power resetting; it supports clock and calendar functions.

4.13.1. Backup register

84Bytes backup register is built in, and is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system resetting, software resetting and power resetting.

4.14. CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

4.15. FPU

The product has built-in independent FPU floating-point operation processing unit, supports IEEE754 standard, supports single-precision floating-point operation, and supports algorithms such as CMP, SUM, SUB, PRDCT, MAC, DIV, INVRGSQT, RGSQT, SUMSQ, DOT, floating-point to integer conversion and integer to floating point conversion.

5. Electrical characteristics

5.1. Test conditions of electrical characteristics

5.1.1. Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at TA=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2. Typical values

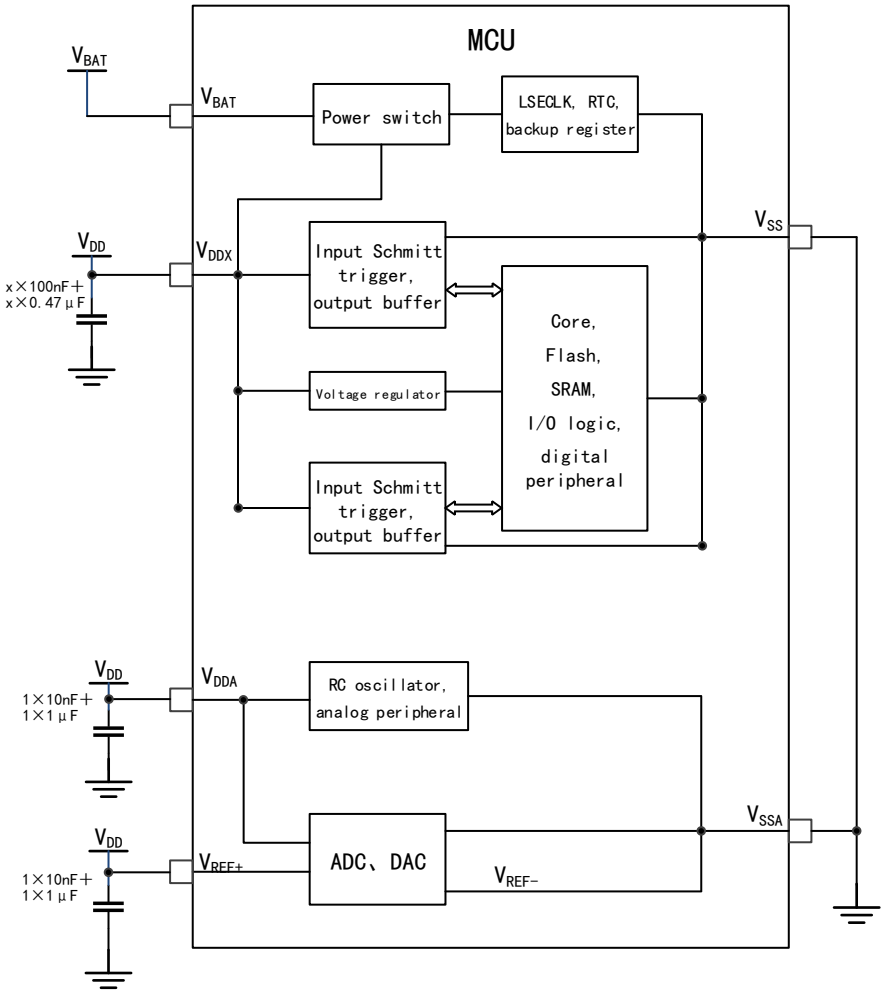
Unless otherwise specified, typical data are measured based on TA=25℃, V_{DD}=V_{DDA}=3.3V. these data are only used for design guidance.

5.1.3. Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4. Power supply scheme

Figure 7 Power Supply Scheme



Notes: V_{DD}x in the figure means the number of V_{DD} is x

5.1.5. Load capacitance

Figure 8 Load conditions when measuring pin parameters

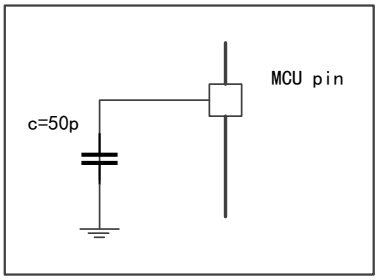


Figure 9 Pin Input Voltage Measurement Scheme

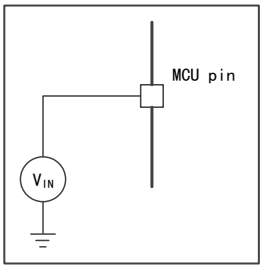
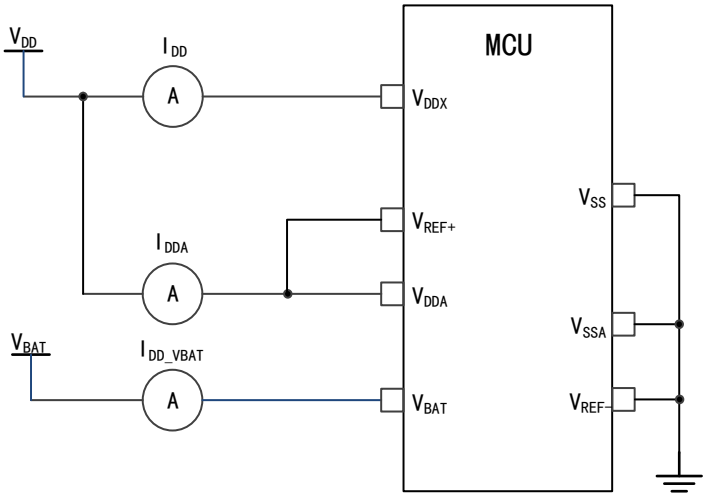


Figure 10 Power Consumption Measurement Scheme



5.2. Test under general operating conditions

Table 11 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	48	
f_{PCLK2}	Internal APB2 clock frequency	-	-	96	
V_{DD}	Main power supply voltage	-	2	3.6	V
V_{DDA}	Analog power supply voltage (When neither ADC nor DAC is used)	Must be the same as V_{DD}	V_{DD}	3.6	V
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.8	3.6	V
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	℃
	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	℃

5.3. Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent

damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1. Maximum temperature characteristics

Table 12 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	℃
T_J	Maximum junction temperature	150	℃

5.3.2. Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 13 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog power supply voltage	-0.3	4.0	
V_{BAT}-V_{SS}	Power supply voltage of external backup domain	-0.3	4.0	
V_{DD}-V_{DDA}	Voltage difference allowed by V_{DD}>V_{DDA}	-	0.3	
V_{IN}	Input voltage on FT pins	V_{SS}-0.3	5.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}$-$V_{SS} \rvert$	Voltage difference between different grounding pins	-	50	

5.3.3. Maximum rated current features

Table 14 Current Characteristics

Symbol	Description	Maximum	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Irrigation current on any I/O and control pins	25	
	Source current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2) (3)	Injection current of 5T pin	±5	
	Injection current of other pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins(5)	±25	

Note:

(1) All power (V_{DD}，V_{DDA}) and ground (V_{SS}，V_{SSA}) pins must always be connected to a power supply within the external allowable range.

(2) Negative injection disturbs the analog performance of the device.

(3) Positive injection is not possible on these I/Os. a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

(4) A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

(5) When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4. Electrostatic discharge (ESD)

Table 15 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 ℃, conforming to ANSI/ESDA/JEDEC JS-001-2017	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 ℃, conforming to ANSI/ESDA/JEDEC JS-002-2018	500	

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5. Static latch-up (LU)

Table 16 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A = +25 ℃/105℃, conforming to EIA/JESD78E	Ⅱ level A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4. On-chip memory

5.4.1. Flash characteristics

Table 17 Flash Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
t_{prog}	16-bit programming time	T_A = -40~105℃ V_{DD}=2.4~3.6V	50	56	60	μs
t_{ERASE}	Page (2KBytes) erase time	T_A = -40~105℃ V_{DD}=2.4~3.6V	6	9	10	ms
t_{ME}	Whole erase time	T_A = -40~105℃ V_{DD}=2.4~3.6V	4	9	10	ms
V_{prog}	Programming voltage	T_A = -40~105℃	2	-	3.6	V

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5. Clock

5.5.1. Characteristics of external clock source

High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 18 HSECLK4~16MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistance	-	-	170	-	kΩ
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, CL=10pF@8MHz	-	281	-	mA
I_2	Drive current	-	-	-	2.35	mA
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable	-	2	-	ms
$Duty_{(HSECLK)}$	HSECLK duty cycle	-	45	-	55	%

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 19 LSECLK Oscillator Characteristics (f_{LSECLK}=32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{OSF_IN}	Oscillator frequency	-	-	32.768	-	KHz
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	1.27	-	μA
I_2	Drive current	-	-	-	2.2	μA
$t_{SU(LSECLK)}$(1)	Startup time	V_{DDIOx} is stable	-	2	-	s

Note: It is obtained from a comprehensive evaluation and is not tested in production.

（1） $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2. Characteristics of internal clock source

High speed internal (HSICLK) RC oscillator

Table 20 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
f_{HSICLK}	Frequency	-	-	8	-	MHz

Symbol	Parameter	Conditions		Min	Type	Max	Unit
$A_{CCHSICLK}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-2	-	2.5	%
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	-	160	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V，T_A=-40~105℃		0.8	-	2	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Low speed internal (LSICLK) RC oscillator

Table 21 LSICLK Oscillator Characteristics

Symbol	Parameter	Min	Type	Max	Unit
f_{LSICLK}	Frequency (V_{DD} =2-3.6V, T_A =-40~105℃)	30	42	60	KHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.73	-	μA
$t_{SU(LSICLK)}$	LSICLK oscillator startup time, (V_{DD}=3.3V, T_A=-40~105℃)	-	-	82	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.3. PLL Characteristics

Table 22 PLL Characteristics

Symbol	Parameter	Numerical Value			Unit
		Minimum value	Typical values	Maximum value	
f_{PLL_IN}	PLL input clock	1	8	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock, (V_{DD}=3.3V, T_A=-40~105℃)	16	-	96	MHz
t_{LOCK}	PLL phase locking time	-	-	250	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.6. Reset and power management

5.6.1. Test of embedded reset and power control block characteristics

Table 23 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.86	1.87	1.88	V
		Rising edge	1.90	1.92	1.93	V
$V_{PDRhyst}$	PDR hysteresis	-	45	50	55	mV
$T_{RSTTEMPO}$	Reset duration	-	2	-	4.5	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 24 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.14	2.17	2.19	V
		PLS[2:0]=000 (falling edge)	2.04	2.07	2.08	V
		PLS[2:0]=000(PVD hysteresis)	100.00	101.11	110.00	mV
		PLS[2:0]=001 (rising edgeg)	2.24	2.27	2.29	V
		PLS[2:0]=001 (falling edge)	2.13	2.16	2.18	V
		PLS[2:0]=001(PVD hysteresis)	109.00	110.00	111.00	mV
		PLS[2:0]=010 (rising edgeg)	2.34	2.37	2.39	V
		PLS[2:0]=010 (falling edge)	2.23	2.26	2.28	V
		PLS[2:0]=010(PVD hysteresis)	100.00	107.78	110.00	mV
		PLS[2:0]=011 (rising edgeg)	2.43	2.47	2.48	V
		PLS[2:0]=011 (falling edge)	2.33	2.36	2.38	V
		PLS[2:0]=011(PVD hysteresis)	100.00	103.33	110.00	mV
		PLS[2:0]=100 (rising edgeg)	2.53	2.57	2.58	V
		PLS[2:0]=100 (falling edge)	2.43	2.46	2.47	V
		PLS[2:0]=100(PVD hysteresis)	100.00	110.00	110.00	mV
		PLS[2:0]=101 (rising edgeg)	2.63	2.66	2.68	V
		PLS[2:0]=101 (falling edge)	2.53	2.56	2.58	V
		PLS[2:0]=101(PVD hysteresis)	90.00	102.22	110.00	mV
		PLS[2:0]=110 (rising edgeg)	2.73	2.76	2.78	V
		PLS[2:0]=110 (falling edge)	2.62	2.65	2.67	V
		PLS[2:0]=110(PVD hysteresis)	100.00	107.78	110.00	mV
		PLS[2:0]=111 (rising edgeg)	2.82	2.85	2.87	V
		PLS[2:0]=111 (falling edge)	2.72	2.75	2.77	V
		PLS[2:0]=111(PVD hysteresis)	90.00	100.00	100.00	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.7. Power consumption

5.7.1. Power consumption test environment

（1） The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)

Unless otherwise specified, all peripherals are turned off

The relationship between Flash waiting cycle setting and f_{HCLK} :

0~24MHz: 0 waiting cycle

24~48MHz: 1 waiting cycle

48~72MHz: 2 waiting cycles

72~96MHz: 3 waiting cycles

The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)

When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/2$， $f_{PCLK2}=f_{HCLK}$

5.7.2. Power consumption in run mode

Table 25 Power Consumption in Run Mode when the Program is Executed in Flash/RAM

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2), enabling all peripherals	96MHz	294.22	23.68	326.20	25.30
		72MHz	187.31	16.97	207.06	18.27
		48MHz	139.58	13.73	153.64	14.83
		36MHz	104.35	10.45	115.28	11.51
		24MHz	76.46	7.51	86.20	8.56
		16MHz	59.67	5.18	69.26	6.20
		8MHz	4.44	2.76	5.42	3.69
	HSECLK bypass (2), turning off all peripherals	96MHz	293.73	14.19	325.69	15.00
		72MHz	187.12	10.60	206.76	11.37
		48MHz	139.39	8.91	153.53	9.60
		36MHz	104.28	6.82	115.19	7.47
		24MHz	76.38	5.09	86.2	5.85
		16MHz	59.57	3.58	69.25	4.30
		8MHz	4.44	1.97	5.4	2.69
	HSICLK (2), enabling all peripherals	72MHz	251.29	16.65	267.90	17.38
		48MHz	203.14	12.61	216.89	13.22
		32MHz	169.61	10.14	182.42	10.78
		24MHz	139.84	6.87	152.90	7.45
		16MHz	123.15	4.94	136.65	5.53
	HSICLK (2), turning off all peripherals	72MHz	251.21	10.24	267.90	10.69
		48MHz	203.19	7.72	216.95	8.24
		32MHz	169.65	6.51	182.39	7.01
		24MHz	139.82	4.46	153.00	4.97
		16MHz	123.05	3.32	136.73	3.87

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.3. Power consumption in sleep mode

Table 26 Power Consumption in Sleep Mode when the Program is Executed in Flash

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in sleep mode	HSECLK bypass (2) , enabling all peripherals	96 MHz	293.83	16.25	325.72	17.00
		72MHz	187.08	11.08	206.84	11.67
		48MHz	139.42	8.40	153.49	9.01
		36MHz	104.27	6.42	115.27	7.00
		24MHz	76.40	4.38	86.28	5.00
		16MHz	59.64	3.03	69.29	3.68
		8MHz	4.43	1.65	5.4	2.27
	HSECLK bypass (2) , turning off all peripherals	96 MHz	293.36	4.68	325.34	5.21
		72MHz	186.93	3.26	206.62	3.80
		48MHz	139.32	2.55	153.43	3.10
		36MHz	104.21	2.00	115.15	2.54
		24MHz	76.30	1.48	86.22	2.02
		16MHz	59.49	1.13	69.28	1.69
		8MHz	4.43	0.68	5.4	1.24
	HSICLK (2) , enabling all peripherals	72MHz	206.69	10.78	218.44	11.7
		48MHz	158.91	8.16	167.41	9.13
		36MHz	124.43	6.19	131.22	7.11
		24MHz	95.99	4.19	102.67	5.12
		16MHz	79.34	2.89	86.24	3.78
	HSICLK (2) , turning off all peripherals	72MHz	206.50	3.08	218.56	3.93
		48MHz	158.83	2.37	167.53	3.23
		36MHz	124.31	1.83	131.33	2.69
		24MHz	95.94	1.31	102.74	2.16
		16MHz	79.30	0.95	86.36	1.82

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL

5.7.4. Power consumption in stop mode and standby mode

Table 27 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions	Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)		Unit
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=105℃		
		I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	
Power consumption in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	3.96	23.73	4.42	23.71	4.61	24.67	5.44	457.80	μA
	Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	3.96	9.3	4.41	9.26	4.58	9.08	5.43	405.80	
Power consumption in standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.40	0.17	3.04	0.34	3.30	0.39	3.81	4.74	
	Low-speed internal RC oscillator on, independent watchdog OFF	2.4	0.05	3.04	0.16	3.30	0.22	3.81	4.41	
	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	2.03	0.01	2.5	0.01	2.68	0.01	3.23	3.95	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.5. Backup domain power consumption

Table 28 Backup Domain Power Consumption

Symbol	Conditions	Typical value (1), T_A=25℃			Maximum value (1), V_{BAT}=3.6V			Unit
		V_{BAT}=2.0V	V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=25℃	T_A=85℃	T_A=105℃	
$I_{DD}\_V_{BAT}$	The low-speed oscillator and RTC are in ON state	1.2	1.3	1.5	1.7	2.2	2.7	μA

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.6. Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 29 Peripheral Power Consumption

Parameter	Peripheral	Typical value [1] T_A =25℃, V_{DD} =3.3V	Unit
AHB	DMA1	1.06	mA
	CRC	0.80	
APB1	TMR2	1.34	
	TMR3	1.31	
	TMR4	1.33	
	WWDT	0.88	
	IWDT	0.06	
	SPI2	0.82	
	USART2	0.93	
	USART3	0.92	
	I2C1	0.93	
	I2C2	0.94	
	USBD	1.23	
	CAN1	1.05	
	CAN2	1.09	
	BAKPR	0.85	
	PMU	0.85	
	DAC	0.74	
APB2	GPIOA	0.96	
	GPIOB	0.96	
	GPIOC	0.93	
	GPIOD	0.96	
	GPIOE	0.95	
	ADC1	1.34	
	ADC2	1.28	
	TMR1	1.57	
	SPI1	0.97	
	USART1	1.15	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.8. Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the

time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 30 Wake Up Time in Low-power Mode

Symbol	Parameter	Conditions	Typical value (T_A=25℃)	Maximum value			Unit	Symbol
				2V	3.3V	3.6V		
$t_{WUSLEEP}$	Wake-up from sleep mode	-	0.51	0.558	0.567	0.575	0.64	μs
t_{WUSTOP}	Wake up from stop mode	The voltage regulator is in run mode	2.05	2.491	2.221	2.179	2.59	
		The voltage regulator is in low power mode	2.85	5.122	3.551	3.440	5.61	
$t_{WUSTDBY}$	Wake up from standby mode	-	57.29	81.59	68.96	68.11	93.69	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.9. Pin characteristics

5.9.1. I/O pin characteristics

Table 31 DC Characteristics (test condition of V_{DD}=2.7~3.6V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{IL}	Low level input voltage	CMOS port	-0.5	-	0.35VDD	V
V_{IH}	High level input voltage		0.7VDD	-	VDD+0.5	
V_{IL}	Low level input voltage	TTL port	-0.5	-	0.8	
V_{IH}	Standard I/O High level input voltage		2	-	VDD+0.5	
	I/O FT Low level input voltage		2	-	5.5	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis	-	150	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis		5%VDD	-	-	mV
I_{lkg}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O port	-	-	±1	μA
		V_{IN}=5V, I/O FT port	-	-	4.6	
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{IN}=V_{DD}	30	40	50	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

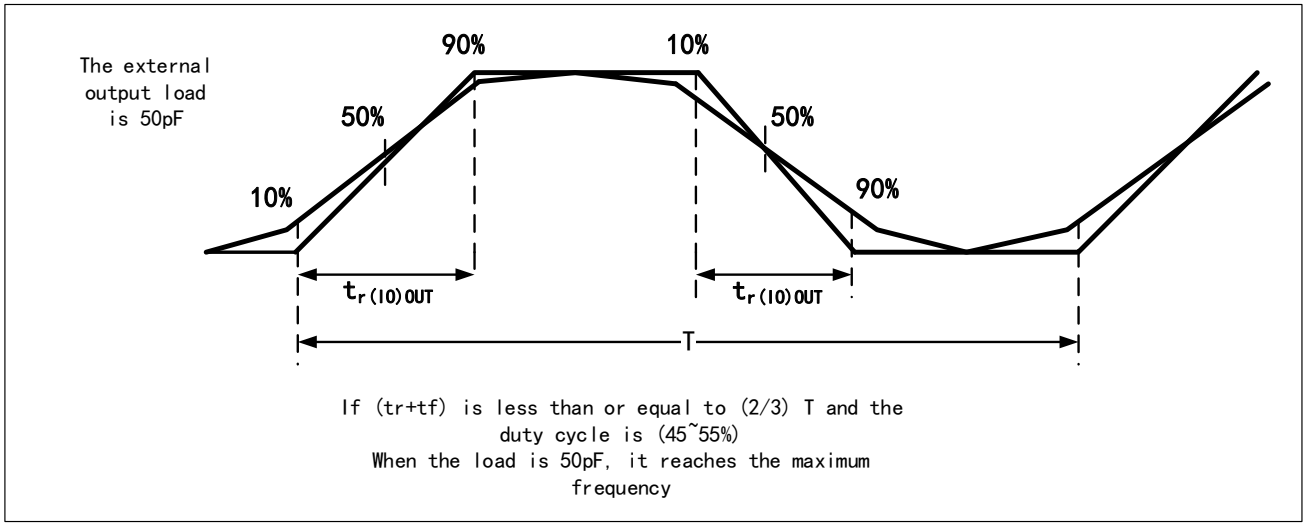
Table 32 AC Characteristics

MODEy[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency	CL=50 pF, V_{DD}=2~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	CL=50 pF, V_{DD} =2~3.6V	-	125	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	125	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency	CL=50 pF, V_{DD} =2~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	CL=50 pF, V_{DD} =2~3.6V	-	25	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	25	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency	CL=30 pF, V_{DD} =2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	CL=30 pF, V_{DD} =2.7~3.6V	-	6	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	6	

Note: (1) The rate of I/O port can be configured through MODEy.

(2) The data are obtained from a comprehensive evaluation and is not tested in production.

Figure 11 I/O AC Characteristics Definition



Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 33 Output Drive Current Characteristics (test condition V_{DD}=2.7~3.6V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	IIO = +8mA 2.7V<V_{DD}<3.6V	-	0.4	V

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-0.4	-	
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	IIO = +20mA 2.7V<V_{DD}<3.6V	-	1.3	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-1.3	-	

5.9.2. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 34 NRST Pin Characteristics (test condition V_{DD}=3.3V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Min	Type	Max	Unit
$V_{IL(NRST)}$	NRST low level input voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$	NRST high level input voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
RPU	Weak pull-up equivalent resistance	V_{IN} = V_{SS}	30	40	50	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.10. Communication peripherals

5.10.1. I2C peripheral characteristics

To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

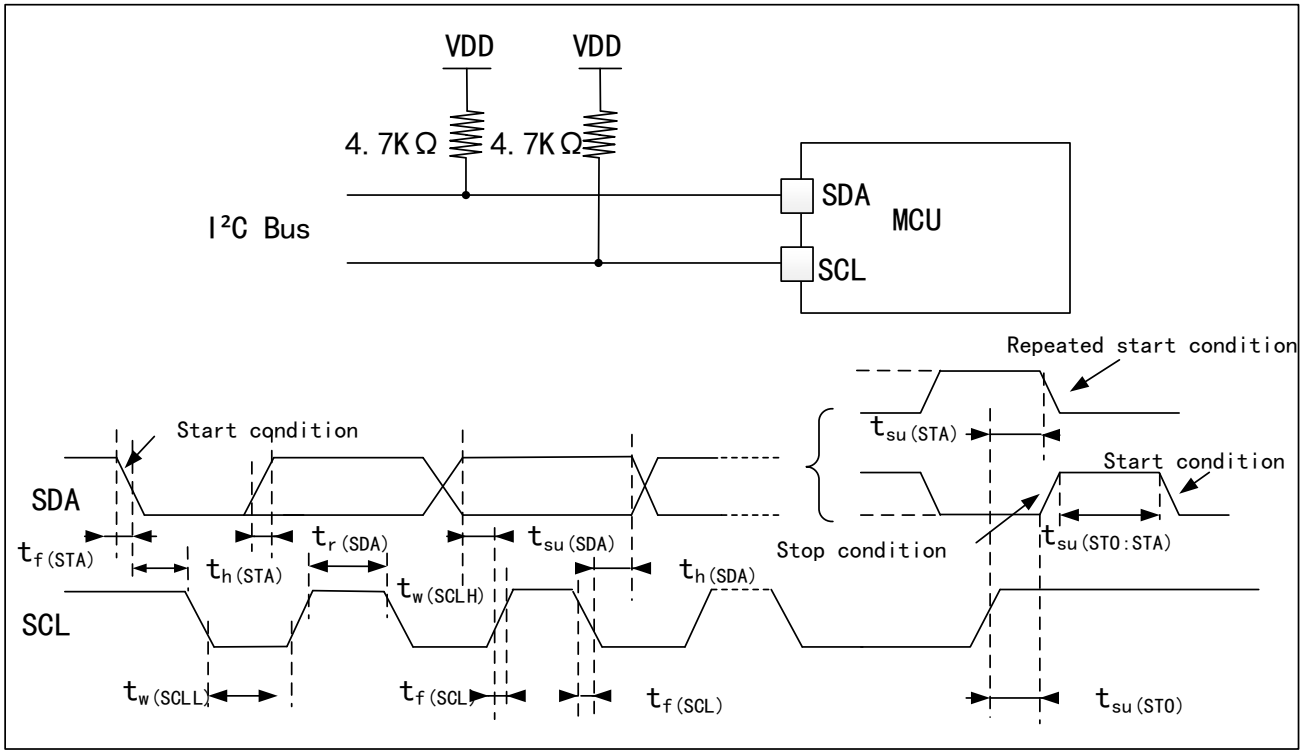
Table 35 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450	-	900	
$t_{r(SDA)}$/$t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$/$t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.9	-	0.8	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.9	-	0.8	-	
$t_{su(STO)}$	Setup time of stop condition	4.9	-	0.8	-	

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.9	-	1.7	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 12 I2C Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2. SPI peripheral characteristics

Table 36 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: C = 30pF	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Main mode, f_{PCLK} = 36MHz, Prescaler coefficient=4	50	60	ns
$t_{su(MI)}$	Data input setup time	Master mode	8	-	ns

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
$t_{su(SI)}$		Slave mode	18	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	30	-	ns
		Slave mode	22	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	3tPCLK	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	6		ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	7	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	12	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	2	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 13 SPI Timing Diagram - Slave Mode and CPHA=0

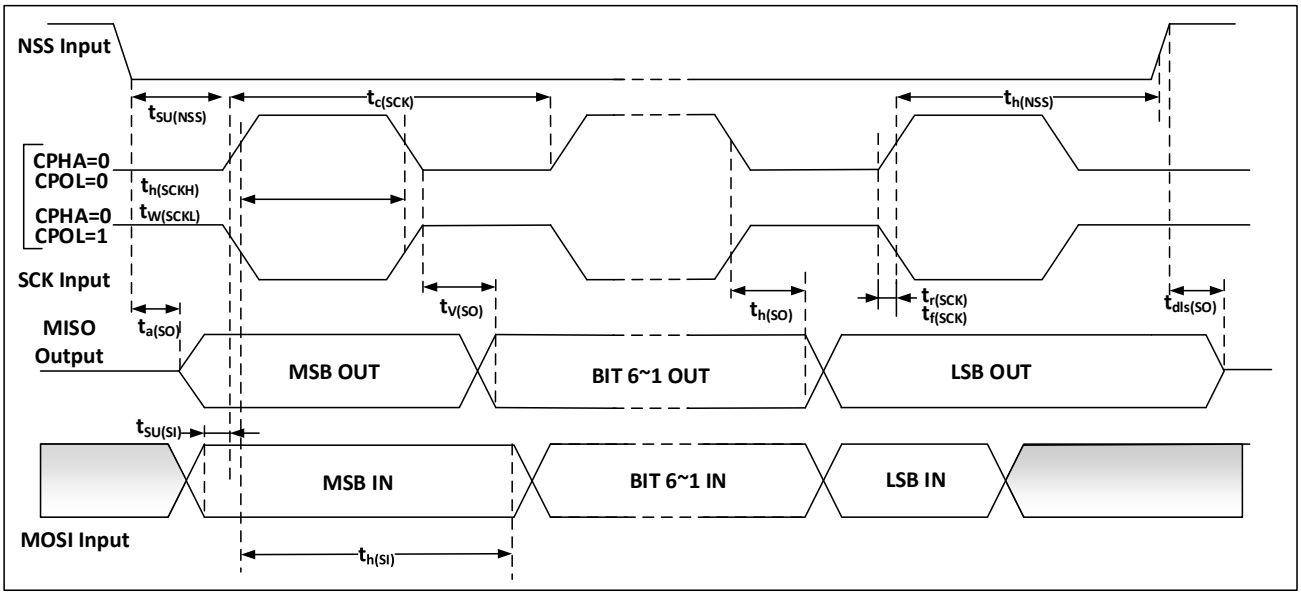
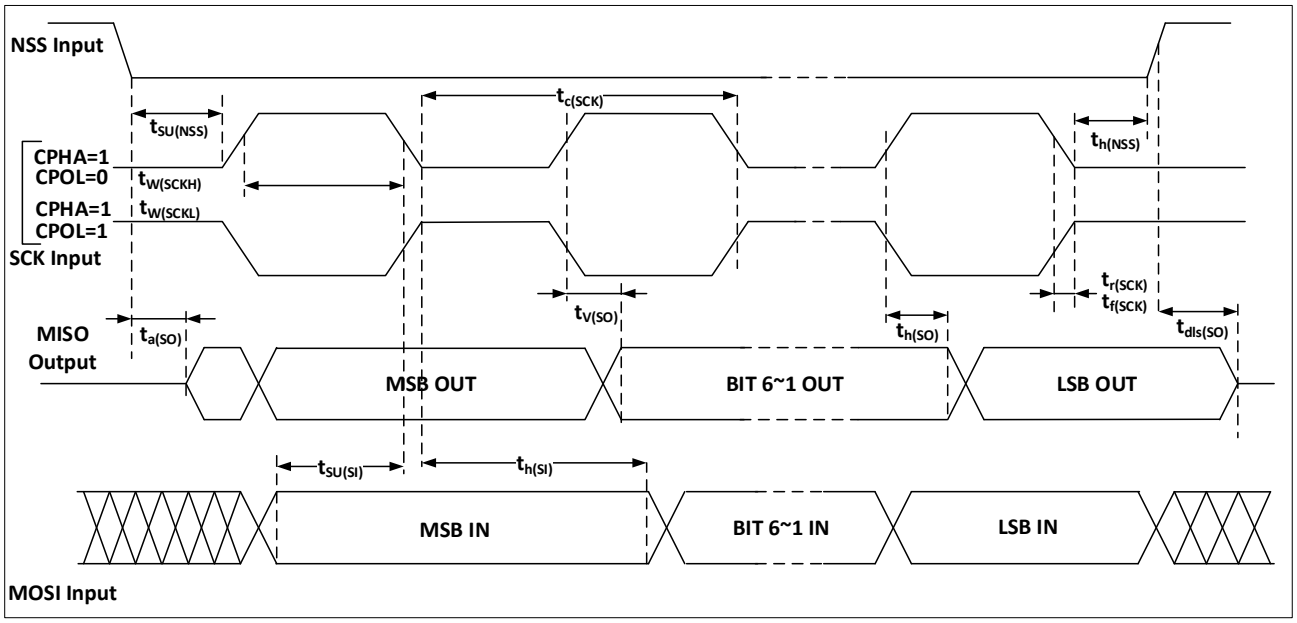
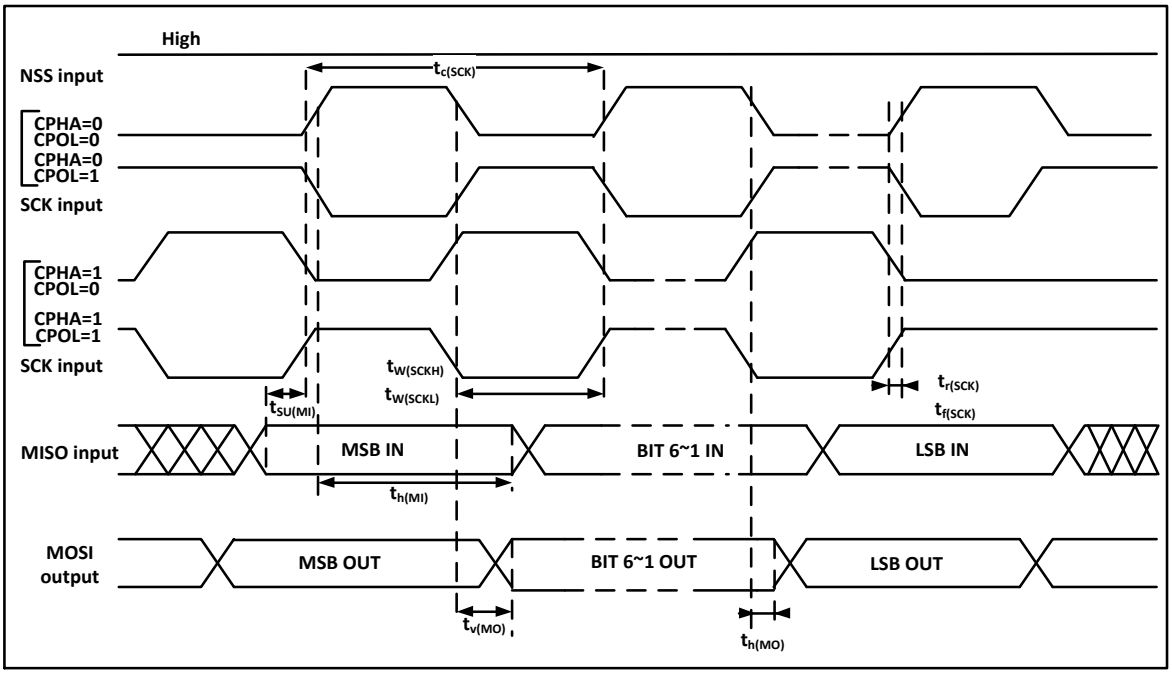


Figure 14 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 15 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.3. USBD peripheral characteristics

Figure 16 USBD Timing : Definition of Rise and Fall Time of Data Signal

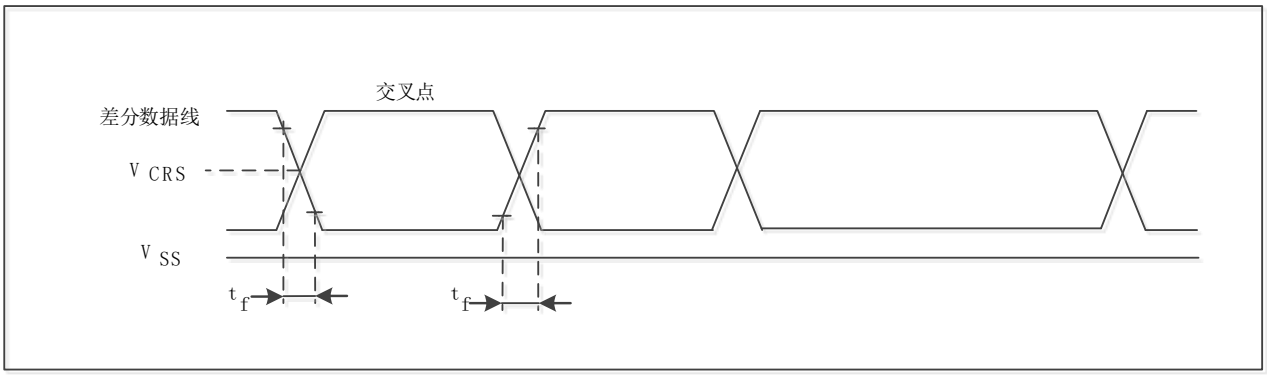


Table 37 USBD Characteristics （TA=25℃，VDD=3.0~3.6V）

Symbol	Parameter	Conditions	Min (1)	Max (1)	Unit
Input level					
V_{DD}	USBD Operating voltage (2)	-	3.0(3)	3.6(3)	V
V_{DI}(4)	Differential input sensitivity	I（USBDP，USBDM）	0.2	-	V
V_{CM}(4)	Differential common mode range	Include V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output level					
V_{OL}	Static output low level	RL of 1.5kΩ connected to 3.6V(5)	-	0.3	V
V_{OH}	Static output high level	RL of 15kΩ connected to V_{SS}(5)	2.8	3.6	

（1） All voltage measurements are based on the ground wire at the equipment end.

（2） In order to be compatible with USB2.0 full speed electrical specifications, the USBDP (D+) pin must be connected to 3.0~3.6V through a 1.5k Ω resistor.

（3） The correct USBD function of APM32S103xx can be guaranteed at 2.7 V, rather than the degraded electrical characteristics at 2.7~3.0 V.

（4） There is a comprehensive evaluation guarantee, and it will not be tested in production.

（5） RL is the load connected to the USBD drive.

Table 38 USBD Full speed electrical characteristics（TA=25℃，VDD=3.0~3.6V，）

符号	参数	条件	最小值	最大值	单位
t_r	Rise time	C_L = 50pF	4	20	ns

符号	参数	条件	最小值	最大值	单位
t_f	Fall time	C_L = 50pF	4	20	ns
t_{rfm}	Rise and fall time matching	t_r / t_f	90	110	%
V_{CRS}	Output signal cross voltage	-	1.3	2.0	V

5.11. Analog peripherals

5.11.1. ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second
- Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.11.1.1. 12-bit ADC characteristics

Table 39 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{DDA}	Power supply voltage	-	2.4	-	3.6	V
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	-	8	pF
R_{ADC}	Sampling resistor	-	-	-	1	Ω
t_S	Sampline Time	f_{ADC}=14MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz, 12-bit conversion	1	-	18	μs

Table 40 12-bit ADC Accuracy

Symbol	Parameter	Conditions	Typical values	Maximum value	Unit
|ET|	Composite error	f_{PCLK}=56MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	±2.5	±5.5	LSB
|EO|	Offset error		±2.1	±3.5	
|EG|	Gain error		±2.5	±4	
|ED|	Differential linear error		±1.5	±2.5	
|EL|	Integral linear error		±1.8	±3	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.2. Test of Built-in Reference Voltage Characteristics

Table 41 Embedded Reference Voltage Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < T_A < +105℃ V_{DD}= 2-3.6 V	1.16	1.20	1.26	V
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1	μs
V_{RERINT}	Built-in reference voltage extends to temperature range	V_{DD}=3V ±10mV	-	-	18	mV
T_{coeff}	Temperature coefficient	-	-	-	123	ppm/℃

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.3. Temperature sensor Characteristics

Table 42 Temperature sensor Characteristics

符号	参数	最小值	典型值	最大值	单位
Avg_Slope 错误!未找到引用源。	Average slope（V_{DD} = 3.3V，TA = -40~105℃）	3.8	3.9	4.0	mV/ºC
V_{25}	Voltage at 25 º C（V_{DD} = 2~3.6V）	1.42	1.43	1.45	V
t_{START} 错误!未找到引用源。	Setup Time	4		10	μs
T_{S_temp} 错误!未找到引用源。错误!未找到引用源。	ADC sampling time when reading temperature			17.1	μs

(1) Data is guaranteed by analysis on features, and is not tested in production.

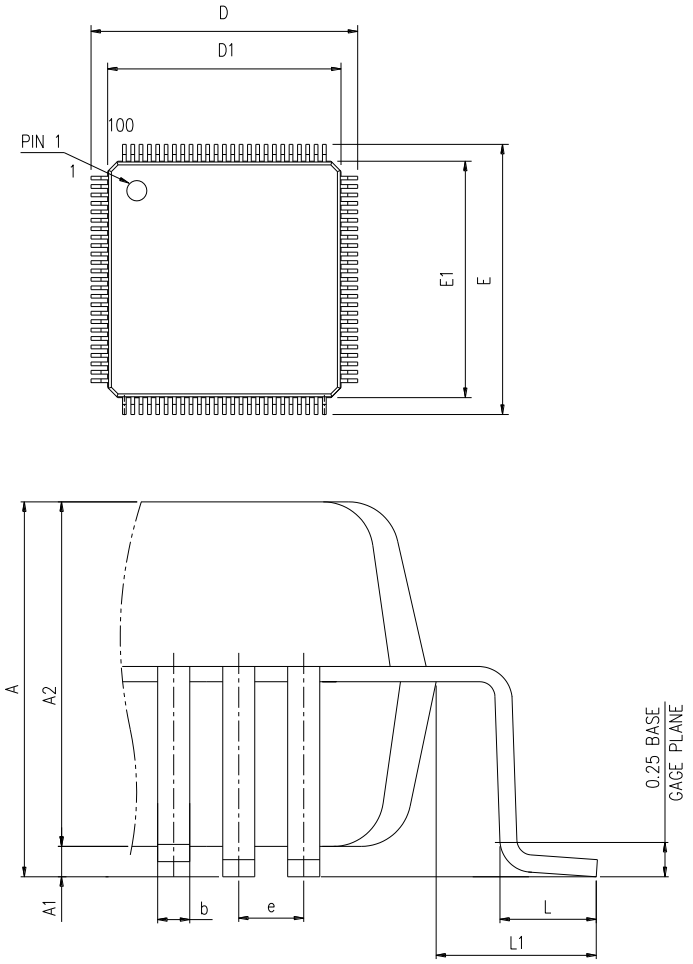
(2) Data is guaranteed from design, and is not tested in production.

(3) The shortest sampling Time can be determined by the application through multiple iterations.

6. Package information

6.1. LQFP100 package diagram

Figure 17 LQFP100 Package Diagram



（1） The figure is not drawn to scale.

（2） All pins should be soldered to the PCB

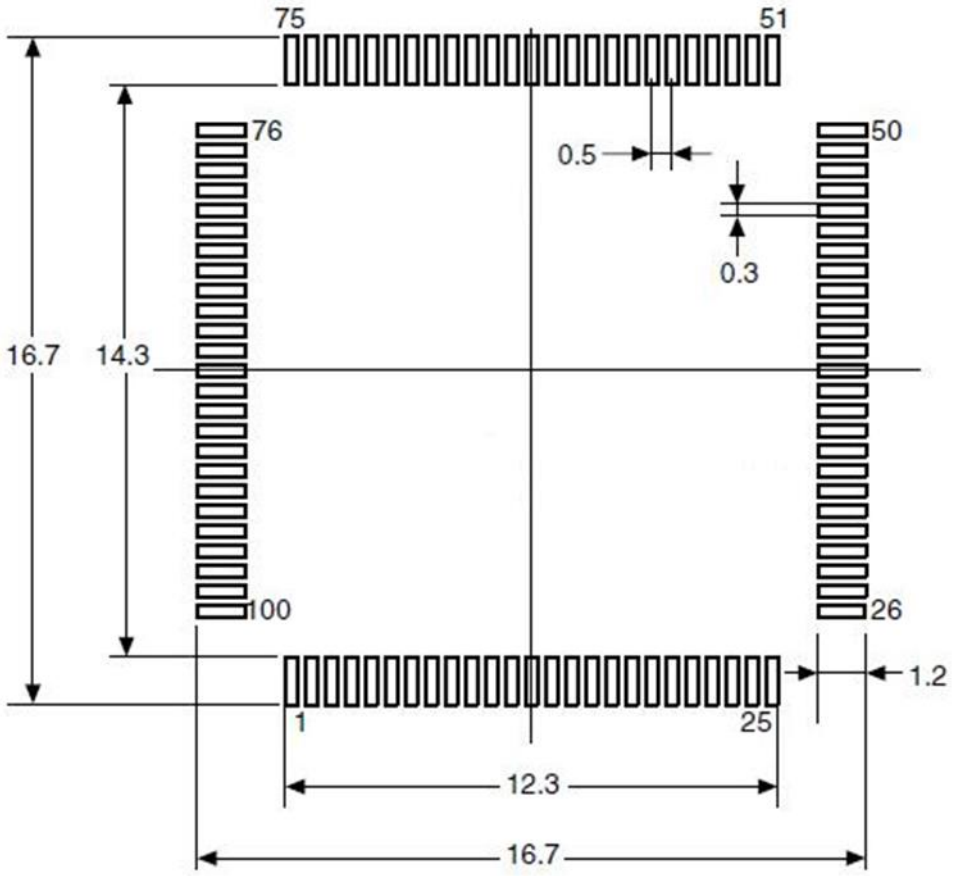
Table 43 LQFP100 Package Data

S/N	SYM	Millimeters		
		Min	Typ	Max
1	A	-	-	1.60
2	A1	0.05	-	0.15
3	A2	1.35	1.40	1.45
4	D	15.80	16.00	16.20
5	D1	13.90	14.00	14.10
6	E	15.80	16.00	16.20
7	E1	13.90	14.00	14.10

S/N	SYM	Millimeters		
		Min	Typ	Max
8	L	0.45	-	0.75
9	L1	1.00		
10	b	0.18	-	0.26
11	e	0.50		

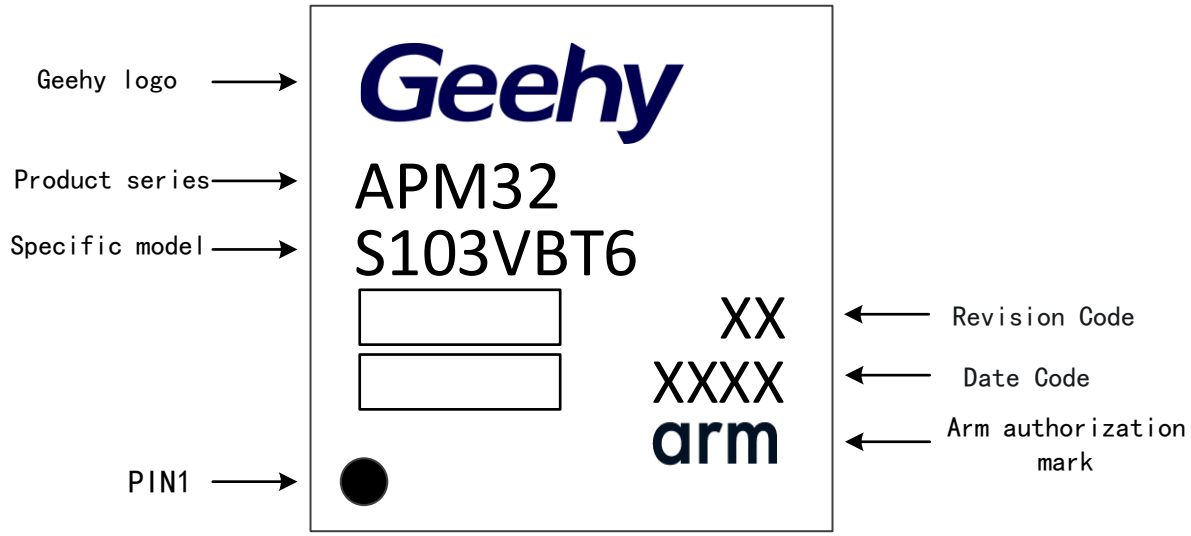
（1） Dimensions are expressed in mm

Figure 18 LQFP100-100 pins, 14×14mm recommended welding Layout



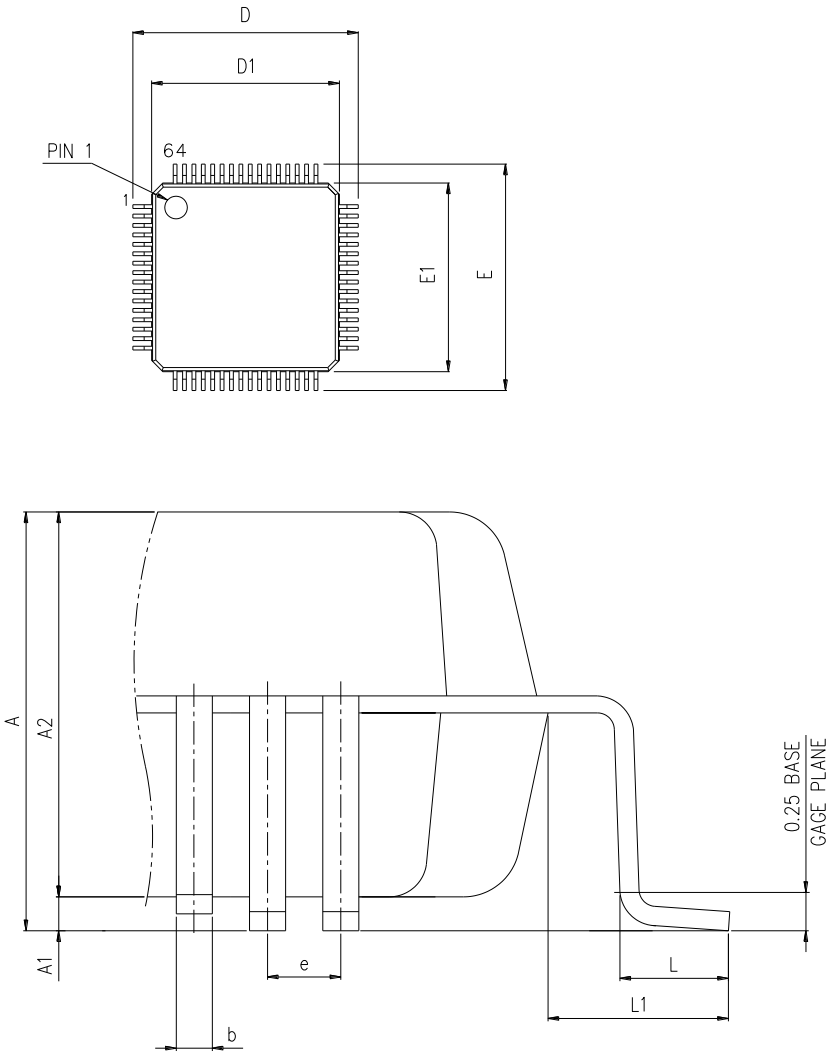
（1） Dimensions are expressed in mm

Figure 19 LQFP100-100 pins, 14×14mm package identification



6.2. LQFP64 Package Diagram

Figure 20 LQFP64 Package Diagram



(1) The figure is not drawn to scale.

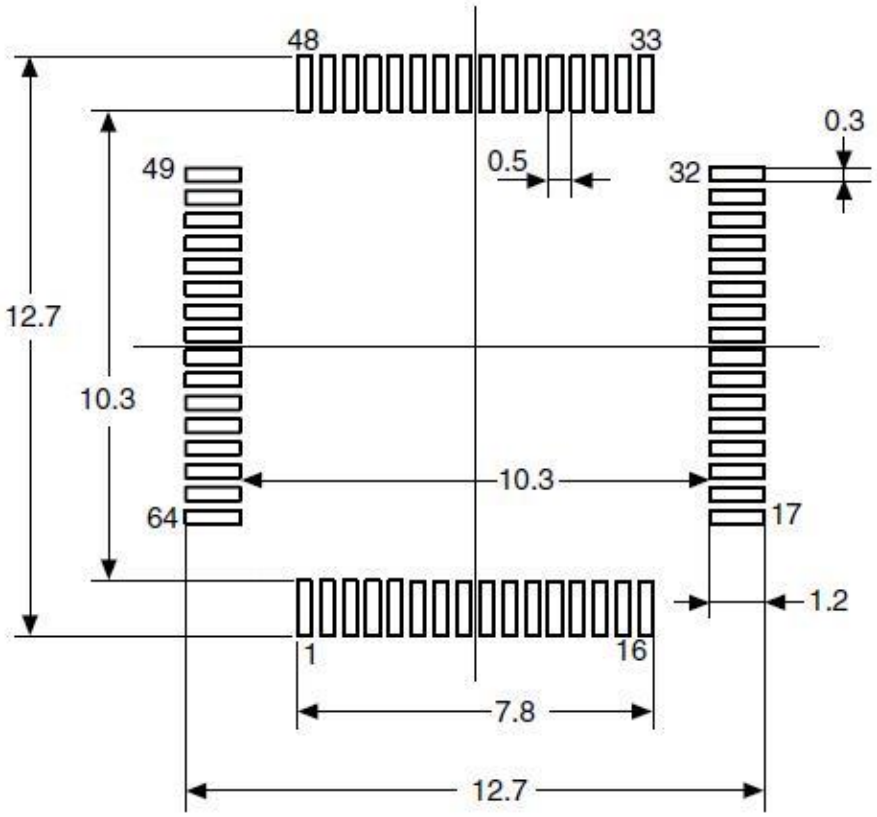
(2) All pins should be soldered to the PCB

Table 44 LQFP64 Package Data

S/N	SYM	Millimeters		
		Min	Typ	Max
1	A	-	-	1.60
2	A1	0.05	-	0.15
3	A2	1.35	1.40	1.45
4	D	11.80	12.00	12.20
5	D1	9.90	10.00	10.10
6	E	11.80	12.00	12.20
7	E1	9.90	10.00	10.10
8	L	0.45	-	0.75
9	L1	1.00		
10	b	0.18	-	0.26
11	e	0.50		

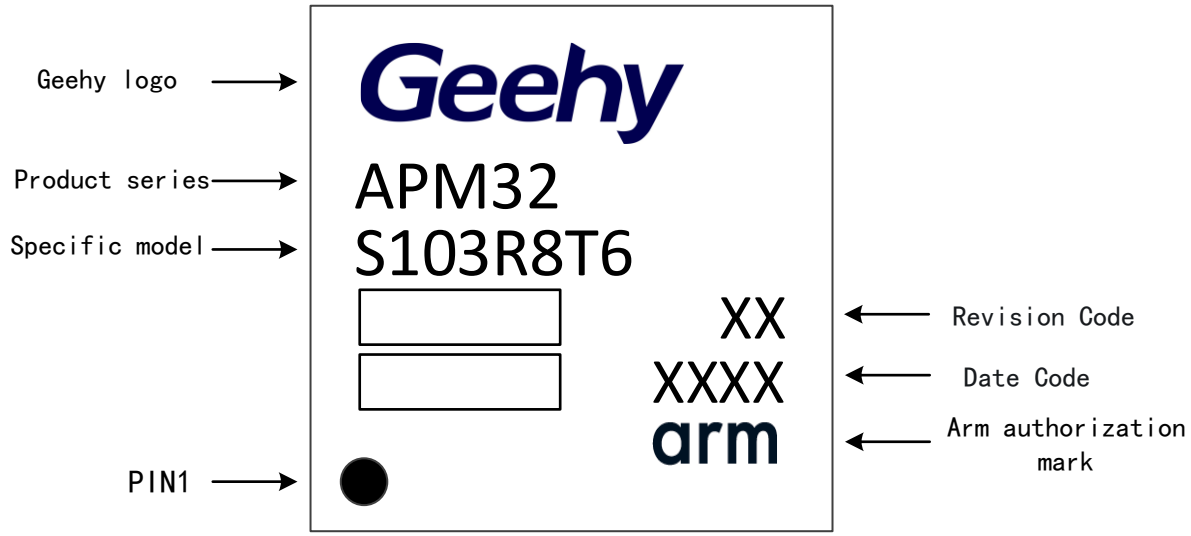
（1） Dimensions are expressed in mm

Figure 21 LQFP64 recommended welding Layout



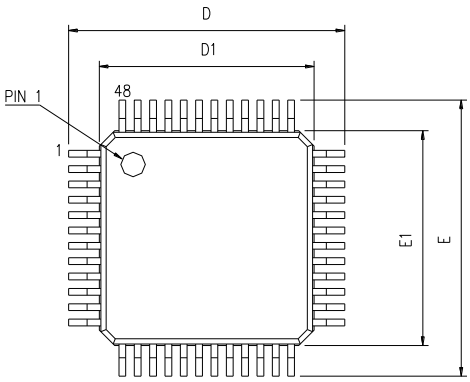
(1) Dimensions are expressed in mm

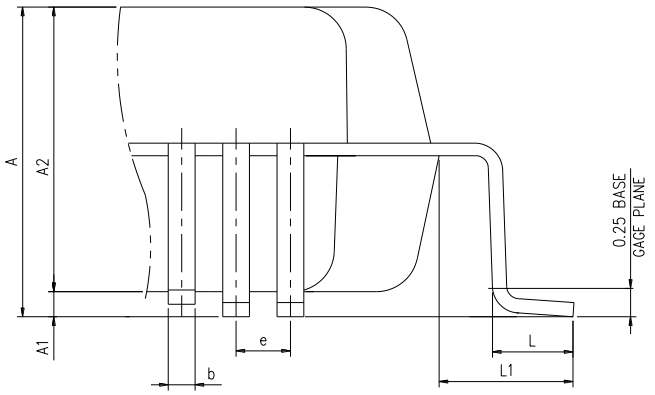
Figure 22 LQFP64 pins identification diagram



6.3. LQFP48 package diagram

Figure 23 LQFP48 Package Diagram





(1) The figure is not drawn to scale.

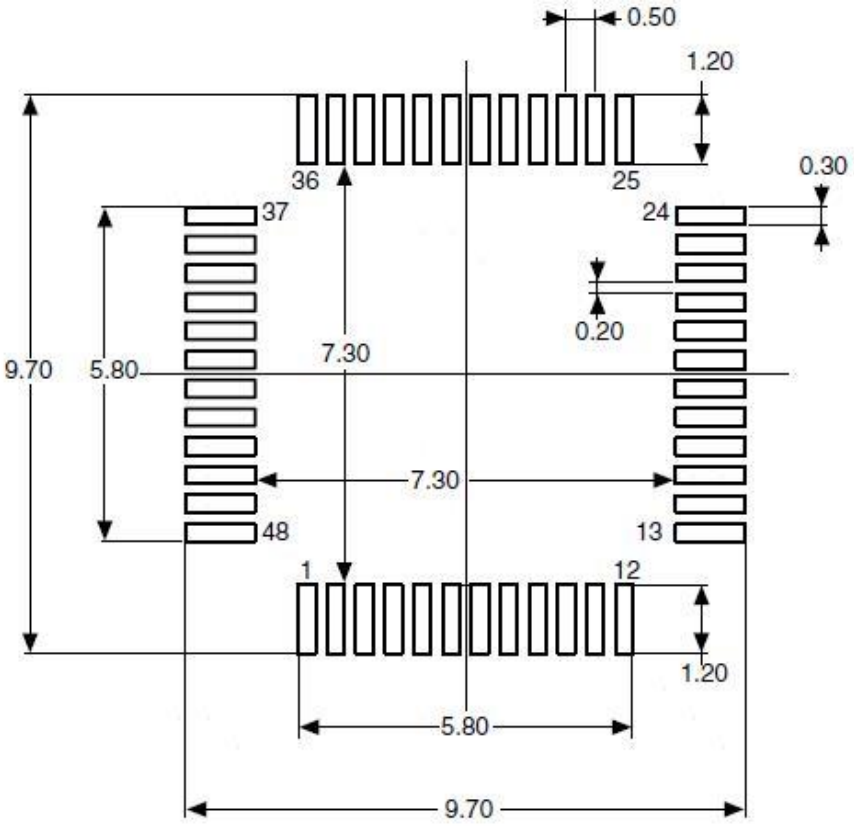
(2) All pins should be soldered to the PCB

Table 45 LQFP48 Package Data

S/N	SYM	Millimeters		
		Min	Typ	Max
1	A	-	-	1.60
2	A1	0.05	-	0.15
3	A2	1.35	1.40	1.45
4	D	8.80	9.00	9.20
5	D1	6.90	7.00	7.10
6	E	8.80	9.00	9.20
7	E1	6.90	7.00	7.10
8	L	0.45	-	0.75
9	L1	1.00		
10	b	0.18	-	0.26
11	e	0.50		

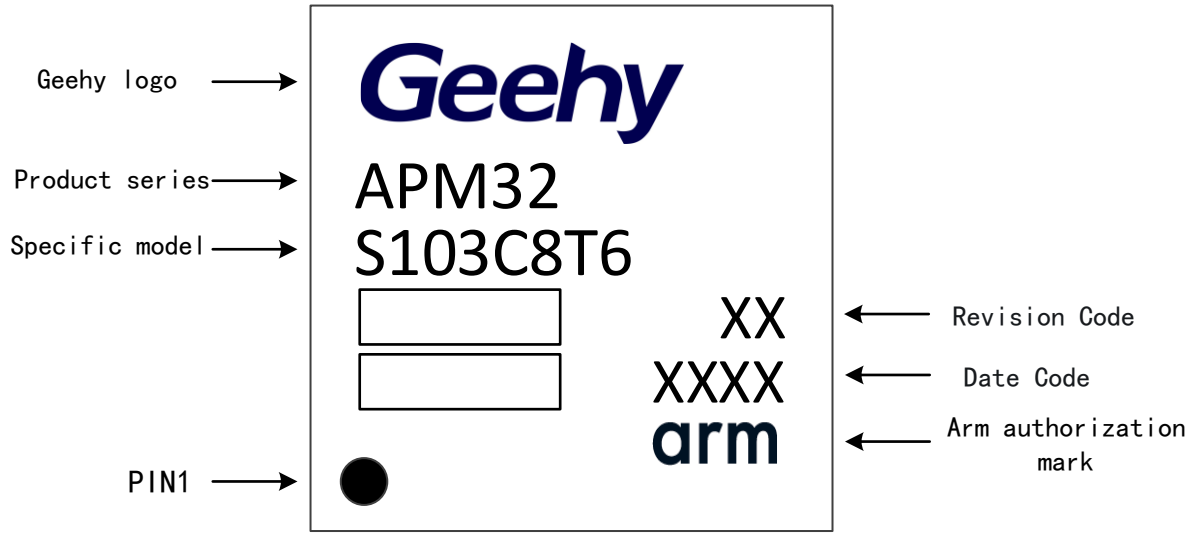
(1) Dimensions are expressed in mm

Figure 24 LQFP48 recommended welding Layout



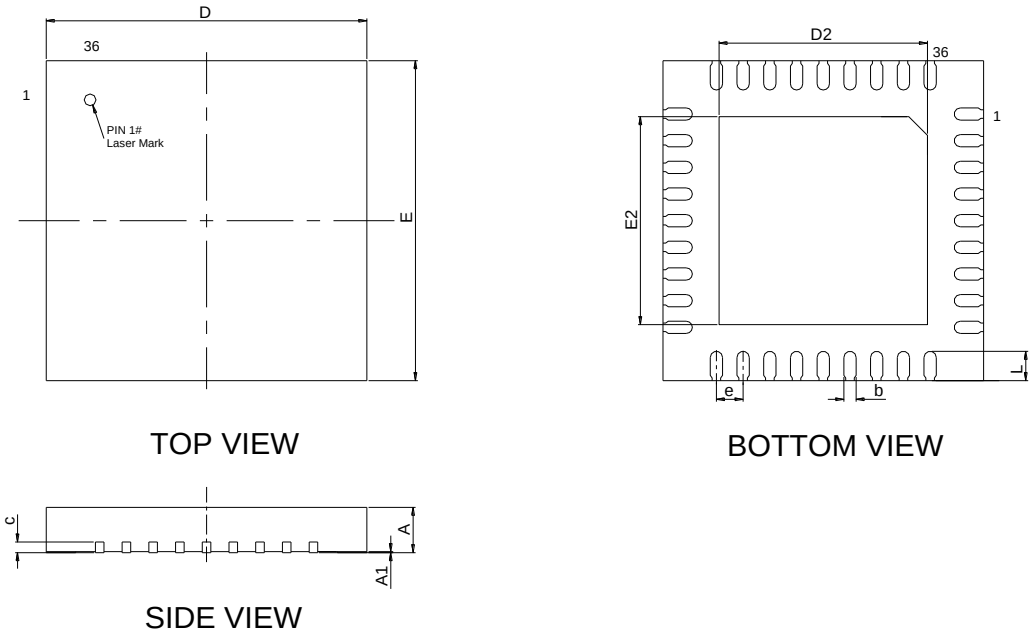
(1) Dimensions are expressed in mm

Figure 25 LQFP64 pins identification diagram



6.4. QFN36 package diagram

Figure 26 QFN36 Package Diagram



(1) Drawing is not to scale.

(2) The inside of the pad on the back is not connected to V_{SS} or V_{DD}.

(3) There is a pad on the bottom of the QFN package that should be soldered to the PCB.

(4) All pins should be soldered to the PCB.

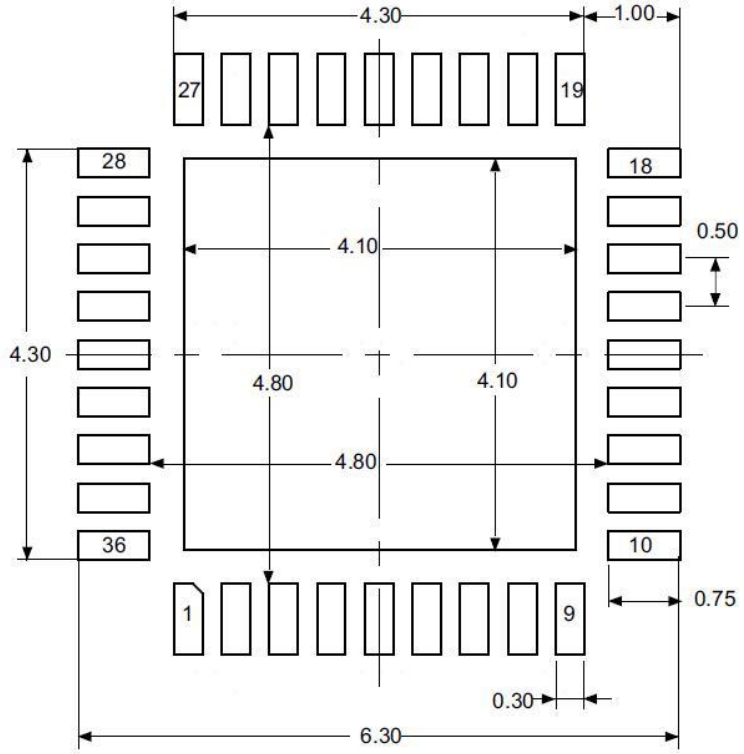
Table 46 QFN36 Package Data

S/N	SYM	Millimeters		
		Min	Typ	Max
1	A	0.80	0.85	0.90

S/N	SYM	Millimeters		
		Min	Typ	Max
2	A1	0.00	0.02	0.05
3	c	0.18	0.20	0.23
4	D	5.90	6.00	6.10
5	D2	3.80	3.90	4.00
6	E	5.90	6.00	6.10
7	E2	3.80	3.90	4.00
8	L	0.50	0.55	0.60
9	b	0.18	0.23	0.30
10	e	0.50		

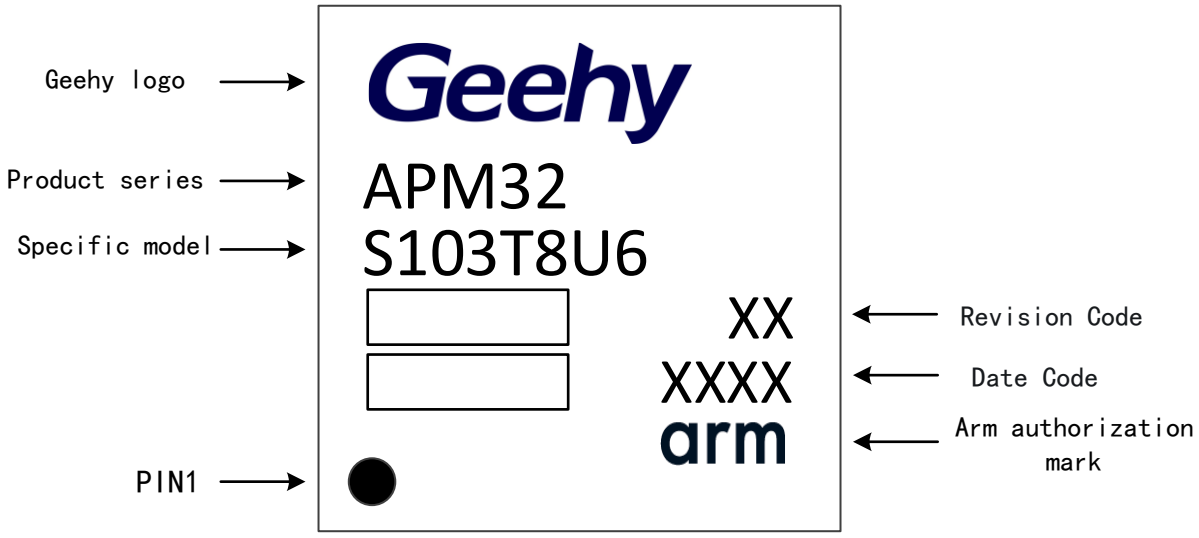
（1） Dimensions are expressed in mm

Figure 27 QFN36 pin Welding Layout Proposal



（1） Dimensions in millimeters。

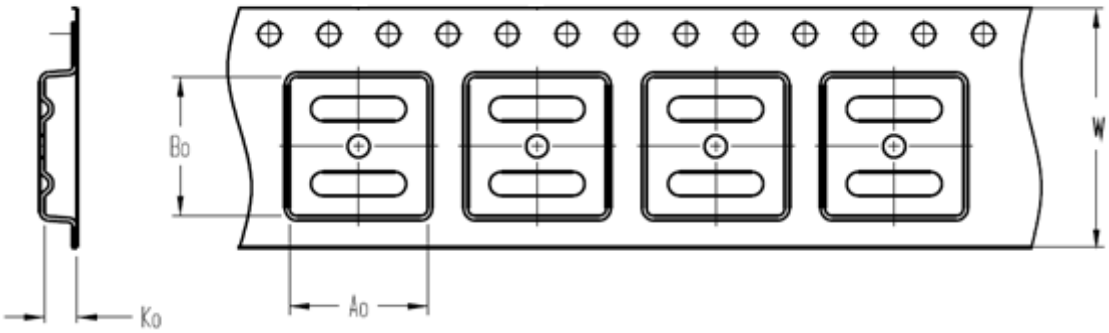
Figure 28 QFN36 pins package identification



7. Packaging information

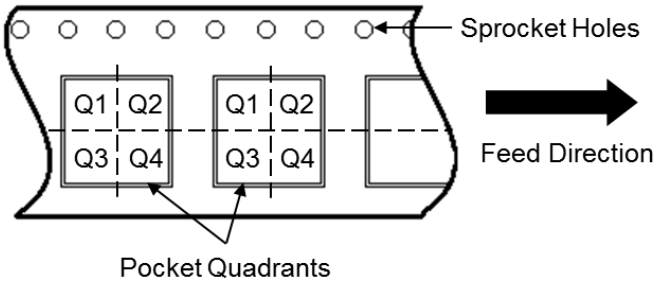
7.1. Reel packaging

Figure 29 Specification Drawing of Reel Packaging

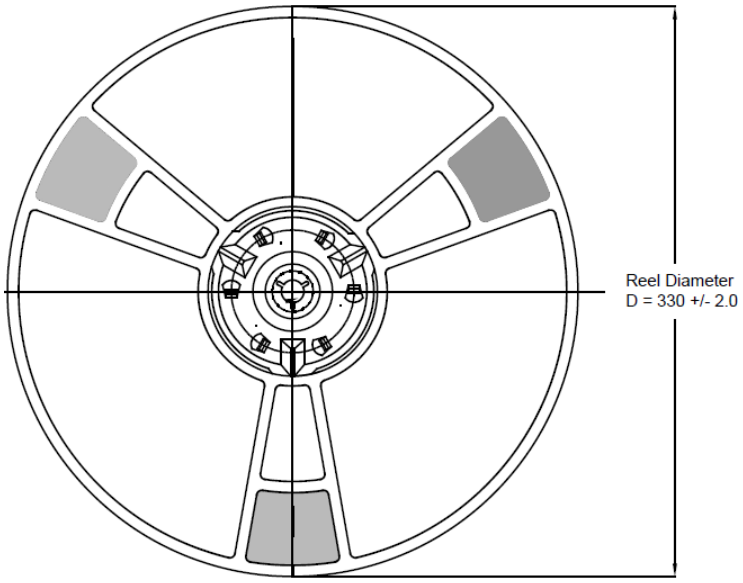


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



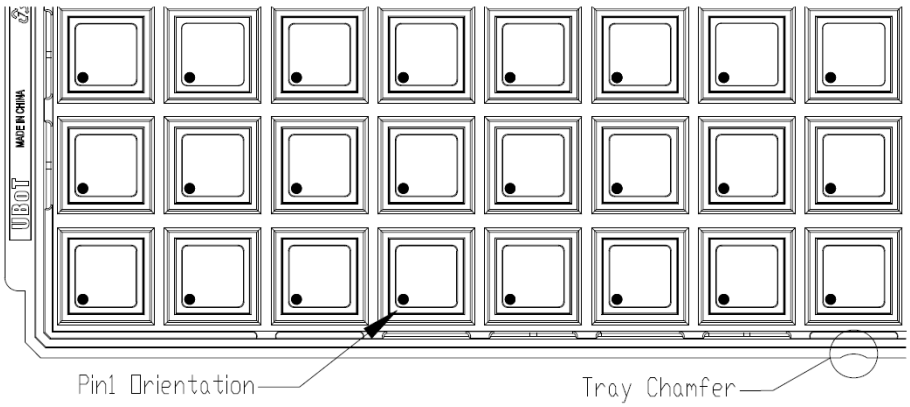
All photos are for reference only, and the appearance is subject to the product.

Table 47 Reel Packaging Parameter Specification Table

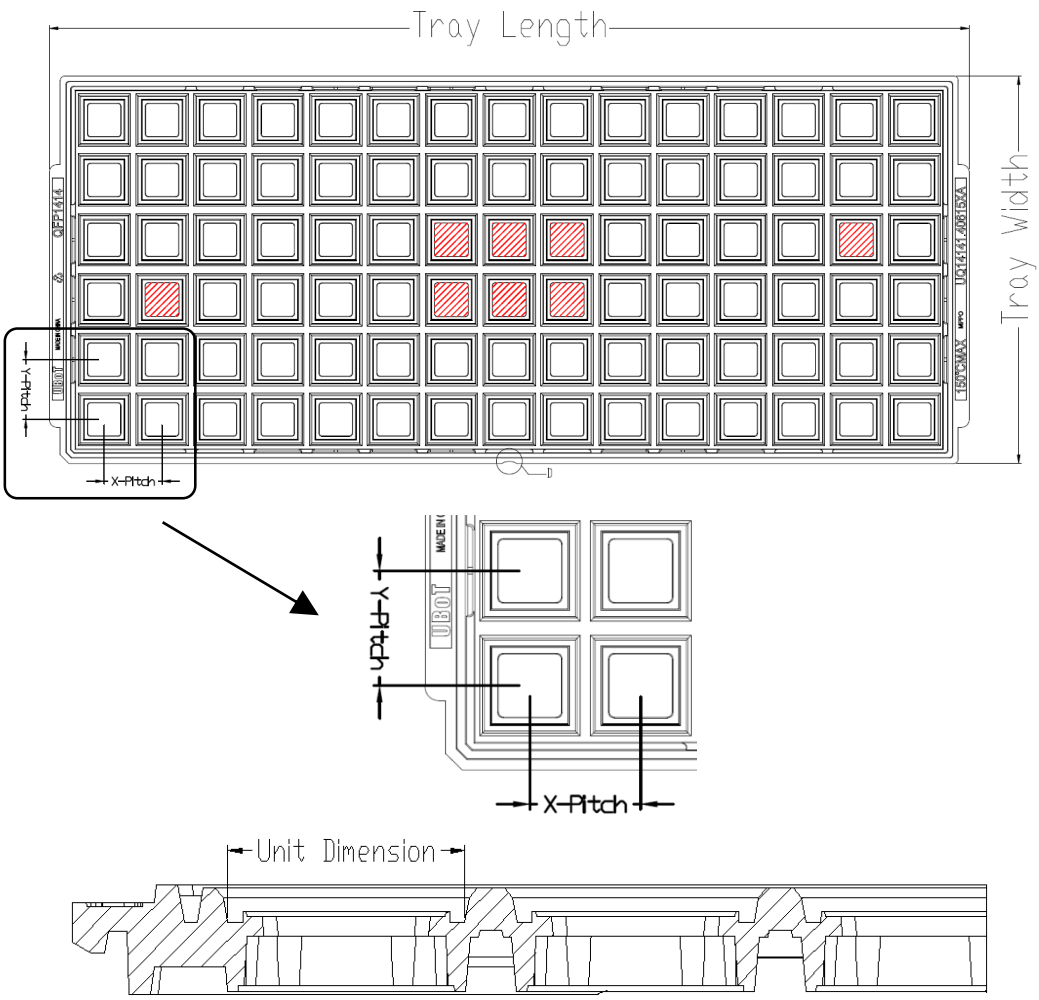
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32S103TBU6	QFN	36	2500	330	6.4	6.4	2.2	16	Q1
APM32S103C8T6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32S103CBT6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32S103RBT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1

7.2. Tray packaging

Figure 30 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table 48 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32S103TBU6	QFN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32S103C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32S103CBT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32S103RBT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32S103VBT6	LQFP	100	300	16.6	16.6	20.3	21	322.6	135.9

8. Ordering information

Figure 31 Product Naming Rules

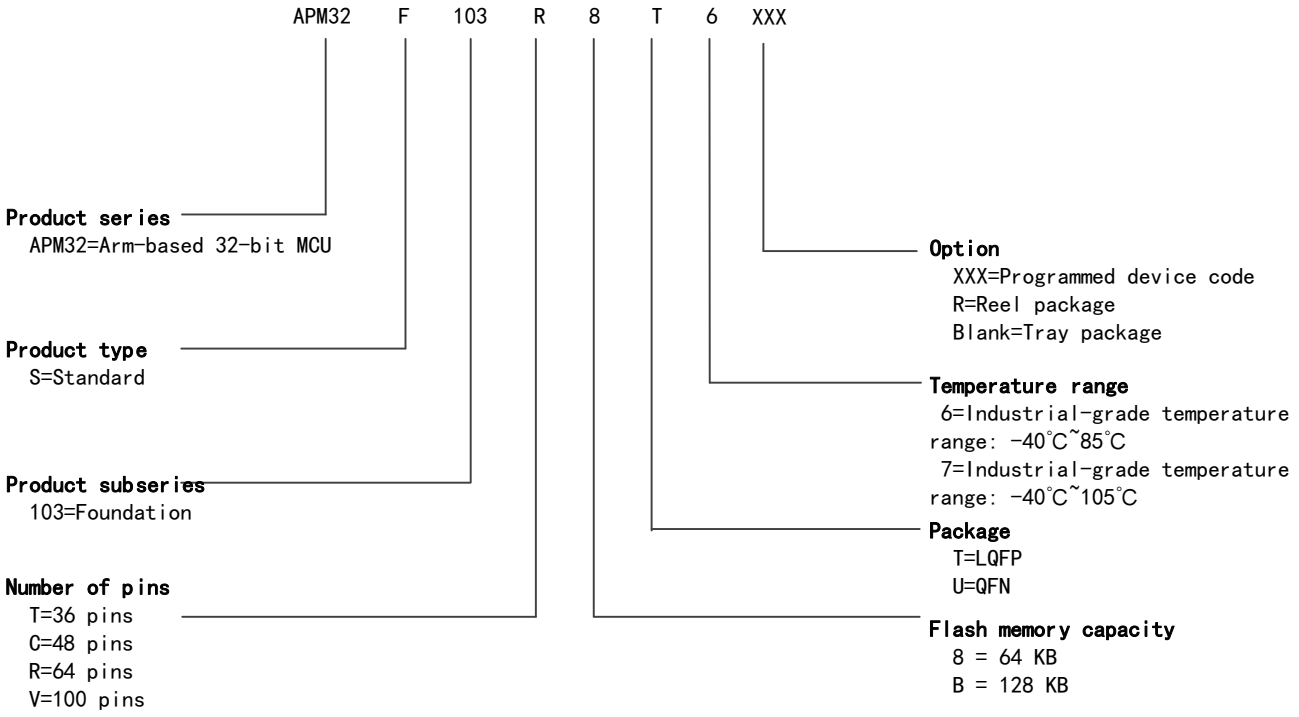


Table 49 Ordering Information Table

订货编码	FLASH（KB）	SRAM（KB）	封装	SPQ	温度范围
APM32S103TBU6	128	36	QFN36	4900	工业级 -40℃~85℃
APM32S103C8T6	64	36	LQFP48	2500	工业级 -40℃~85℃
APM32S103CBT6	128	36	LQFP48	2500	工业级 -40℃~85℃
APM32S103RBT6	128	36	LQFP64	1600	工业级 -40℃~85℃
APM32S103VBT6	128	36	LQFP100	900	工业级 -40℃~85℃
APM32S103TBU6-R	128	36	QFN36	2500	工业级 -40℃~85℃
APM32S103C8T6-R	64	36	LQFP48	2000	工业级 -40℃~85℃
APM32S103CBT6-R	128	36	LQFP48	2000	工业级 -40℃~85℃
APM32S103RBT6-R	128	36	LQFP64	1000	工业级 -40℃~85℃

9. Commonly used function module denomination

Table 1 Commonly Used Function Module Denomination

Chinese description	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
Genera-purpose IO	GPIO
Multiplexing IO	AFIO
Wake up controller	WUPT
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10. Version history

Table 2 Document Version History

Date	Version	Change History
July, 2022	1.0	New
July, 2022	1.1	(1) Correct "CAN_RX" and "CAN_TX" in pin information to "CAN1_RX" and "CAN1_TX"
November, 2022	1.2	(1) Modify pin definition PD10 default multiplexing function QSPI_ CMU is QSPI_ CLK (2) Modify the ESD table (3) Modify product information table
December 28, 2022	1.3	(1) Modify the USBD name in the system block diagram, address map, and pin definition (2) Modify address mapping

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.

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