

Vcc

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Data sheet acquired from Harris Semiconductor SCHS069D – Revised November 2004

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9208-39308

**TERMINAL ASSIGNMENT** 

VDD

FOUT

SELECT

**EOUT** 

FIN

EIN

# CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

High-Voltage Types (20-Volt Rating)
Features:
Independence of power-supply sequence
considerations-Vo. can exceed Vol.

- Independence of power-supply sequence considerations-V<sub>CC</sub> can exceed V<sub>DD</sub>; input signals can exceed both V<sub>CC</sub> and V<sub>DD</sub>
- Up and down level-shifting capability
- Shiftable input threshold for either CMOS or TTL compatibility
- Standardized symmetrical output characteristics
- 100% tested for quiescent current @ 20 V

CD4504B Types

- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25° C
- 5 V, 10 V, and 15 V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

CD4504B hex voltage level-shifter consists of six circuits which shift input signals from the  $V_{\rm CC}$  logic level to the  $V_{\rm DD}$  logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the  $V_{\rm CC}$  HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

The CD4504B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and MT suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

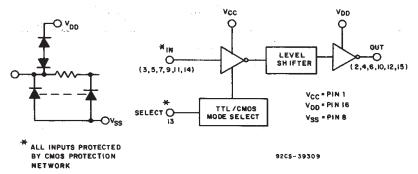


Fig. 1 - Functional diagram for CD4504B.

MAXIMUM RATINGS, Absolute-Maximum Values:	
DC SUPPLY-VOLTAGE RANGE, (VDD)	
Voltages referenced to VSS Terminal)	0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	0.5V to V <sub>CC</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (PD):	
For T <sub>A</sub> = -55°C to +100°C	
For T <sub>A</sub> = +100°C to +125°C"	Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR -	
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types	s)100mW
OPERATING-TEMPERATURE RANGE (TA)	55°C to +125°C
STORAGE TEMPERATURE RANGE (Tato)	85°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max	+265°C

# STATIC ELECTRICAL CHARACTERISTICS

			CONDI	TIONS			LIMITS A	AT INDICA	TED TEN	IPERATU	RES (°C)		
		ν <sub>O</sub>	VIN	Vcc	V <sub>DD</sub>						+25		1
CHARACTERISTIC		(V)	(V)	(V)	(V)	-55	-40	+85	+125	MIN	TYP	MAX	UNITS
Quiescent D		_	0, 5	5	5	1.5	1.5	1.5	1.5	_	0.02	1.5	
Current, IDD Max and ICC in CMOS-CMOS Mode			0,10	5	10	2	2	2	2		0.02	2	mA
			0, 15	5	-15	4	4	120	120	<u> </u>	0.02	4	μА
	<u> </u>	<u> </u>	0,20	5	20	20	20	600	600	_	0.04	20	1
	evice Current,		0,5	5	5	5	5	6	6	_	2.5	5	
ICC Max T	TL-CMOS Mode		0, 10	5	10	5	5	6	6	_	2.5	5	mA
		_	0,15	5	15	5	5	6	6	_	2.5	5	1
Output Low		0.4	0.5	_	5	0.64	0.61	0.42	0.36	0.51	1	_	
Current, IO	L Min	0.5	0,10	_	10	1.6	1.5	1.1	0.9	1.3	2.6	_	1
		1.5	0, 15		15	4.2	4	2.8	2.4	3.4	6.8	_	1 .
Output High		4.6	0,5	-	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	_	l mA
Current, IO	H Min	2.5	0,5	_	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	_	1
		9.5	0, 10	_	10	-1.6	-1.5	-1,1	-0.9	-1.3	-2.6	_	
		13.5	0,15	_	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8		
Output Voltage:		<b> </b>	0,5		5		0.	05		_	0	0.05	†
Low-Level,	V <sub>OL</sub> Max	_	0,10	_	10		0.0	05		-	0	0.05	
		_	0,15	_	15		0.	05			0	0.05	
Output Volta	ge:	-	0,5		5	4.95				4.95	5	_	f
High-Level		_	0,10		10	9.95				9.95	10		
		_	0, 15	_	15		14	95		14.95	15		1
Input Low	TTL-CMOS	1	_	5	10		0.	.8		_	_	0.8	1
Voltage,	TTL-CMOS	1	_	5	15		0.			_		0.8	v
V <sub>IL</sub> Max Note 1	CMOS-CMOS	1		5	10		1.	.5				1.5	
	CMOS-CMOS	1.5	_	5	15		1.					1,5	
	CMOS-CMOS	1.5	_	10	15							3	1
Input High	TTL-CMOS	9	_	5	10					2		<u> </u>	1
Voltage,	TTL-CMOS	13.5	_	5	15	,				2		<del></del>	1
V <sub>IH</sub> Min Note 1	CMOS-CMOS	9		5	10		3.			3.5			1
11010 1	CMOS-CMOS	13.5		5	15		3.	<del></del>		3.5			1
	CMOS-CMOS	13.5		10	15		7			7			1
Input Current	1		0,18	<del>-</del>	18	±0.1	±0.1	±1	±1		±10 <sup>-5</sup>	±0.1	μА

Note 1: Applies to the 6 input signals. For mode control (P13), only the CMOS-CMOS ratings apply.

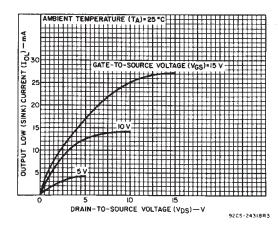


Fig. 2 - Typical output low (sink) current characteristics.

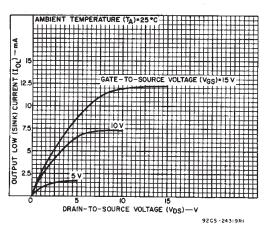
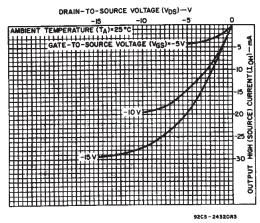


Fig. 3 - Minimum output low (sink) current characteristics.

#### CD4504B Types



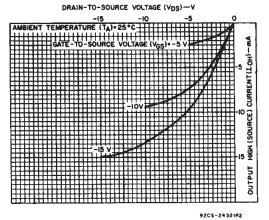


Fig. 4 - Typical output high (source) current characteristics.

Fig. 5 - Minimum output high (source) current characteristics.

#### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD	LIM	ITS	UNITS
OHARACIERISTIC	(V)	Min.	Max.	ONITS
Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range)	_	5	18	٧

### DYNAMIC ELECTRICAL CHARACTERISTICS, At TA = 25°C; Input tr,tf = 20 ns, CL = 50 pF, RL = 200 Ω

CHARACTERISTIC		SHIFTING MODE	VCC (V)	VDD (V)	LIMITS		UNITS
OTIANACT ENIST		SHIFTING MODE	VCC (V)VDD (V		TYP.	MAX.	UNITS
		TTL to CMOS	5	10	140	280	
		V <sub>DD</sub> > V <sub>CC</sub>	5	15	140	280	
Propagation Delay:	ſ	CMOS to CMOS	5	10	120	240	]
High-to Low,	t <sub>PHL</sub>	$V_{DD} > V_{CC}$	5	15	120	240	
		. *	10	15	70	140	
	ſ	CMOS to CMOS	10	5	275	550	
		$V_{CC} > V_{DD}$	15	5	275	550	
			15	10	70	140	
		TTL to CMOS	5	10	140	280	ns
	1	V <sub>DD</sub> > V <sub>CC</sub>	5	15	140	280	
	[	CMOS to CMOS	5	10	120	240	7
Low-to-High,	telH	$V_{DD} > V_{CC}$	5	15	120	240	
	21		10	15	70	140	
		CMOS to CMOS	10	5	200	400	
		Vcc > Vpp	15	5	200	400	
	A + " " "		15	10	60	120	
	1		1	5	100	200	
Transition Time,	t <sub>THL</sub> ,t <sub>TLH</sub>	All Modes		10	50	100	
				15	40	80	
Input Capacitance,	Cin	Any Input			5	7.5	pF

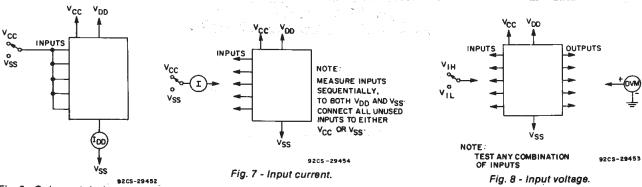


Fig. 6 - Quiescent device current.

# CD4504B Types

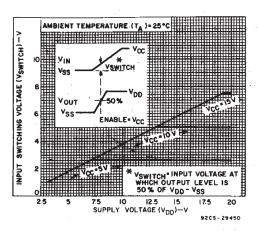


Fig. 9 - Typical input switching as a function of high-level supply voltage.
(SELECT at Vcc-CMOS mode).

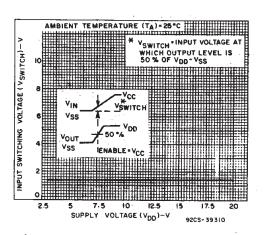


Fig. 10 - Typical input switching as a function of high-level supply voltage (SELECT at Vss-TTL mode).

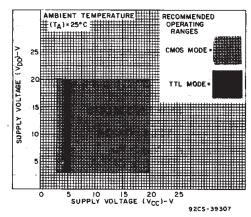
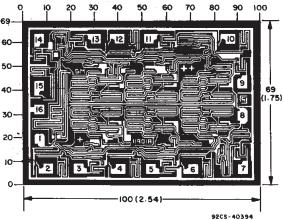


Fig. 11 - High-level supply voltage vs. low-level supply voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and pad layout for CD4504BH.



30-Jan-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD4504BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD4504BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD4504BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD4504BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

# PACKAGE OPTION ADDENDUM



www.ti.com 30-Jan-2012

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF CD4504B, CD4504B-MIL:

Catalog: CD4504B

● Enhanced Product: CD4504B-EP, CD4504B-EP

Military: CD4504B-MIL

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications



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• Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

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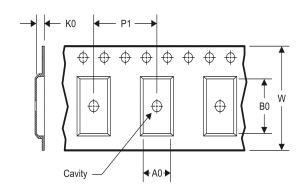
# TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**





#### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4504BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4504BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**PACKAGE MATERIALS INFORMATION** 

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4504BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4504BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

# 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDS0-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

# PLASTIC SMALL OUTLINE

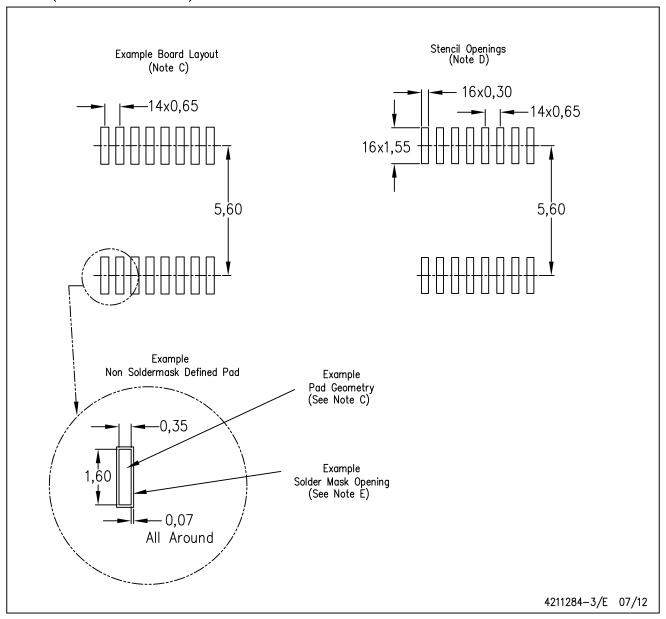


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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