Antenna

YSOS001AA Datasheet

Antenna Services

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About the Document

Revision History

Version	Date	Author	Note
-	2021-12-16	Rison LI	Creation of the document
1.0	2021-12-16	Rison LI	First official release
1.1	2022-03-10	Rison LI	Updated the antenna picture (Chapter 2).

Contents

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1 Product Description

The YSOS001AA is a Single Pole Quad Throw (SP4T) RF antenna aperture switch optimized for low C OFF enabling applications up to 6.0 GHz. This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. Unlike GaAs technology, the 0.1dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

2 Product Features

- Designed for high linearity and high RF voltage tuning applications
- Multiple selectable switch configurations:
  Each throw directly and independently controlled
- Low RON resistance of 1.6 ohm at each port in ON state
- Low COFF capacitance of 120 fF at each port in OFF state
- High bidirectional RF operating voltage of 36 V in OFF state
- Low harmonic generation
- 2 GPIO pins control interface
- Supply voltage range: 1.65–3.6 V
- No RF parameter change within supply voltage range
- Small form factor 1.1 mm x 1.5 mm (MSL1, 260°C per JEDEC J-STD-020)
- RoHS and WEEE compliant package

3 Product Specifications

Maximum Ratings (T_A = 25 °C, unless otherwise specified)		
Frequency Range	≥ 0.1 GHz	1)
Supply Voltage 2)	-0.5 V to 3.6 V	Only for infrequent and short duration time periods
Storage Temperature Range	-55 °C to 150 °C	
RF Input Power	≤ 39 dBm	Pulsed RF input power, duty cycle of 25 % with T period = 4620 µs, ON-state, setup as of Fig. 1.
RF Voltage	≤ 48 V	Short term peaks (1 µs, duty cycle 0.1%), isolation mode, test setup acc. Fig. 2/Fig. 3 and exceeding typical linearity, *RON* and *COFF* parameters.
ESD Capability, CDM 3)	-1.5 kV to 1.5 kV	-
ESD Capability, HBM 4)	-1 kV to 1 kV	-
ESD Capability, System Level (RF Port) 5)	-8 kV to 8 kV	RF vs system GND, with 27 nH shunt inductor
Junction Temperature	≤ 125 °C	-
Thermal Resistance Junction - Soldering Point	≤ 45 K/W	-
Maximum DC-voltage on RF-Ports and RF-Ground	0 V	No DC voltages allowed on RF-Ports
Control Voltage Levels	-0.7 - VDD + 0.7 (Max. 3.6) V	-
Moisture Sensitivity Level	1	-

1) Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports (*VRFDC)* has to be 0 V.

2) Note: Consider potential ripple voltages on top of *VIO*.
Including RF ripple, *VIO* must not exceed the Max. ratings: *VCtrl* = *VDC* + *VRipple*.

3) Field Induced Charged Device Model (CMD) ANSI/ESDA/JEDEC JS-002. The CDM Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

4) Human Body Model ANSI/ESDA/JEDEC JS-001 (*R* = 1.5 kΩ, *C* = 100 pF).

5) IEC 61000-4-2 (*R* = 330 Ω, *C* = 150 pF), Contact Discharge.

Warning: Stresses above the Max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

DC Characteristics (T_A = -40 °C to 85 °C)		
Supply Voltage	1.65 V Min. 2.8 V Typ. 3.6V Max.	-
Supply Current	80 uA Typ. 150 uA Max.	-
Control Voltage Low	0–0.45 V	-
Control Voltage High	1.2 V Min. 1.8 V Typ. 2.85 V Max.	$V_{ctrl,high} < V_{DD}$
Control Current Low	-1 uA Typ. 0 uA Typ. 1 uA Max.	-
Control Current High	-1 uA Typ. 0 uA Typ. 1 uA Max.	$V_{ctrl,high} < V_{DD}$
Ambient Temperature	-40 °C Min. 25 °C Typ. 85 °C Max.	*PIN = 0 dBm, Z0 = 50 Ω* *TA = −40 °C to + 85 °C* *VDD = 1.65–3.6 V* *Refer to Fig. 4 and Fig. 5.*
RF Switching Time	2 us Typ. 5 us Typ. 7 us Max.	
Startup Time	20 us Typ. 30 us Max.	-
RF Small Signal Parameter		
Frequency Range	0.1–6 GHz	-
Switch ON Resistance	1.6 Ω Typ.	RFx to RFC
Switch OFF Capacitance	120 fF Typ.	RFx to GND; Extracted Value for 2 GHz
Parasitic RF Shunt Capacitance	42 fF Typ.	-
Switch Series Inductance	0.1 nH Typ.	-
Insertion Loss[1), 2)] 600–960 MHz	0.15 dB Min. 0.22 dB Typ.	

	0.36 dB Max.	*VDD* = 1.65–3.6 *V* *Z*0 = *50 Ω* *TA* = *−40 ˚C* to + *85 °C*
Insertion Loss[1), 2)] 1710–1980 MHz	0.23 dB Min. 0.37 dB Typ. 0.47 dB Max.	
Insertion Loss[1), 2)] 1980–2170 MHz	0.29 dB Min. 0.39 dB Typ. 0.49 dB max	*VDD* = 1.65–3.6 *V* *Z*0 = *50 Ω* *TA* = *−40 ˚C* to + *85 °C*
Insertion Loss[1), 2)] 2170–2690 MHz	0.36 dB Min. 0.46 dB Typ. 0.59 dB Max.	*VDD* = 1.65–3.6 *V* *Z*0 = *50 Ω* *TA* = *−40 ˚C* to + *85 °C*
Return Loss[1), 2)] All Ports @ 600–960 MHz	20 dB Min. 22 dB Typ. 26 dB Max.	*VDD* = 1.65–3.6 *V* *Z*0 = *50 Ω* *TA* = *−40 ˚C* to + *85 °C*
Return Loss[1), 2)] All Ports @ 1710–2690 MHz	17 dB Min. 21 dB Typ. 25 dB Max.	
Isolation RFx to RFC[1), 2)] 600–960 MHz	29 dB Min. 31 dB Typ. 38 dB Max.	*VDD* = 1.65–3.6 *V* *Z*0 = *50 Ω* *TA* = *−40 ˚C* to + *85 °C*
Isolation RFx to RFC[1), 2)] 1710–1980 MHz	21 dB Min. 25 dB Typ. 35 dB Max.	
Isolation RFx to RFC[1), 2)] 1980–2170 MHz	20 dB Min. 23 dB Typ. 35 dB Max.	
Isolation RFx to RFC[1), 2)] 2170–2690 MHz	17 dB Min. 20 dB Typ. 27 dB Max.	

1) Valid for all RF power levels, no compression behavior.

2) On application board without any matching components.

RF Large Signal Parameter		
RF Operating Voltage	≤ 36 V	All Switch throws operated in isolation Mode, except one throw switched ON with open termination. Test condition schematic in Fig.2. All RF parameters in specs including harmonic distortion.
Harmonic Generation (up to 12.75 GHz) [1), 2), 3)] All RF Ports – Second Order Harmonics	105 dBc Typ.	25 dBm, 50 Ω, f_0 = 786 MHz
Harmonic Generation (up to 12.75 GHz) [1), 2), 3)] All RF Ports – Third Order Harmonics	115 dBc Typ.	25 dBm, 50 Ω, f_0 = 786 MHz

Harmonic Generation (up to 12.75 GHz) [1), 2), 3)] All RF Ports - Second Order Harmonics	93 dBc Typ.	33 dBm, 50 Ω, f_0 = 824 MHz
Harmonic Generation (up to 12.75 GHz) [1), 2), 3)] All RF Ports– Third Order Harmonics	94 dBc Typ.	33 dBm, 50 Ω, f_0 = 824 MHz
Harmonic Generation (up to 12.75 GHz) [1), 2), 3)] All RF Ports	≥ 105 dBc	25 dBm, 50 Ω
Intermodulation Distortion IMD2 [1), 2), 3)] IIP2, Low	110 dBm Typ.	IIP2 Conditions Table 1
Intermodulation Distortion IMD2 [1), 2), 3)] IIP2, High	120 dBm Typ.	-
Intermodulation Distortion IMD2 [1), 2), 3)] IIP3	75 dBm Typ.	IIP3 Conditions Table 2
SV LTE Intermodulation [1), 2), 3)] IIP3, SVLTE	75 dBm Typ.	SVLTE Conditions Table 3

1) Terminating Port Impedance: Z0 = 50 Ω.
2) Supply Voltage: VDD = 1.65–3.6 V.
3) On application board without any matching components.

4 Overall Performance

4.1. Test Setup

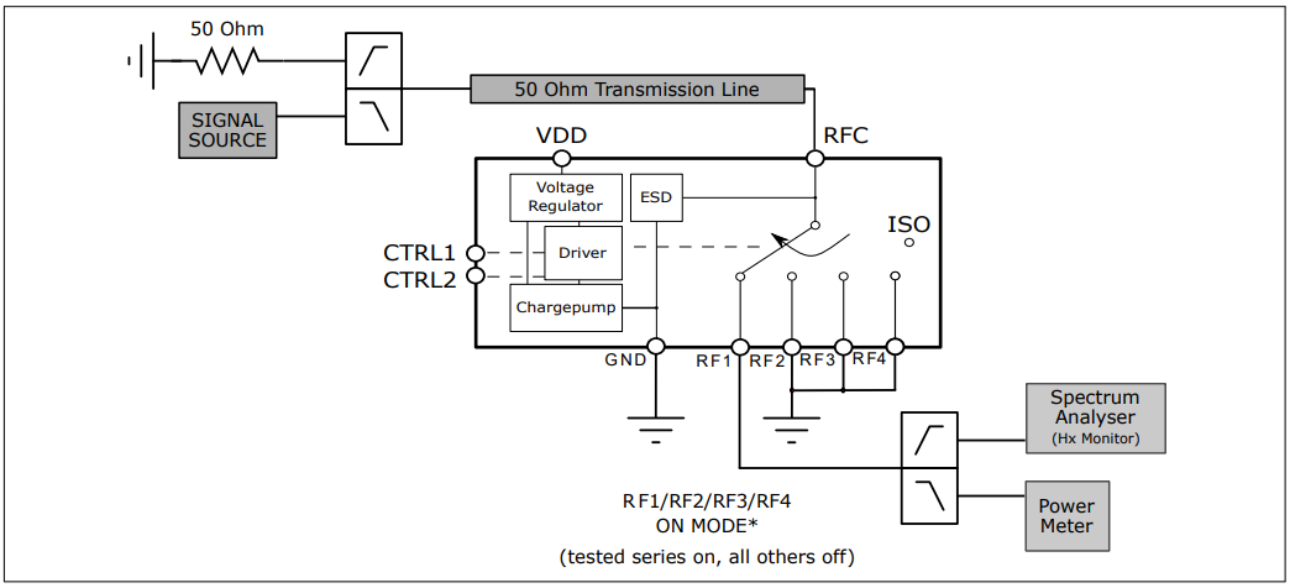

Figure 1: RF Operating and Harmonics Generation Measurement Configuration - RFx ON Mode

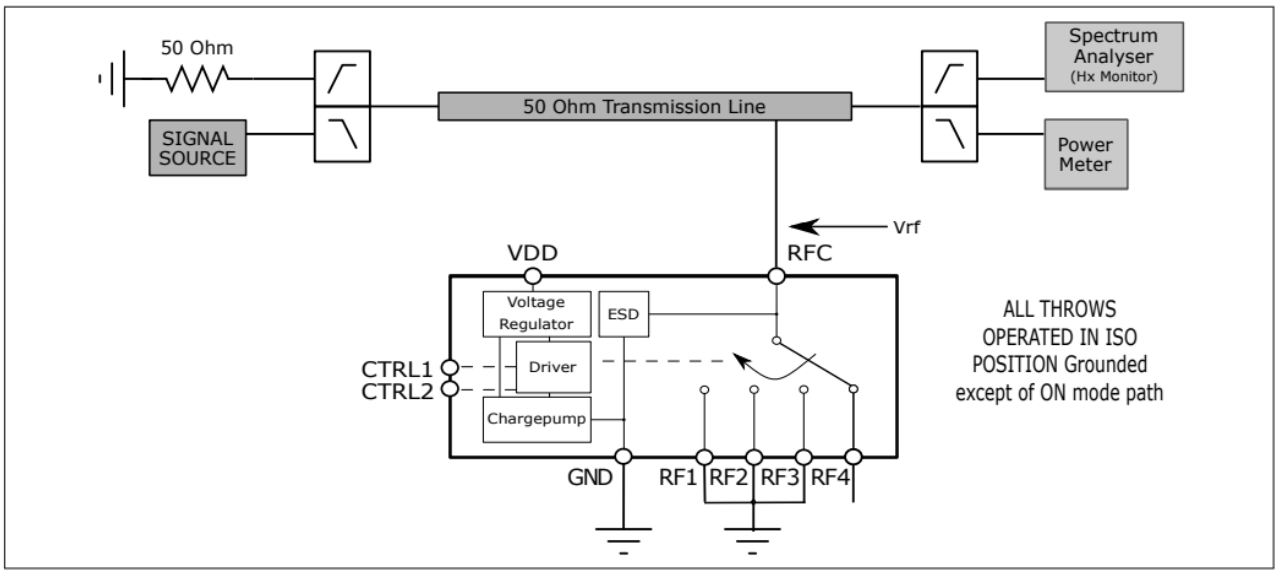

Figure 2: RF Operating Voltage Measurement Configuration - OFF Mode at RFC

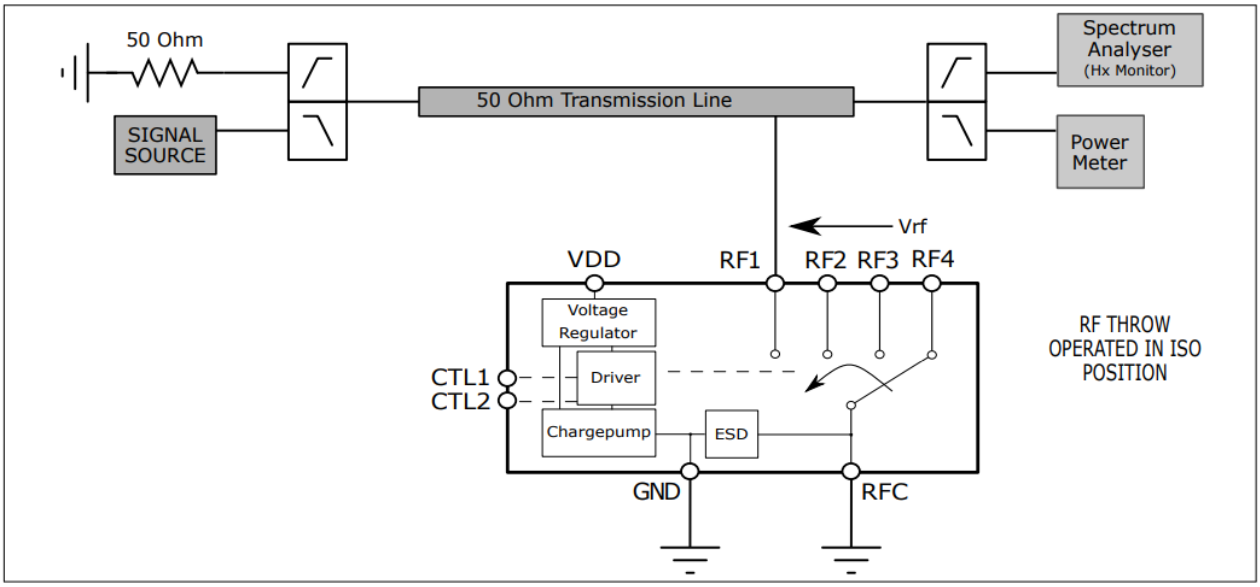

Figure 3: RF Operating Voltage Measurement Configuration - OFF Mode at RFx

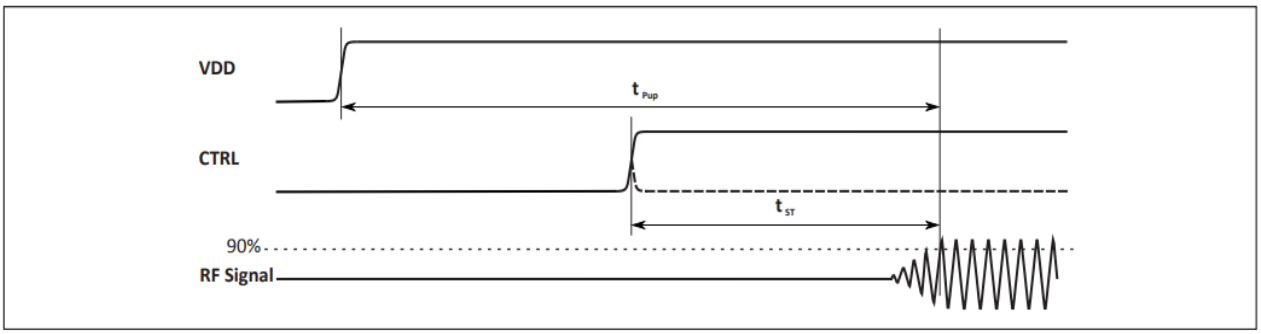

Figure 4: Switching Time Definition

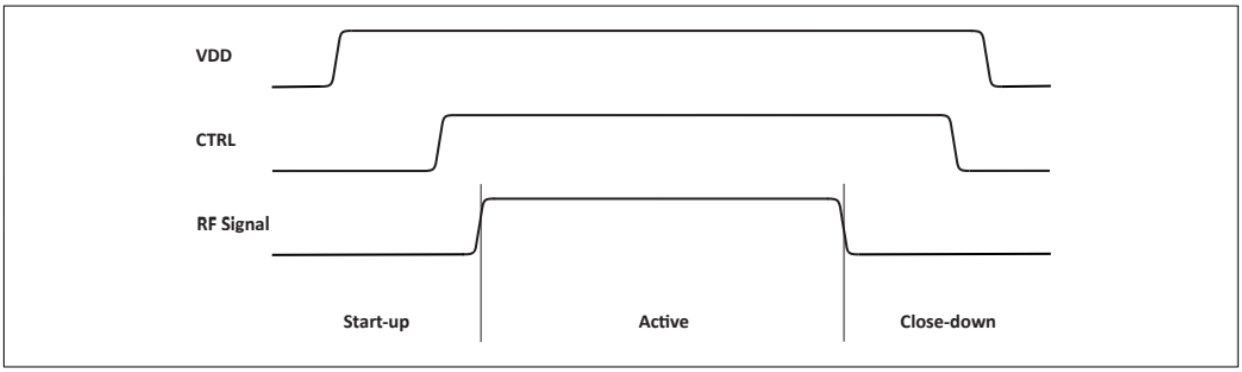

Figure 5: Timing of Control and RF Signals for Valid Operation

Table 1: IIP2 Conditions

Band	In-Band Frequency [MHz]	Blocker Frequency1 [MHz]	Blocker Power1 [dBm]	Blocker Frequency2 [MHz]	Blocker Power2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 2: IIP3 Conditions

Band	In-Band Frequency [MHz]	Blocker Frequency1 [MHz]	Blocker Power1 [dBm]	Blocker Frequency2 [MHz]	Blocker Power2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

Table 3: SVLTE Conditions

Band	In-Band Frequency [MHz]	Blocker Frequency1 [MHz]	Blocker Power1 [dBm]	Blocker Frequency2 [MHz]	Blocker Power2 [dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

4.2. Logic Truth table

Table 4: Modes of Operation

State	Mode	CTRL1	CTRL2
1	RF1 to RFc	0	0
2	RF2 to RFc	0	1
3	RF3 to RFc	1	0
4	RF4 to RFc	1	1

- Mapping of Switch Rows to Bit: ON = 1, OFF = 0.

4.3. Application Information

- Pin Configuration and Function

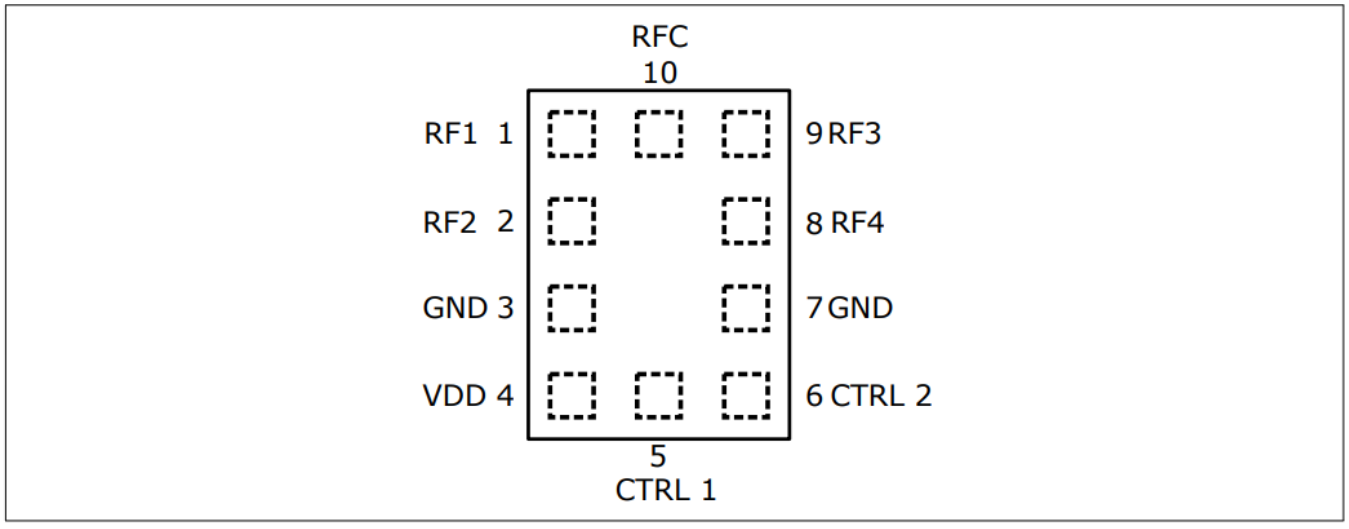

Figure 6: YSOS001AA Pin Configuration (Top View)

Table 5: Pin Configuration and Function

Pin No.	Name	Function
1	RF1	RF1 Port
2	RF2	RF2 Port
3	GND	Ground
4	VDD	Power Supply
5	CTRL1	GPIO Digital Control Line
6	CTRL2	GPIO Digital Control Line
7	GND	Ground
8	RF4	RF4 Port
9	RF3	RF3 Port
10	RFC	Common RF

5 Product Size

Table 6: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	X	1.1 ±0.05	mm
Y-Dimension	Y	1.5 ±0.05	mm
Size	Size	2.25	mm^2
Height	H	0.375 + 0.025/ 0.375 − 0.015	mm

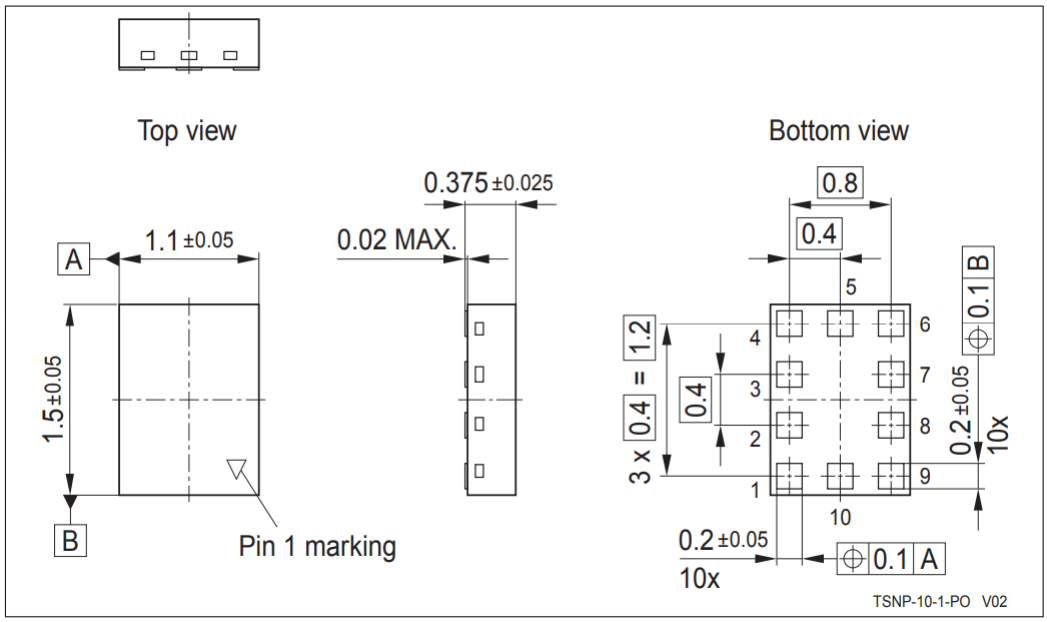

Figure 7: TSNP-10-1 Package Outline (Top, Side and Bottom Views)

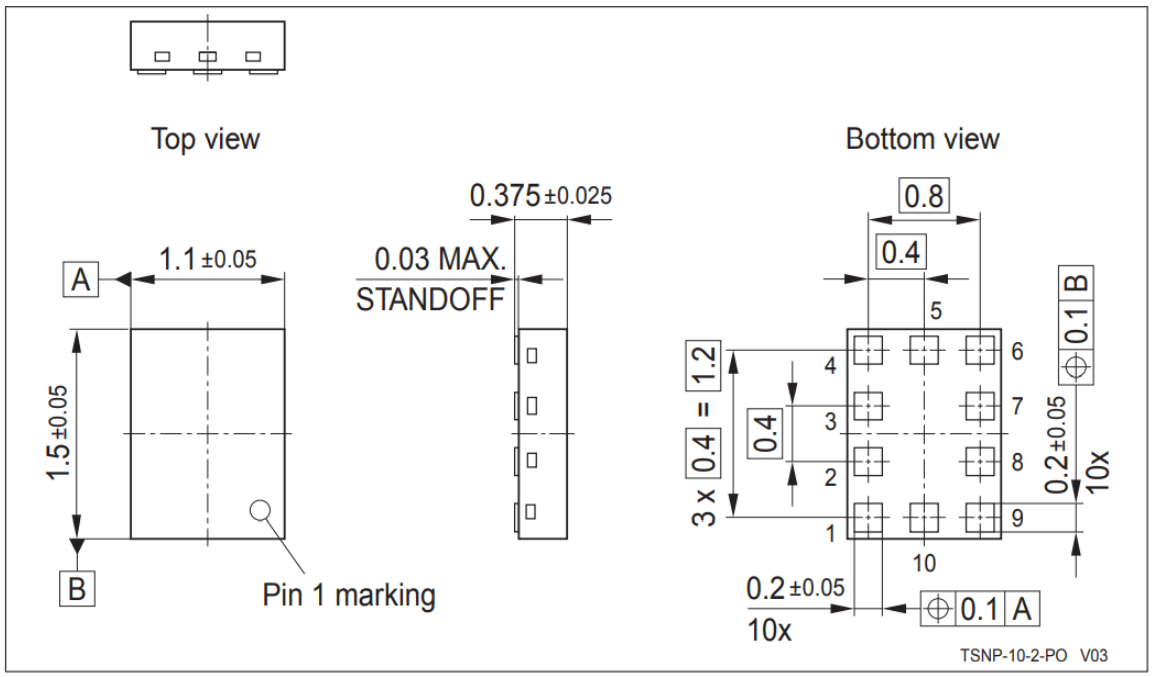

Figure 8: TSNP-10-2 Package Outline (Top, Side and Bottom Views)

Table 7: Year Data Code Marking – Digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 8: Week Date Code Marking - Digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t	-	-
11	L	22	Z	33	g	44	u	-	-

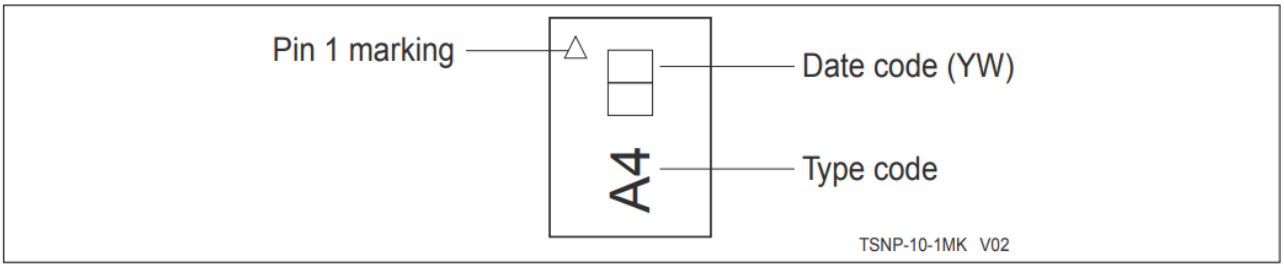

Figure 9: TSNP10-1 Marking Specification (Top View): Data Code Digits Y and W (Defined in Table 11/12)

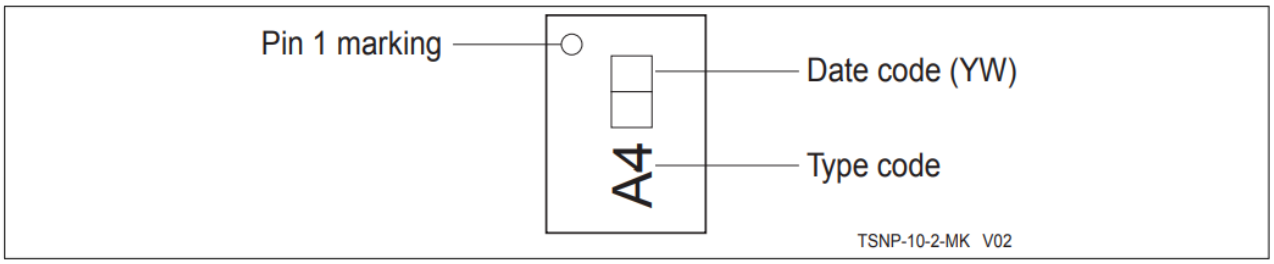

Figure 10: TSNP10-2 Marking Specification (Top View): Data Code Digits Y and W (Defined in Table 11/12)

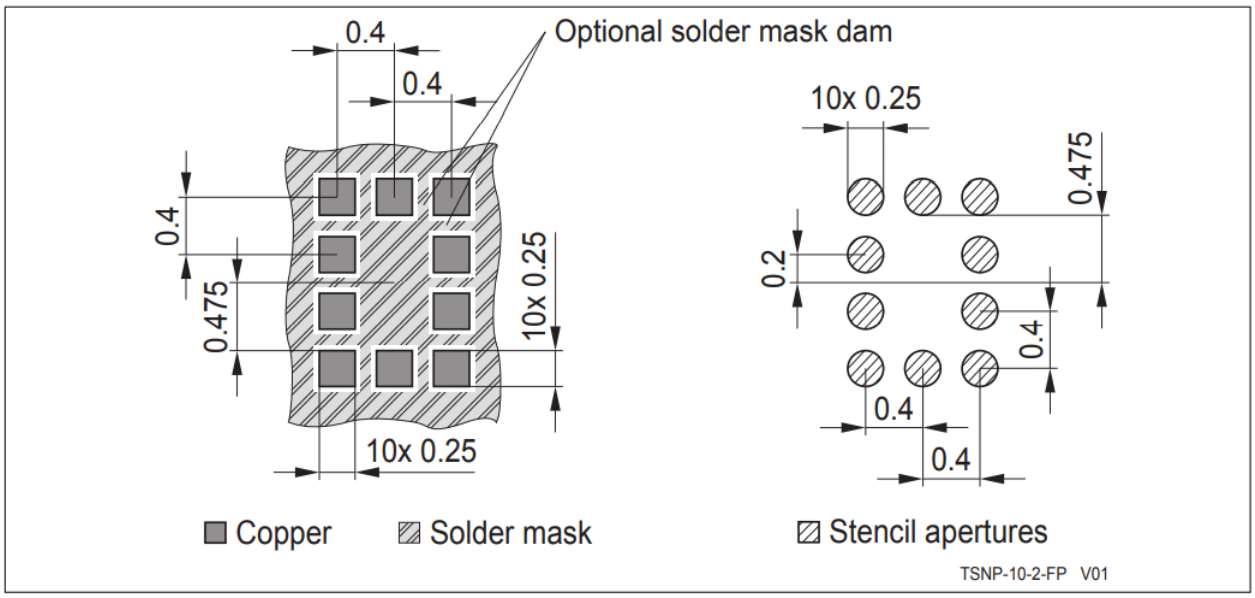

Figure 11: Land Pattern and Stencil Mask (TSNP-10-1/-2)

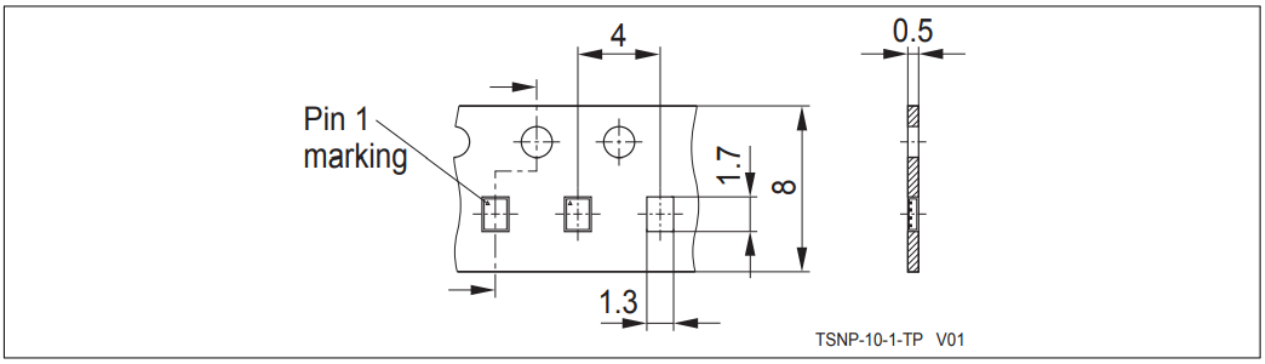

Figure 12: Carrier Tape (TSNP-10-1)

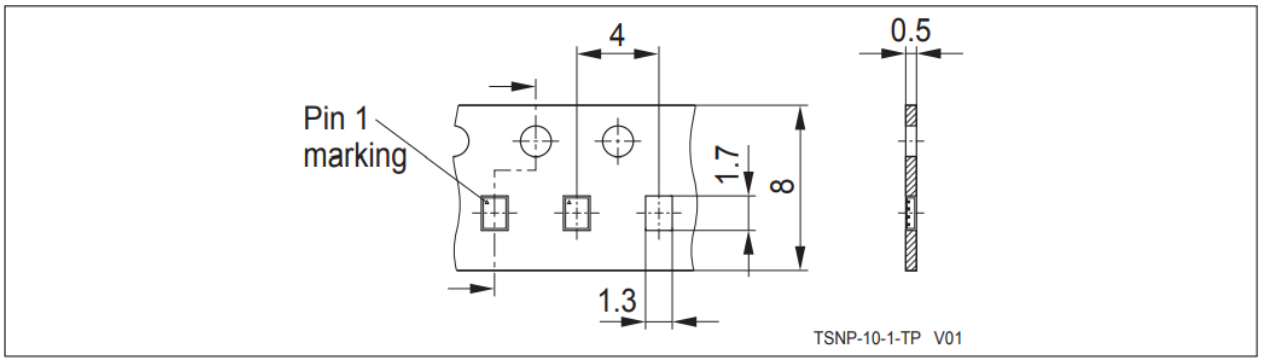

Figure 13: Carrier Tape (TSNP-10-2)