

CMT812X High-Speed, Dual-Channel Digital Isolator

1 Features

- Safety-related certifications
 - DIN VDE V 0884-11: 2017-01
 - UL 1577 component recognition program
 - CSA certification according to IEC 60950-1, IEC 62368-1, IEC 61010-1 and IEC 60601-1 end equipment standards
 - CQC approval per GB4943.1-2022
 - TUV certification according to EN 60950-1, EN 62368-1 and EN 61010-1
- Robust electromagnetic compatibility
 - System-level ESD, EFT, and surge immunity
 - ± 8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
 - Low emissions
- Data rate: up to 150 Mbps
- Wide supply range: 2.5 to 5.5 V
- Operation temperature: -40°C to 125°C
- Robust isolation barrier
 - More than 40-year projected lifetime
 - Up to 5 kV_{RMS} isolation rating
 - Up to 8 kV surge capability
 - ± 200 kV/ μ s typical CMTI
- Default output high or low options
- Low power consumption, typical 1.5 mA per channel at 1 Mbps
- Low propagation delay: 9 ns typical (5V supplies)
- SOIC-16 package (wide body), WB(N) SOW8L and SOIC-8 (narrow body)

2 Applications

- Industrial automatic control
- New energy vehicles
- Solar inverters
- Motor control
- Isolated SPI
- General purpose multichannel isolation

3 Description

The CMT812X series devices are high-performance, quad channel digital isolators with as high as 5 kV_{rms} isolation voltage by means of silicon-dioxide (SiO₂) insulation barrier.

The digital isolator is used to communicate between two different power supply domains while prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

This device comes with enable pins that can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The CMT812X device has two forward and one reverse-direction channels. If the input power or signal is lost, the default output is high for the CMT812X1 device and low for the CMT812X0 device. See the Device Functional Modes section for further details.

The isolator provides high electromagnetic immunity and low emissions at low-power consumption. Through innovative chip design and layout techniques, electromagnetic compatibility of the CMT812X device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

The CMT812X series device is available in both narrow-body (NB) and (WB) SOW8L / (WB) 16-pin SOIC packages.

Device Information

Part No.	Package	Body Size (mm x mm)
CMT812X	NB(N) SOIC-8	4.9 x 3.9
	WB(W) SOW8L	5.85 x 7.5
	WB(W) SOIC-16	10.4 x 7.5

Refer to section 14 for ordering information.

Simplified Schematic

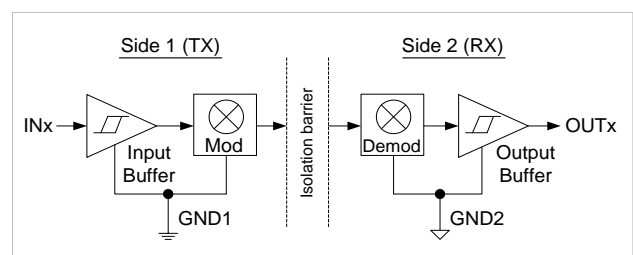


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4 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings^[1]

Parameters	Symbol	Condition	Min.	Max.	Unit
Power supply voltage ^[2]	VDD1, VDD2		-0.5	6.5	V
Maximum input voltage	IN _x	x = A, B	-0.4	VDD+0.4	V
Maximum output voltage	OUT _x	x = A, B	-0.4	VDD+0.4	V
Maximum Input / output pulse voltage	-	Pulse width should be less than 100 ns, and the duty cycle should be less than 10%	-0.8	VDD+0.8	V
Common-mode transient immunity	CMTI		±200		kV/us
Output current	I _o		-15	15	mA
Maximum surge immunity	-			8	kV
Operating temperature	T _A		-40	125	°C
Storage temperature	T _{STG}		-40	150	°C

Notes:

[1]. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

[2]. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

5 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	VDD1, VDD2		2.5	5	5.5	V
High level input voltage	V _{IH}	VDDI: input side VDD	0.7*VDD		VDDI	V
Low level input voltage	V _{IL}	VDDI: input side VDD	0		0.3VDD	V
Data rate	DR		0		150	Mbps
Operating temperature	T _A		-40	25	125	°C
Junction temperature	T _J		-40		150	°C

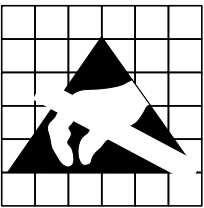
6 ESD Ratings

Table 3. ESD Ratings

Parameter	Symbol	Condition	Max.	Unit
Electrostatic discharge	V_{ESD}	Human-body model (HBM)	±8000	V
		Charged-device model (CDM)	±2000	

Notes:

- IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
- Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

7 Pin Description

Both narrow-body (N) and wide-body (W) 16-pin SOIC packages are available for the series part number CMT8120x, CMT8121x and CMT8122x. The pin lists are shown as below.

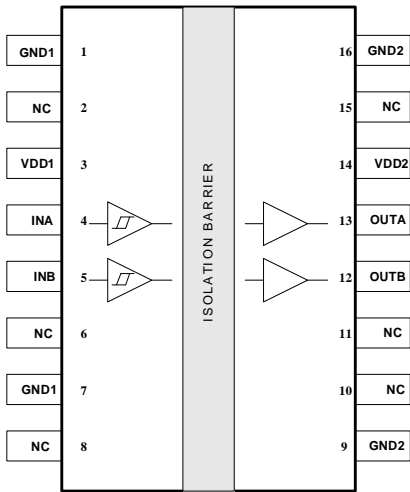


Figure 1. CMT8120WXM

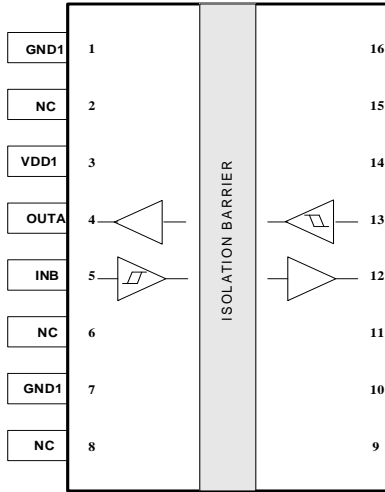


Figure 2. CMT8121WXM Pin List

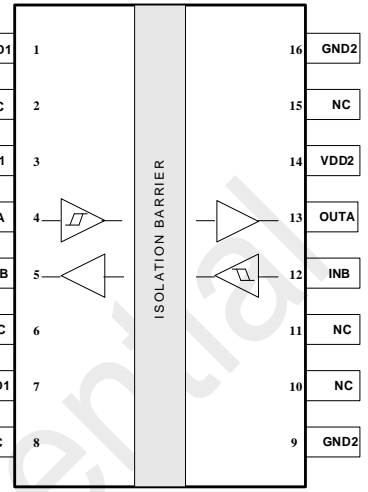


Figure 3. CMT8122WXM Pin List

Pin List

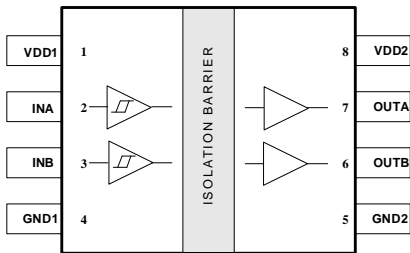


Figure 4. CMT8120NX /
CMT8120WX Pin List

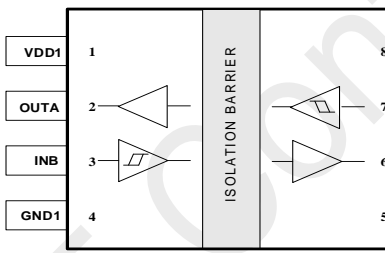


Figure 5. CMT8121NX/
CMT8121WX Pin List

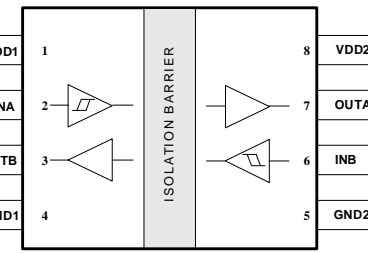


Figure 6. CMT8122NX /
CMT8122WX Pin List

Table 4. CMT8120 / 21 / 22X Pin Description

Pin Name	Pin Nmuber						I/O	Description
	WB SOIC-16			NB SOIC-8/ SOW8L				
	CMT8120W	CMT8121W	CMT8122W	CMT8120N	CMT8121N	CMT8122N		
GND1	1	1	1	4	4	4	-	Left ground
	7	7	7					
GND2	9	9	9	5	5	5	-	Right ground
	16	16	16					
INA	4	13	4	2	7	2	I	Input, channel A
INB	5	5	12	3	3	6	I	Input, channel B
NC	2, 6, 8, 10,11,15	2, 6, 8, 10,11,15	2, 6, 8, 10,11,15	-	-	-	-	Disconnect / connect to the GND
OUTA	13	4	13	7	2	7	O	Output, channel A
OUTB	12	12	5	6	6	3	O	Output, channel B
VDD1	3	3	3	1	1	1	-	Power supply for left side
VDD2	14	14	14	8	8	8	-	Power supply for right side

8 Typical Application

8.1 Typical Application Schematic

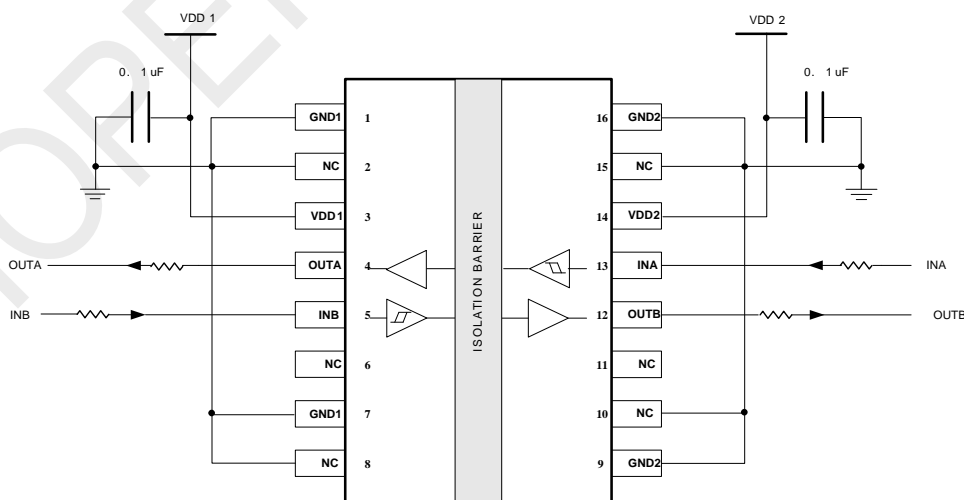


Figure 7. Typical Application Schematic (Take the CMT8121WXM as an example)

Note: users should be careful not to connect ground and VDD reversely.

8.2 PCB Layout Guidelines

The CMT812X requires a 0.1 μF bypass capacitor in both input side and output side. The capacitor should be placed as close as possible to the package pin of VDD1 and VDD2 respectively. The figures below show the recommended PCB layout. Please make sure the space under the chip keeps free from planes, traces, pads and via. To enhance the robustness of design, users may also include resistors (50 ~ 300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately $50 \Omega \pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

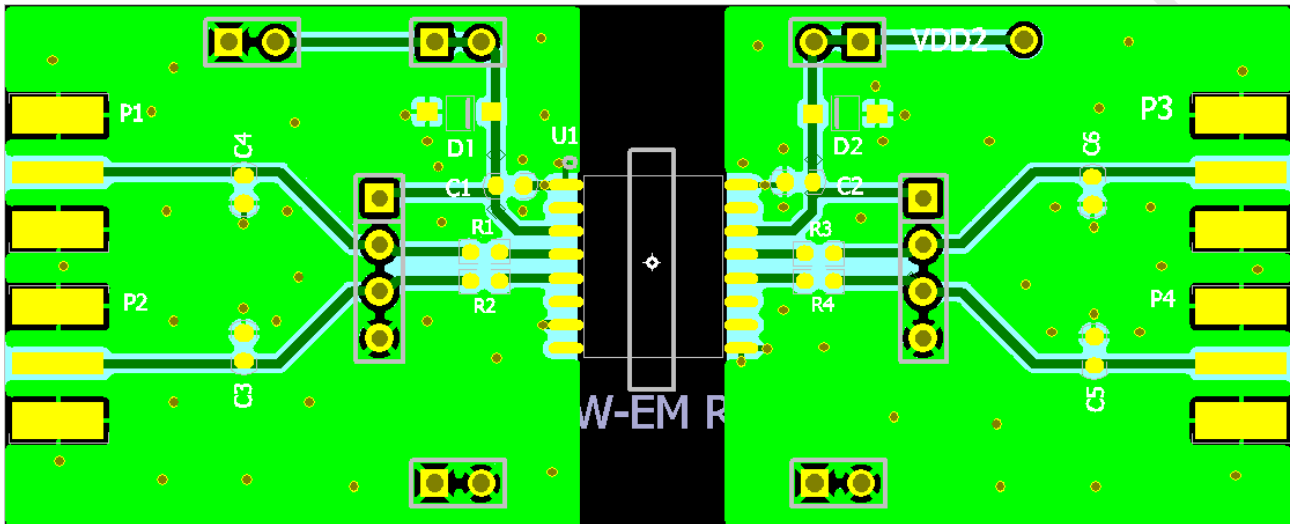


Figure 8. Recommended PCB Layout

9 Parameter Measurement Circuit Setup

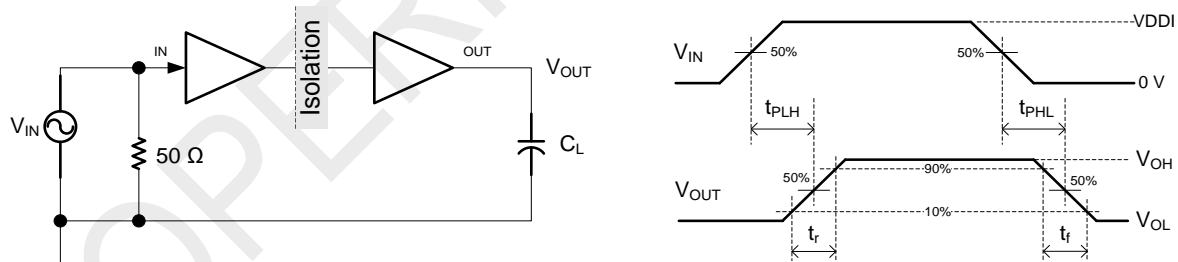


Figure 9. Switching Characteristics Test Circuit and Voltage Waveforms

Notes:

1. The input pulse is supplied by a generator V_{IN} having the following characteristics: $f_{PULSE} \leq 100 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_O = 50 \Omega$. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. Load capacitance influences the measurement results quite a lot, including instrumentation and fixture capacitance, totally no more than 15 pF loading is preferred.

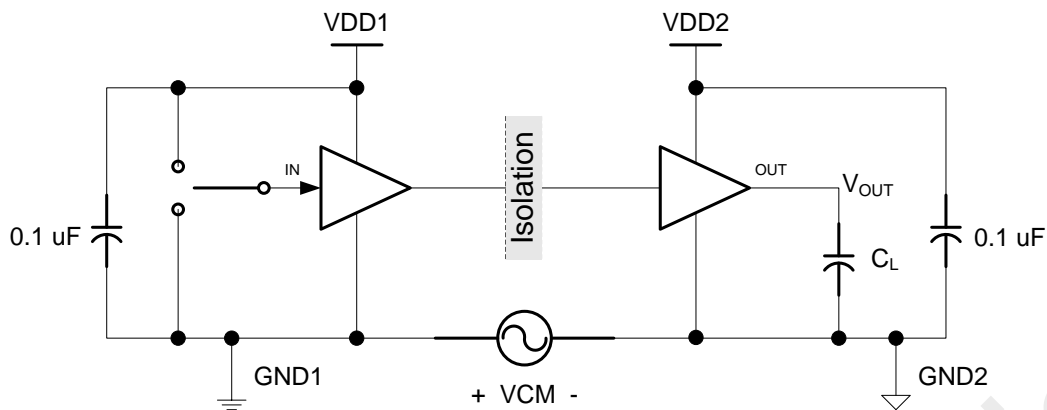


Figure 10. Common-Mode Transient Immunity Test Circuit

Notes:

1. $C_L = 15 \text{ pF}$, the total instrumentation and connection is within $\pm 20\%$.

10 Electrical Specifications

10.1 Electrical Characteristics with 5 V Supply

$V_{DD1} = V_{DD2} = 5\text{V}$, $T_A = -40$ to $125 \text{ }^\circ\text{C}$.

Table 5. Electrical Characteristics with 5 V Supply

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Power on reset	V_{POR}	POR threshold as during power-up		2.3		V
	V_{HYS}	POR threshold hysteresis		0.1		V
Input threshold	V_{IT}	Input threshold at rising edge			$0.7 \cdot V_{DD1}$	V
	V_{IT-}	Input threshold at falling edge	$0.3 \cdot V_{DD1}$			V
	V_{ITHYS}	Input threshold hysteresis		$0.2 \cdot V_{DD1}$		V
High level input voltage	V_{IH}		2			V
Low level input voltage	V_{IL}				0.8	V
High level output voltage	V_{OH}	$I_{OH} = -4\text{mA}$	$V_{DD} - 0.3$			V
Low level output voltage	V_{OL}	$I_{OL} = 4\text{mA}$			0.3	V
Output impedance	R_O			50		Ω
Input pull high or low current	I_{pull}			10	15	μA
Start-up time after POR	trbs			10		μs
Common mode transient	CMTI			± 200		$\text{kV}/\mu\text{s}$

10.2 Supply Current Characteristics with 5 V Supply

VDD1 = VDD2 = 5V, T_A = -40 to 125 °C.

Table 6. Supply Current Characteristics with 5 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8120				
Supply current EN = VDDI, V _{IN} = 0 V	I _{DD1}	0.67		mA
	I _{DD2}	1.14		mA
Supply current: device is disabled. EN = VDDI, V _{IN} = VDDI,	I _{DD1}	2.96		mA
	I _{DD2}	1.19		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.82		mA
	I _{DD2}	1.34		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.85		mA
	I _{DD2}	2.84		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C _L = 15 pF	I _{DD1}	2.29		mA
	I _{DD2}	9.82		mA
CMT8121				
Supply current EN = VDDI, V _{IN} = 0 V	I _{DD1}	1.12		mA
	I _{DD2}	1.14		mA
Supply current: device is disabled. EN = VDDI, V _{IN} = VDDI,	I _{DD1}	2.27		mA
	I _{DD2}	2.30		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.79		mA
	I _{DD2}	1.83		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C _L = 15 pF	I _{DD1}	2.21		mA
	I _{DD2}	2.25		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C _L = 15 pF	I _{DD1}	6.33		mA
	I _{DD2}	6.62		mA
CMT8122				
Supply current EN = VDDI, V _{IN} = 0 V	I _{DD1}	1.13		mA
	I _{DD2}	1.13		mA
Supply current: device is disabled. EN = VDDI, V _{IN} = VDDI,	I _{DD1}	2.35		mA
	I _{DD2}	2.30		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.83		mA
	I _{DD2}	1.82		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C _L = 15 pF	I _{DD1}	2.25		mA
	I _{DD2}	2.24		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C _L = 15 pF	I _{DD1}	6.32		mA
	I _{DD2}	6.60		mA

Table 7-1. Supply Current with 5 V Supply- Characteristics of CMT812X

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR		0	150		Mbps
Minimum pulse width	PW	See figure 6, $C_L = 15$ pF		5	5	ns
Propagation delay rising	t_{PLH}	See figure 6, $C_L = 15$ pF		9	15	ns
Propagation delay falling	t_{PHL}	See figure 6, $C_L = 15$ pF		9	15	ns
Pulse width distortion $ t_{PHL} - t_{PLH} $	PWD	See figure 6, $C_L = 15$ pF			5	ns
Rising time	t_r	See figure 6, $C_L = 15$ pF			5	ns
Falling time	t_f	See figure 6, $C_L = 15$ pF			5	ns
Peak eye diagram Jitter	$t_{JIT}(PK)$			400		ps
Channel-to-channel delay Skew	$t_{SK}(c2c)$			1.5	2.5	ns
Part-to-part delay skew	$t_{SK}(p2p)$				5	ns

10.3 Supply Current Characteristics with 3.3 V Supply

VDD1 = VDD2 = 3.3V, $T_A = -40$ to 125 °C.

Table 8. Supply Current Characteristics with 3.3 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8120				
Supply current EN = VDDI, $V_{IN} = 0$ V	I_{DD1}	0.67		mA
	I_{DD2}	1.14		mA
Supply current: device is disabled. EN = VDDI, $V_{IN} = VDDI$,	I_{DD1}	2.94		mA
	I_{DD2}	1.18		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	1.80		mA
	I_{DD2}	1.27		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	1.83		mA
	I_{DD2}	2.26		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	2.34		mA
	I_{DD2}	7.03		mA
CMT8121				
Supply current EN = VDDI, $V_{IN} = 0$ V	I_{DD1}	1.12		mA
	I_{DD2}	1.13		mA
Supply current: device is disabled. EN = VDDI, $V_{IN} = VDDI$,	I_{DD1}	2.25		mA
	I_{DD2}	2.29		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	1.71		mA
	I_{DD2}	1.75		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	2.01		mA
	I_{DD2}	2.05		mA

Parameter	Symbol	Typ.	Max.	Unit
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	4.92		mA
	I_{DD2}	4.91		mA
CMT8122				
Supply current EN = VDDI, $V_{IN} = 0$ V	I_{DD1}	1.14		mA
	I_{DD2}	1.14		mA
Supply current: device is disabled. EN = VDDI, $V_{IN} = VDDI$,	I_{DD1}	2.33		mA
	I_{DD2}	2.31		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	1.75		mA
	I_{DD2}	1.74		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	2.04		mA
	I_{DD2}	2.03		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, $C_L = 15$ pF	I_{DD1}	4.93		mA
	I_{DD2}	4.90		mA

Table 9-1. Supply Current with 3.3 V Supply - Characteristics of CMT812X

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR		0	150		Mbps
Minimum pulse width	PW	See figure 9, $C_L = 15$ pF			5	ns
Propagation delay rising	t_{PLH}	See figure 9, $C_L = 15$ pF		9.15	15	ns
Propagation delay falling	t_{PHL}	See figure 9, $C_L = 15$ pF		7.8	15	ns
Pulse width distortion $ t_{PHL} - t_{PLH} $	PWD	See figure 9, $C_L = 15$ pF		1.35	5	ns
Rising time	t_r	See figure 9, $C_L = 15$ pF		1.01	5	ns
Falling time	t_f	See figure 9, $C_L = 15$ pF		1.05	5	ns
Peak eye diagram Jitter	$t_{JIT(PK)}$			400		ps
Channel-to-channel Delay Skew	$t_{SK(c2c)}$			0.8	2.5	ns
Part-to-part delay skew	$t_{SK(p2p)}$				5	ns

10.4 Supply Current Characteristics with 2.5 V Supply

VDD1 = VDD2 = 2.5 V, T_A = -40 to 125 °C.

Table 10. Supply Current Characteristics with 2.5 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8120				
Supply current EN = VDDI, V _{IN} = 0 V	I _{DD1}	0.66		mA
	I _{DD2}	1.13		mA
Supply current: device is disabled. EN = VDDI, V _{IN} = VDDI,	I _{DD1}	2.93		mA
	I _{DD2}	1.18		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.79		mA
	I _{DD2}	1.24		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.82		mA
	I _{DD2}	2.00		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C _L = 15 pF	I _{DD1}	2.30		mA
	I _{DD2}	5.57		mA
CMT8121				
Supply current EN = VDDI, V _{IN} = 0 V	I _{DD1}	1.11		mA
	I _{DD2}	1.13		mA
Supply current: device is disabled. EN = VDDI, V _{IN} = VDDI,	I _{DD1}	2.24		mA
	I _{DD2}	2.28		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.65		mA
	I _{DD2}	1.69		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.86		mA
	I _{DD2}	1.90		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C _L = 15 pF	I _{DD1}	3.94		mA
	I _{DD2}	3.64		mA
CMT8122				
Supply current EN = VDDI, V _{IN} = 0 V	I _{DD1}	1.14		mA
	I _{DD2}	1.13		mA
Supply current: device is disabled. EN = VDDI, V _{IN} = VDDI,	I _{DD1}	2.32		mA
	I _{DD2}	2.30		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.74		mA
	I _{DD2}	1.72		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C _L = 15 pF	I _{DD1}	1.94		mA
	I _{DD2}	1.92		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C _L = 15 pF	I _{DD1}	3.98		mA
	I _{DD2}	3.63		mA

Table 11-1. Supply Current with 2.5 V Supply - Characteristics of CMT812X

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR		0	150		Mbps
Minimum pulse width	PW	See figure 6, $C_L = 15$ pF		5	5	ns
Propagation delay rising	t_{PLH}	See figure 6, $C_L = 15$ pF		9	15	ns
Propagation delay falling	t_{PHL}	See figure 6, $C_L = 15$ pF		9	15	ns
Pulse width distortion $t_{PHL} - t_{PLH}$	PWD	See figure 6, $C_L = 15$ pF			5	ns
Rising time	t_r	See figure 6, $C_L = 15$ pF			5	ns
Falling time	t_f	See figure 6, $C_L = 15$ pF			5	ns
Peak eye diagram Jitter	$t_{JIT(PK)}$			400		ps
Channel-to-channel Delay Skew	$t_{SK(c2c)}$			2.5	2.5	ns
Part-to-part delay skew	$t_{SK(p2p)}$			5	5	ns

10.5 Typical Characteristics

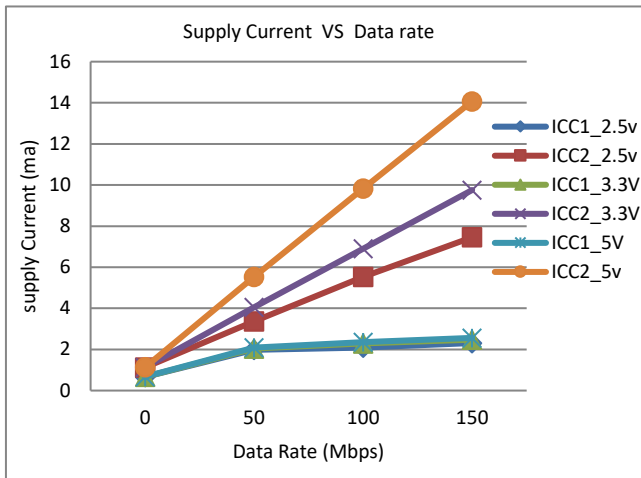


Figure 11. Supply Current vs. Data Rate (with 15-pF Load) $T_A=25^\circ\text{C}$ $C_L=15\text{pF}$

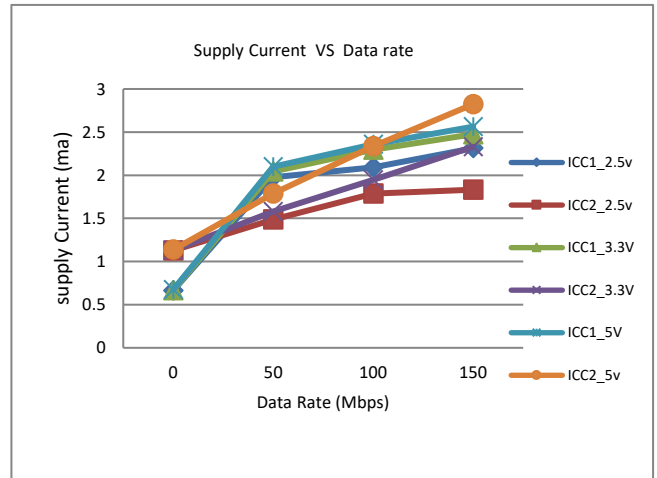


Figure 12. Supply Current vs. Data Rate (with No Load) $T_A=25^\circ\text{C}$ $C_L=\text{No Load}$

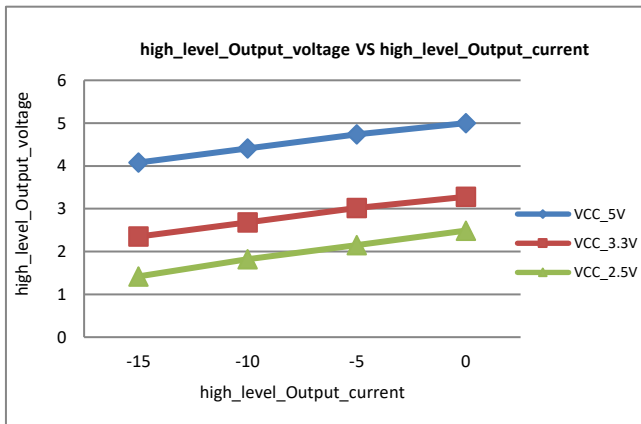


Figure 13. High-Level Output Voltage vs. High-Level Output Current ($T_A=25^\circ\text{C}$)

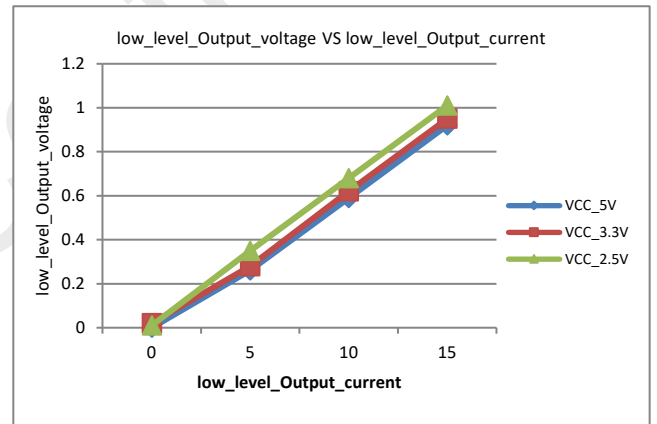


Figure 14. Low-Level Output Voltage vs. Low-Level Output Current ($T_A=25^\circ\text{C}$)

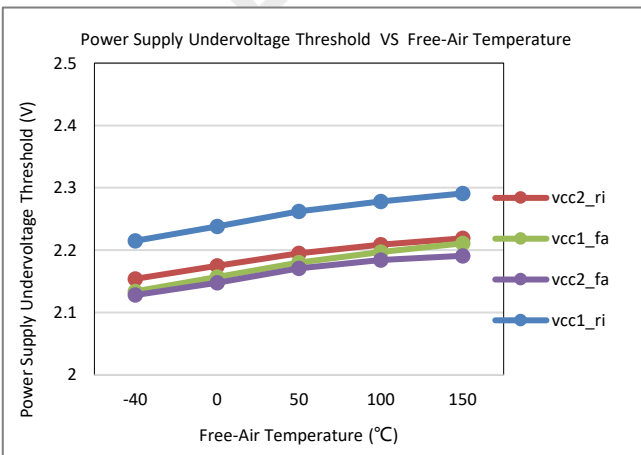


Figure 15. Power Supply Under-voltage Threshold vs. Free-Air Temperature

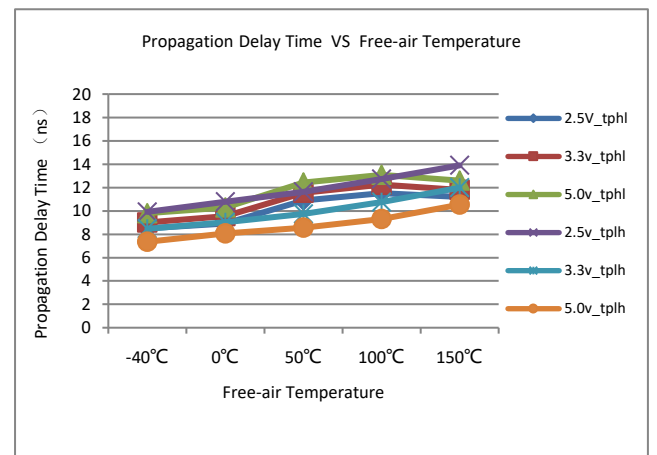


Figure 16. Propagation Delay Time vs. Free-Air Temperature

10.6 Insulation Specifications

Table 12. Insulation Specifications

Parameters	Sym.	Condition	Value		Unit
			NB	WB SOIC-16/SOW8L	
External clearance ^[1]	CLR	The shortest terminal-to-terminal distance through air	4.0	8.0	mm
External creepage ^[1]	CRP	The shortest terminal-to-terminal distance across the package surface	4.0	8.0	mm
Distance through insulation	DTI	Minimum internal gap	20	20	um
Comparative tracking index	CTI	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	> 400	V
Material group	-		1	1	-
Overvoltage category per IEC 60664-1	-	Rated mains voltage $\leq 300 V_{RMS}$	I	I	-
		Rated mains voltage $\leq 600 V_{RMS}$	I-IV	I-IV	-
		Rated mains voltage $\leq 1000 V_{RMS}$	I-III	I-III	-
DIN VDE V 0884-11:2017-01^[2]					
Maximum repetitive isolation voltage	V_{IORM}		565	1176	V_{pk}
Maximum isolation working voltage	V_{IOWM}	AC voltage (sine wave); Time dependent dielectric breakdown (TDDB) test	400	831	V_{RMS}
		DC voltage	565	1176	V_{DC}
Maximum transient isolation voltage	V_{IOTM}	$V_{TEST} = V_{IOTM}, t = 60$ s (qualification); $t = 1$ s (100% production)	5300	7000	V_{pk}
Maximum surge isolation voltage ^[3]	V_{IOSM}	Test method per IEC60065, 1.2/50 us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	5384	6250	V_{pk}
Apparent charge ^[4]	q_{pd}	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10$ s	≤ 5	≤ 5	$\leq 5pC$
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_m = 10$ s	≤ 5	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, $t_{ini} = 1$ s; $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m = 1$ s	≤ 5	≤ 5	
Isolation capacitance, input to output ^[5]	C_{IO}	$V_{IO} = 0.4 \times \sin(2\pi ft)$, $f = 1$ MHz	0.6	0.6	pF
Isolation resistance, input to output ^[5]	R_{IO}	$V_{IO} = 500$ V	$>10^{10}$	$>10^{10}$	Ω
UL 1577					
Withstand isolation voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, $t = 60$ s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1$ s (100% production)	3750	5000	V_{RMS}

Notes:

- [1]. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- [2]. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- [3]. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- [4]. Apparent charge is electrical discharge caused by a partial discharge (pd).
- [5]. All pins on each side of the barrier are tied together creating a two-terminal device.

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10.7 Safety-related Certifications

Table 13. Safety-related Certifications

VDE	UL		CQC	TUV
DIN VDE V0884-11:2017-01 (Patents pending)	UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	GB 4943.1-2011 (SOP8)	EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2: 2013 (Patents pending)
Certificate number: pending	Certificate number: UL-US-2439077-0	Certificate number: UL-CA-2429797-0	Certificate number: CQC23001382478	Client ID number: pending

10.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures

Table 14. Safety Limiting Values

Parameters	Symbol	Test Condition	Value		Unit
			NB SOIC-16	WB SOIC-16/SOW8L	
Safety input, output, or supply current	Is	$R_{\theta JA} = 140 \text{ }^{\circ}\text{C/W}$, $V_I = 5.5 \text{ V}$, $T_J = 125 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$	160		mA
		$R_{\theta JA} = 84 \text{ }^{\circ}\text{C/W}$, $V_I = 5.5 \text{ V}$, $T_J = 125 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$		237	mA
Total power dissipation at 25°C	Ps			1499	mW
Case temperature	Ts		125	125	°C

10.9 Thermal Information

Table 15. Thermal Information

Parameter	Symbol	Value		Unit
		NB SOIC-8	WB SOIC-16/ SOW8L	
Junction-to-ambient thermal resistance	θ_{JA}	78.9	78.9	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC (top)}$	41.1	41.6	°C/W
Junction-to-board thermal resistance	θ_{JB}	49.5	43.6	°C/W

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11 Function Description

11.1 Function Overview

The CMT812X device is a high-performance, quad-channel digital isolator with 5000 V_{RMS} isolation rating. The CMT812X has an On-Off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The CMT812X also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The figure below shows a conceptual detail of how the On-Off keying scheme works.

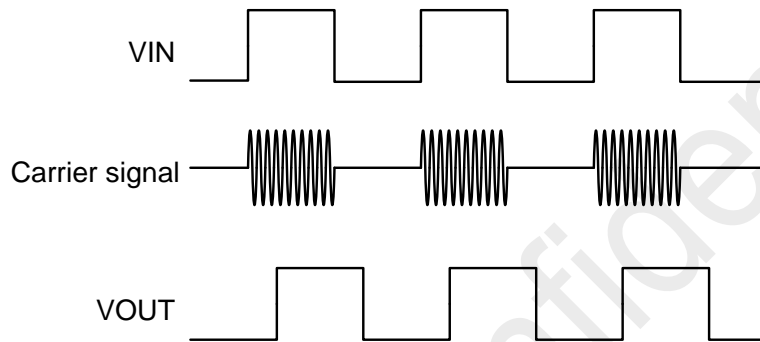


Figure 17. On-Off Keying Based Modulation Scheme

11.2 Functional Modes

The table below lists the functional modes of the CMT812X.

Table 16. Function Table^[1]

VDD1	VDD2	Input (INx) ^[2]	Output (OUTx)	Comment
PU	PU	H	H	Normal operation: A channel output assumes the logic state of its input
		L	L	
		Open	Default	Default mode: when INx is open, the corresponding channel output goes to its default logic state
PD	PU	X	Default	Default mode: when VDD1 is unpowered, a channel output assumes the logic state based on the selected default option. When VDD1 transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When VDD1 transitions from powered-up to unpowered, channel output assumes the selected default state
X	PD	X	Undetermined	When VDD2 is unpowered, a channel output is undetermined ^[3] . When VDD2 transitions from unpowered to powered-up, a channel output assumes the logic state of the input

11.3 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See the figure below for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line

with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

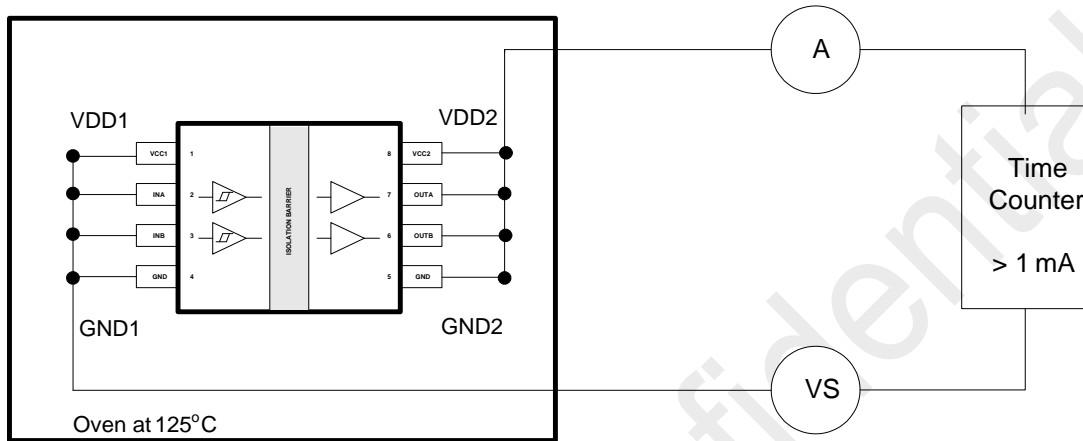


Figure 18. Test Setup for Insulation Lifetime Measurement

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12 Packaging Information

The packaging information of the CMT812X SOIC16 is shown in the figures below.

12.1 CMT812X Narrow Body SOIC-8 Packaging

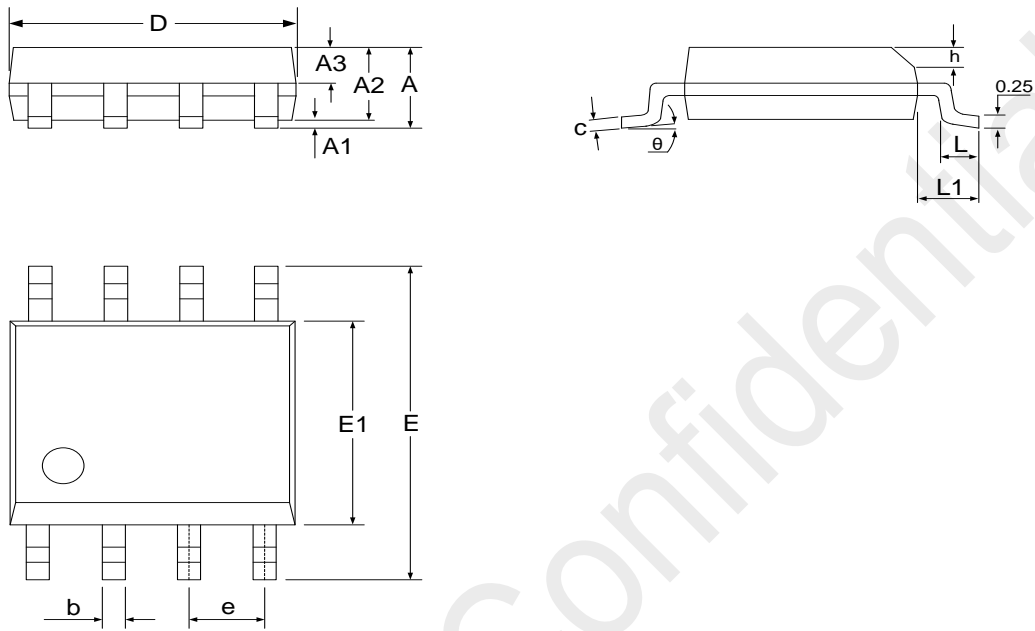


Figure 19. Narrow Body SOIC-8 Packaging

Table 17. Narrow Body SOIC-8 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
c	0.21	-	0.26
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05 BSC		
θ	0	-	8°

12.2 CMT812X Wide Body SOW8L Packaging

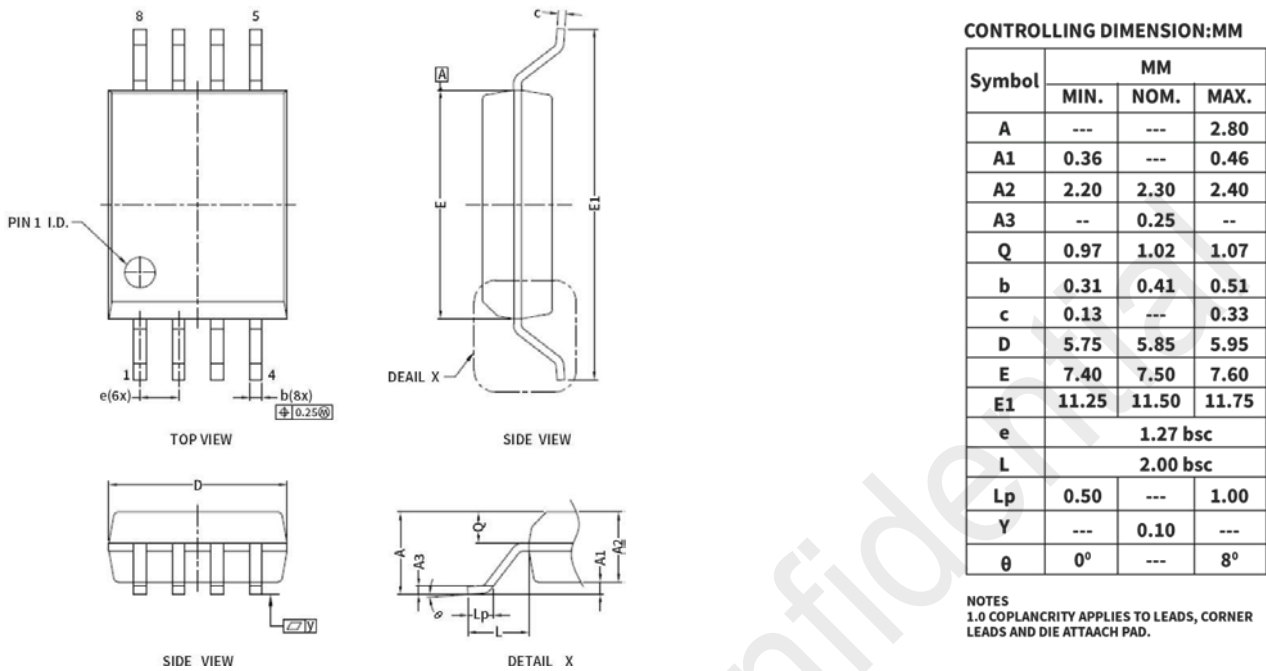


Figure 20. CMT812X SOW8L Package

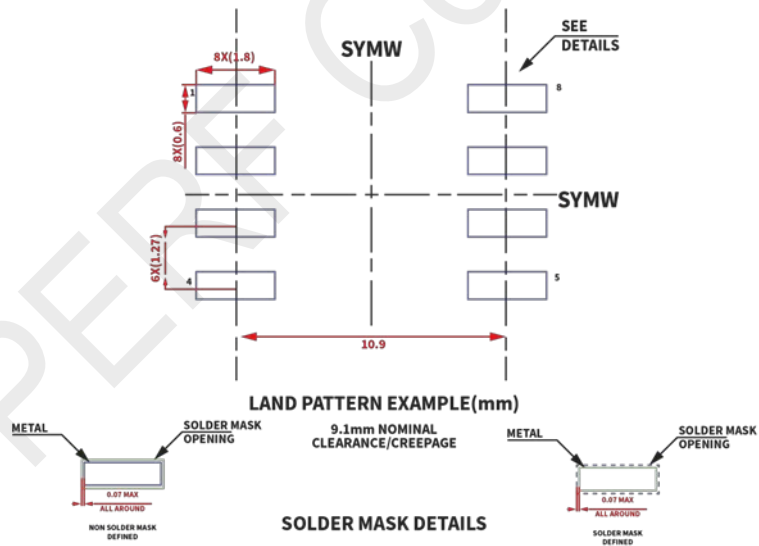


Figure 21. CMT812X SOW8L Package Board Layout Example

12.3 CMT812X Wide Body SOIC-16 Packaging

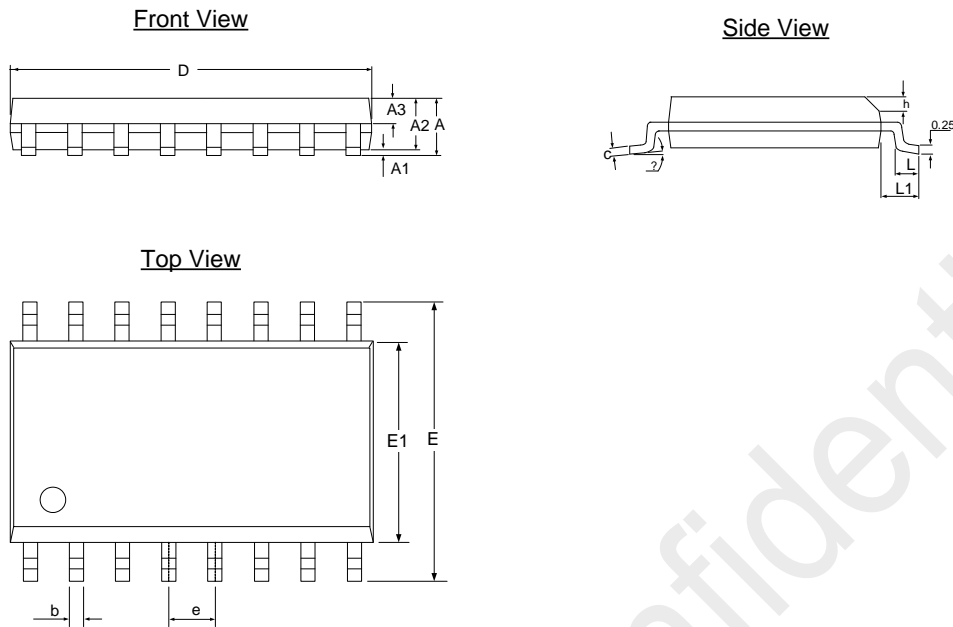


Figure 22. Wide Body SOIC-16 Packaging

Table 18. Wide Body SOIC-16 Packaging Scale

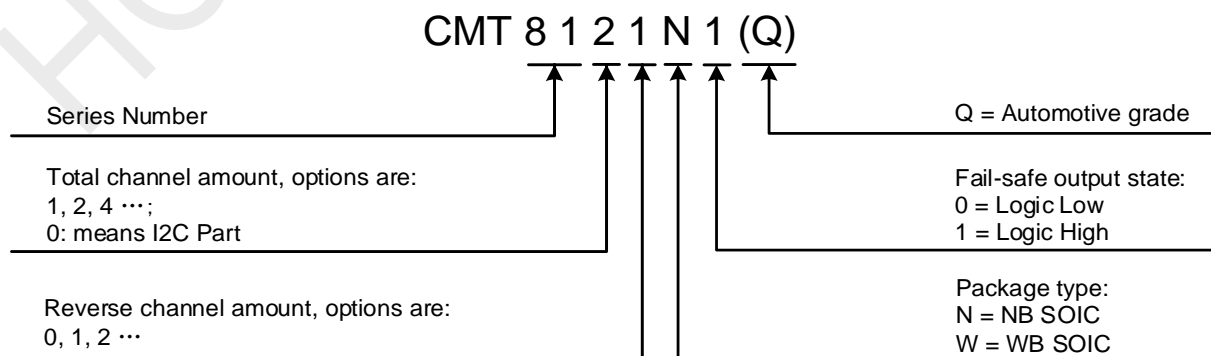
Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	0.20	0.30
A2	2.25	2.30	2.35
A3	1.00	1.05	1.10
b	0.35	0.37	0.43
c	0.15	0.20	0.30
D	10.30	10.40	10.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.14	1.27	1.40
L	0.65	0.70	0.85
L1	1.40		
θ	0	-	8°

13 Ordering Information

Table 19. Part Number List

Part Number	Min. Order Quantity	Withstand Voltage (rms)	Numbers of Total Channels	Numbers of Forward Channel	Numbers of Reversed Channel	Digital Rate (MHz)	Default Output State	Package
CMT8120W0	1000	5000	2	2	0	150	Low	WB SOIC-16
CMT8120W0M	1000	5000	2	2	0	150	Low	WB SOIC-16
CMT8120W1M	1000	5000	2	2	0	150	High	WB SOIC-16
CMT8121W0M	1000	5000	2	1	1	150	Low	WB SOIC-16
CMT8121W1M	1000	5000	2	1	1	150	High	WB SOIC-16
CMT8122W0M	1000	5000	2	1	1	150	Low	WB SOIC-16
CMT8122W1M	1000	5000	2	1	1	150	High	WB SOIC-16
CMT8120W0	1000	5000	2	2	0	150	Low	SOW8L
CMT8120W1	1000	5000	2	2	0	150	High	SOW8L
CMT8121W0	1000	5000	2	1	1	150	Low	SOW8L
CMT8121W1	1000	5000	2	1	1	150	High	SOW8L
CMT8122W0	1000	5000	2	1	1	150	Low	SOW8L
CMT8122W1	1000	5000	2	1	1	150	High	SOW8L
CMT8120N0	3000	3750	2	2	0	150	Low	NB SOIC-8
CMT8120N1	3000	3750	2	2	0	150	High	NB SOIC-8
CMT8121N0	3000	3750	2	1	1	150	Low	NB SOIC-8
CMT8121N1	3000	3750	2	1	1	150	High	NB SOIC-8
CMT8122N0	3000	3750	2	1	1	150	Low	NB SOIC-8
CMT8122N1	3000	3750	2	1	1	150	High	NB SOIC-8

Part Number Naming Rule:



Please visit www.hoperf.com for more product/product line information.

Please contact sales@hoperf.com or your local sales representative for sales or pricing requirements.

14 Tape and Reel Information

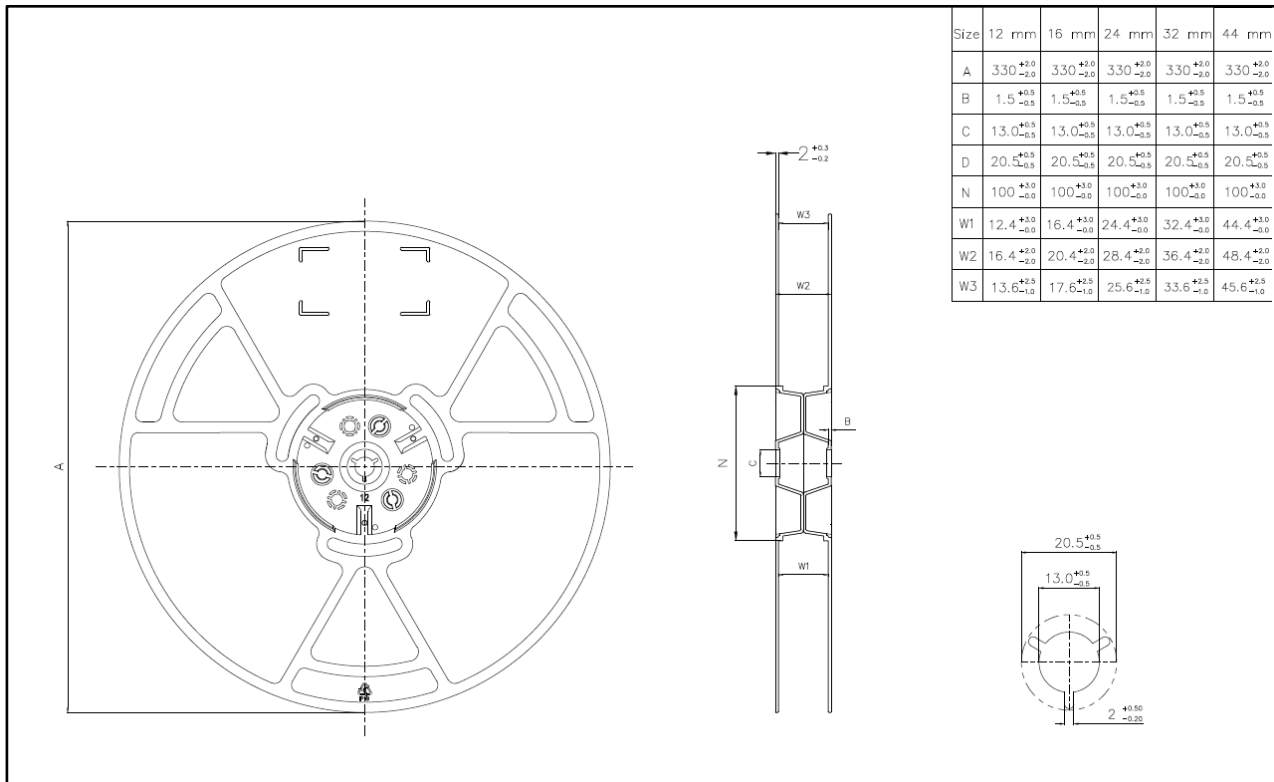


Figure 23. CMT812X WB SOIC-16 Tape & Reel Information

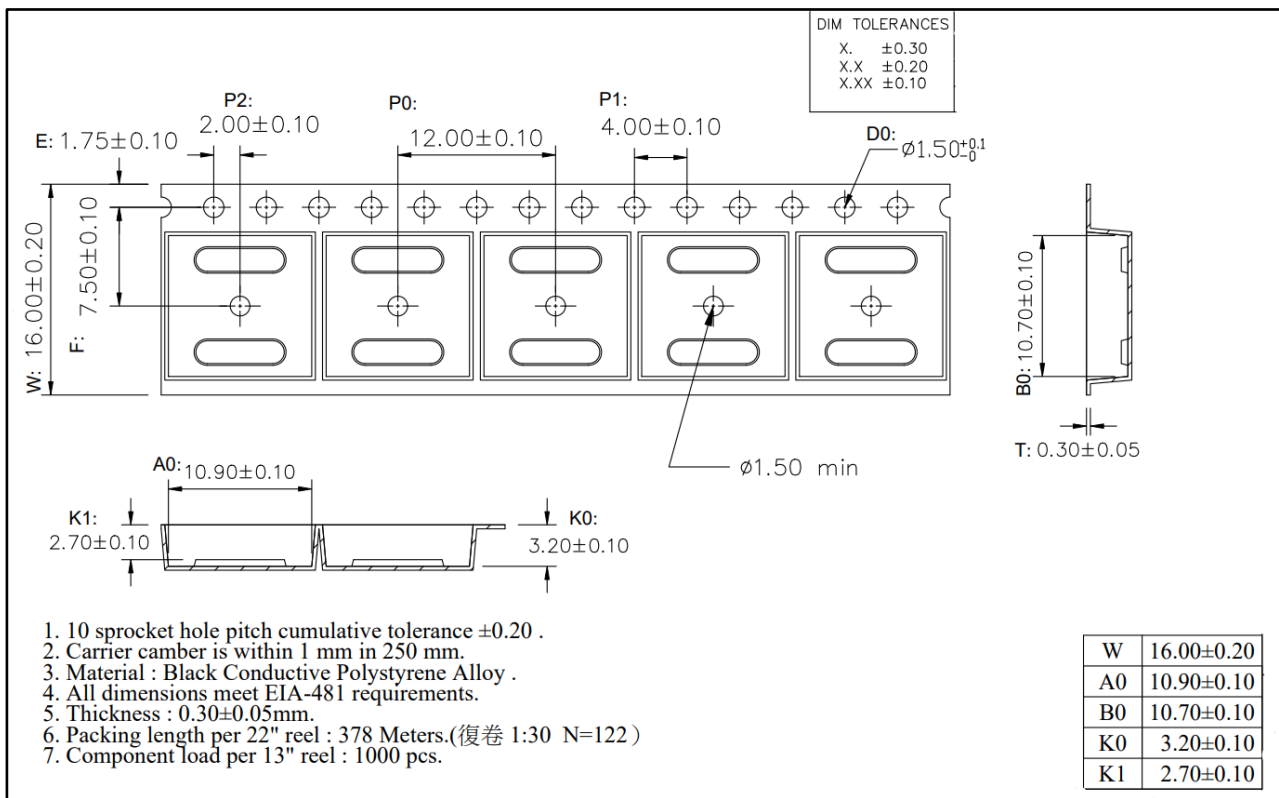


Figure 24. CMT812X WB SOIC-16 Tape & Reel Information

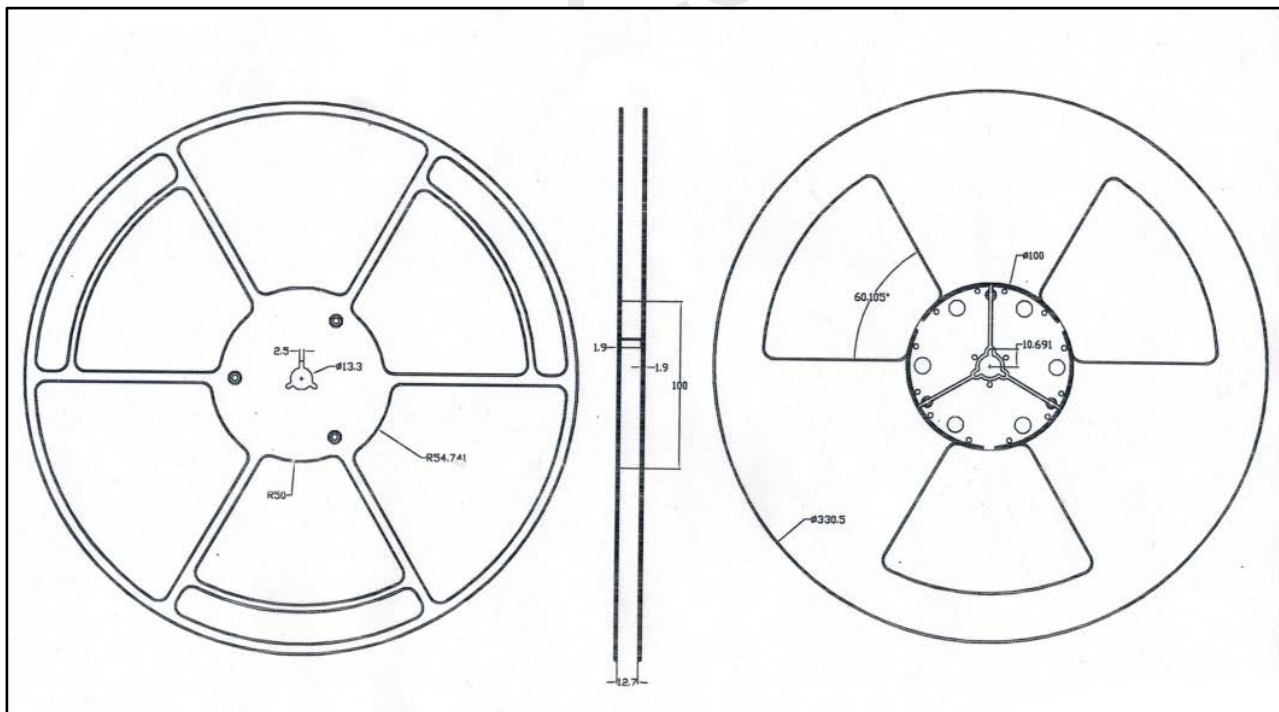


Figure 25. CMT812X NB SOIC-8 Tape & Reel Information

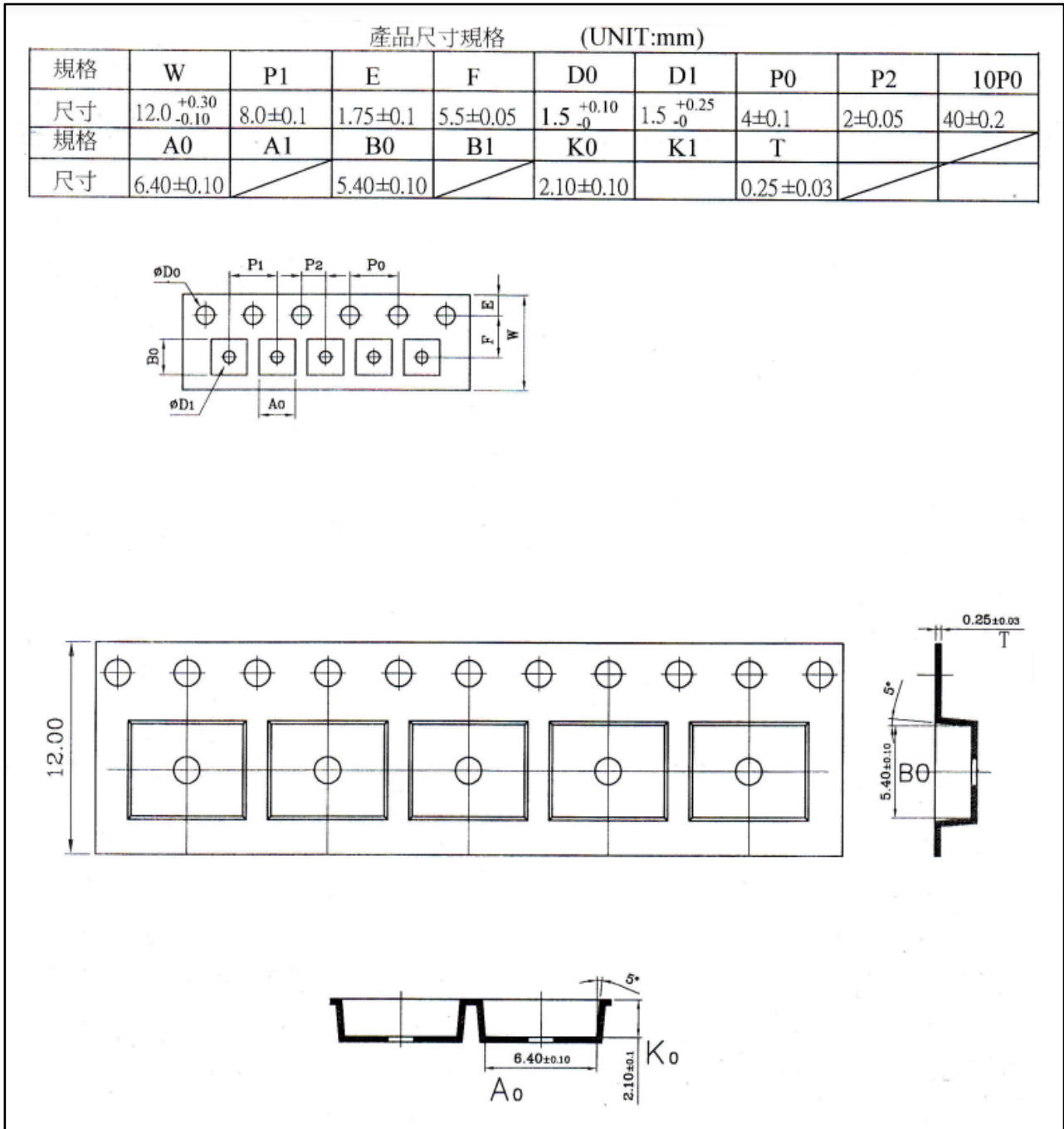


Figure 26. CMT812X NB SOIC-8 Tape & Reel Information

15 Revise History

Table 20. Revise Record

Version No.	Chapter	Description	Date
0.1	All	Initial version	2023/02/22
0.2	15	Added Tape information in Chapter 15	2023/03/09
	14	Update order information	
0.3	All	Delete the silver printing part	2023/04/19
		Added the CQC certificate number	
0.4	All	Added package information of SOW8L	2023/11/07
0.5	All	Update the surge immunity value to 8 kV	2024/01/16
0.6	All	Update order information	2024/4/30

16 Contacts

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