

RoHS Compliant

8GB DDR5 SDRAM CSO-DIMM

Fully lead-free / Halogen free

Product Specifications

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Version 1.2



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General Description

Apacer **DP2.37493H.001** is a 8GB DDR5 SDRAM (Synchronous DRAM) SO-DIMM. This memory module consists of 4 pieces 1G x 16 bits DDR5 synchronous DRAMs in FBGA packages and 8K Bits EEPROM. The module is a 262-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Density	Speed	Organization	DRAM Composition	Rank
DP2.37493H.001	8GB	6400 Mbps	1Gx64	1Gx16 *4	1

Key Parameters

Speed	DDR5-6400	Unit
	-CL52	
tCK (min)	0.312	ns
CAS latency	52	nCK
tRCD (min)	16	ns
tRP (min)	16	ns
tRAS (min)	32	ns
tRC (min)	48	ns
CL-tRCD-tRP	52-52-52	nCK

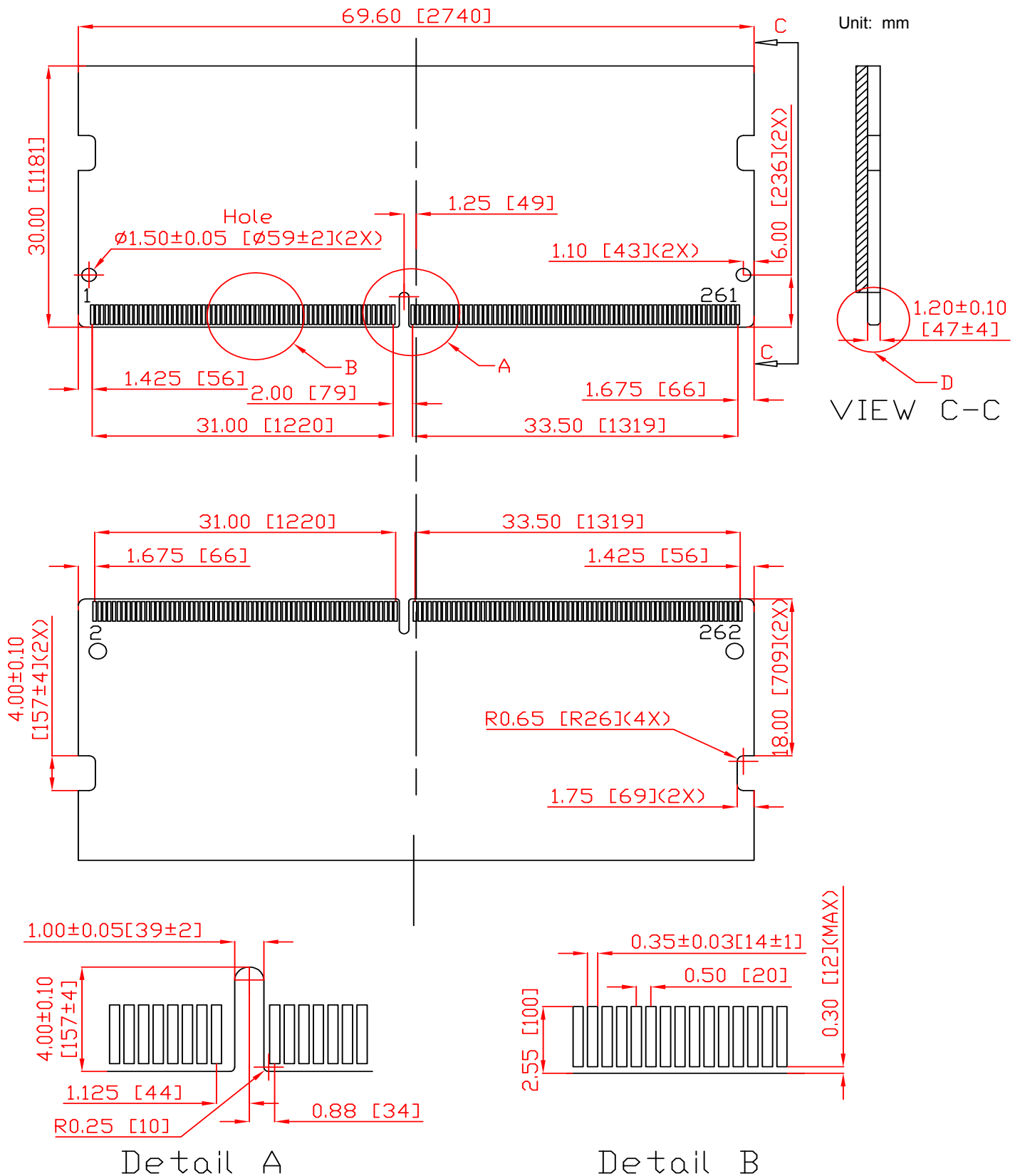
Features:

- ◆ JEDEC standard compliant
- ◆ On-DIMM thermal sensor : Yes
- ◆ PCB: height 30 mm, lead pitch 0.5 mm (pin),
- ◆ VDD = VDDQ= 1.1V (1.067V to 1.166V)
- ◆ VPP = 1.8V (1.746V to 1.908V) 、 VDDSPD = 1.8V
- ◆ 32 internal banks (x4, x8): 8 groups of 4 banks each
- ◆ 16 internal banks (x16): 4 groups of 4 banks each
- ◆ CAS Latency (CL): 22,26,28,30,32,36,40,42,46,48,50,52,54,56
- ◆ CAS Write Latency (CWL): RL-2
- ◆ Operating temperature Tcase—(0°C ~85°C)
- ◆ Average Refresh period 3.9us at lower than Tcase 85°C, 1.95us at 85°C < Tcase < 95 °C.
- ◆ All bank and same bank refresh
- ◆ Bi-Directional Differential Data Strobe
- ◆ 16-bit prefetch architecture
- ◆ On-die ECC
- ◆ ECC transparency and error scrub
- ◆ sPPR and hPPR capability
- ◆ Halogen free
- ◆ Fully lead-free (RoHS compliant without exemptions)
- ◆ DDR5 Clock Driver

Pin Assignments

Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
1	VIN_BULK	2	HSA	133	CK0_A_c	134	CK1_A_c
3	VIN_BULK	4	HSCL	135	VSS	136	VSS
5	RFU	6	HSDA	137	CK0_B_t	138	CK1_B_t
7	PWR_GOOD	8	PWR_EN	139	CK0_B_c	140	CK1_B_c
9	VSS	10	VSS	141	VSS	142	VSS
11	DQ0_A	12	DQ1_A	143	RFU	144	CA12_B
13	VSS	14	VSS	145	CA11_B	146	CA10_B
15	DQ2_A	16	DQ3_A	147	VSS	148	VSS
17	VSS	18	VSS	149	CA9_B	150	CA8_B
19	DM0_A_n	20	DQS0_A_c	151	CA7_B	152	CA6_B
21	VSS	22	DQS0_A_t	153	VSS	154	VSS
23	DQ4_A	24	VSS	155	CA5_B	156	CA4_B
25	VSS	26	DQ5_A	157	CA3_B	158	CA2_B
27	DQ6_A	28	VSS	159	VSS	160	VSS
29	VSS	30	DQ7_A	161	CS0_B_n	162	CA1_B
31	DQ8_A	32	VSS	163	RESET_n	164	CA0_B
33	VSS	34	DQ09_A	165	CS1_B_n	166	VSS
35	DQ10_A	36	VSS	167	VSS	168	CB0_B
37	VSS	38	DQ11_A	169	DQS4_B_c	170	VSS
39	DQS1_A_c	40	VSS	171	DQS4_B_t	172	CB1_B
41	DQS1_A_t	42	DM1_A_n	173	VSS	174	VSS
43	VSS	44	VSS	175	CB3_B	176	CB2_B
45	DQ12_A	46	DQ13_A	177	VSS	178	VSS
47	VSS	48	VSS	179	DQ0_B	180	DQ1_B
49	DQ14_A	50	DQ15_A	181	VSS	182	VSS
51	VSS	52	VSS	183	DQ2_B	184	DQ3_B
53	DQ16_A	54	DQ17_A	185	VSS	186	VSS
55	VSS	56	VSS	187	DM0_B_n	188	DQS0_B_c
57	DQ18_A	58	DQ19_A	189	VSS	190	DQS0_B_t
59	VSS	60	VSS	191	DQ4_B	192	VSS
61	DM2_A_n	62	DQS2_A_c	193	VSS	194	DQ5_B
63	VSS	64	DQS2_A_t	195	DQ6_B	196	VSS
65	DQ20_A	66	VSS	197	VSS	198	DQ7_B
67	VSS	68	DQ21_A	199	DQ8_B	200	VSS
69	DQ22_A	70	VSS	201	VSS	202	DQ9_B

Mechanical Drawing



Revision History

Revision	Date	Description	Remark
1.0	4/12/2022	Initial release	
1.1	11/4/2022	Updated DIMM Voltage Requirements	
1.2	16/2/2024	Add Fully lead-free description	

Global Presence

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