

# **Application Note**

**Document No.: AN1096** 

APM32F035\_HvMOTOR EVAL Senseless

**Vector Control Scheme** 

**Version: V1.1** 



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## 1 General Introduction

## 1.1 **Project Overview**

APM32F035 is a specialized chip launched by Geehy Semiconductor Co., Ltd. for motor control. Based on APM32F035, this design provides a dual-resistance sampling vector control scheme and uses the closed-loop sliding-mode observer estimation scheme. The detailed design specifications are shown in the table below:

Table 1 Design Specifications

Control mode	Sensorless Field Oriented Control (FOC)	
Observer	Back electromotive force observer	
PWM modulation mode	SVPWM	
PWM frequency	8KHz	
Motor speed	100~1000RPM (5 pairs of poles)	
Starting mode	Open-loop starting	
Protection function	Overvoltage, undervoltage, overcurrent, locked rotor	
Code size	11Kbytes	
Development software	Keil C (V5.23 version and above)	

## 1.2 APM32F035 Chip Resources

APM32F035 is a high-performance special MCU for motor control which is based on the Arm Cortex-M0+ core, integrates the mathematical operation accelerators (Cordic, Svpwm, hardware divider, etc.) commonly used in FOC algorithms, and integrates such analog peripherals as amplifiers and comparators, as well as CAN controllers.

Table 2 Functions and Peripherals of APM32F035 Series Chip

Product		APM3	2F035
Mod	el	C8T7	K8T7
Packa	age	LQFP48	LQFP32
Core and maximum	working frequency	Arm® 32-bit Cortex®-M0+@72MHz	
МОСР Со-р	M0CP Co-processor		
Flash memory (KB)		64	
SRAM(KB)		10	
	32 bit/16 bit universal		2
Timer	16-bit advanced	1	
	16-bit basic	2	



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Product		APM32F	035
Model		C8T7	K8T7
	24-bit counter	1	
	Watchdog (WDT)	2 (1 independent watchdog	+1 window watchdog)
	Real-time clock	1	
	USART	2	
Communication into f	SPI/I2S	1/1	
Communication interface	I2C	1	
	CAN	1	
	Unit	1	
12-bit ADC	External channel	16	12
	Internal channel	3	
Comparator (COMP)		2	
Operational amplifier (OPA)		4	2
GPIOs		42	27
Operating temperature		Ambient temperature:	-40℃ to 105℃
		Junction temperature:	-40℃ to 125℃
Working voltage		2.0~3.6	V



## 2 Hardware Introduction

#### 2.1 Overall Hardware Circuit

The overall hardware system is powered by an external AC power supply, and after control conversion through the corresponding rectifier filter and switching power circuits, it will output stable 5V and 3.3V voltages. Users can use the isolated serial port to send data to set the motor speed. At the same time, when the set speed exceeds the starting threshold, the motor will start running, and when the voltage value is below the threshold, the motor will stop running.

After the motor is started, the APM32F035 processor can obtain the phase currents lu, lv, and lw of three phases through the built-in operational amplifier and corresponding sampling circuit, and convert this data through the coordinate axis to control the torque current and phase of the motor. After the FOC control calculation link, adjust the TMR1 peripheral to output the corresponding three-way complementary PWM waves to control the switching components of the inverter.

The hardware block diagram is shown in the figure.

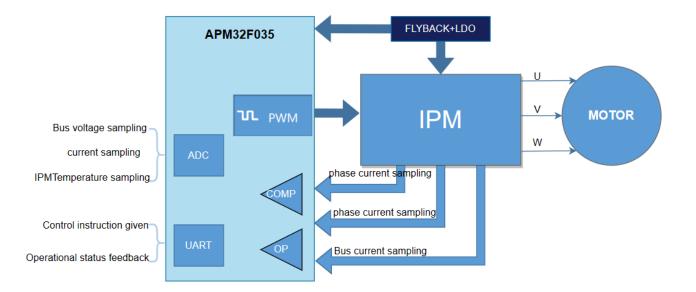


Figure 1 Hardware System Block Diagram



# 2.2 Interface Circuits and Settings

#### 2.2.1 Power circuit

AC 85-264V

Input rectification filtering

Input rectification

Figure 2 Power Circuit

As shown in the figure, the input AC voltage range is 85~264V, which can be stabilized and output stable 5V and 3.3V voltage supply through the rectifier filter circuit and the switching power supply.

switch power supply



## 2.2.2 Bus Voltage Detection Circuit

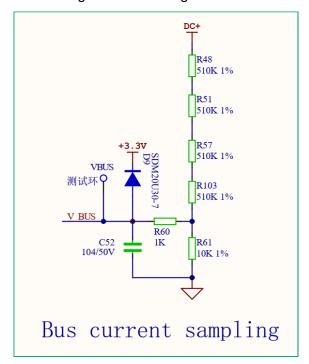


Figure 3 Bus Voltage Detection Circuit

As shown in the figure, the power supply voltage V\_BUS=DC/((510K+510K+510K+510K+10K)/10K)=DC/205

A 12-bit ADC is adopted, and the sampling range 0-3.3V corresponds to 0-4096

Then the maximum sampling voltage corresponding to 3.3V is: DC=3.3 \*205 =676.5V



#### 2.2.3 IPM Circuit

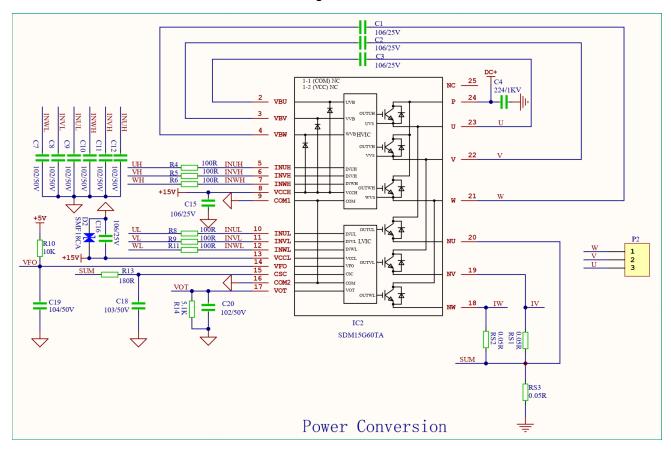


Figure 4 IPM Circuit

As shown in the figure, IPM is used to implement power conversion control, and it also has a protection mechanism. If overcurrent protection occurs, it will be input to the Break In pin of the chip through the VFO port.

#### 2.2.4 Current Sampling Circuit

VREF=1.65V

VO=5\*△Vin+1.65V

VO=5\*△Vin+1.65V

VO=5\*△Vin+1.65V

VREF

R29

R29

R29

R34

R40

PP30

PP30

R44

NC

reference voltage

W—phase current sampling

VO=5\*△Vin+1.65V

Figure 5 Current Sampling Circuit



As shown in the figure, IV=VI\*5+1.65

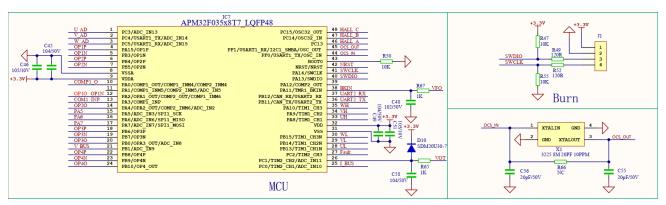
A 12-bit ADC is adopted, and the sampling range 0-3.3V corresponds to 0-4096

As shown in the figure, when the sampling resistance is selected as 0.02R,

the maximum peak-to-peak current corresponding to 3.3V is (3.3-1.65)/5/0.02=16.5A

#### 2.2.5 Minimum system circuit

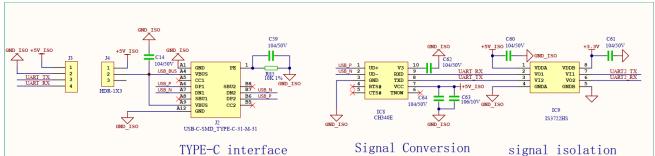
Figure 6 Minimum System Circuit



As shown in the figure, the utilization of APM32F035 MOTOR EVAL V1.0 board hardware interface resources is described in the above figure. The external crystal oscillator input of HSE is 8MHz, and SWD burning interface is adopted for burning.

#### 2.2.6 Communication Interface and Button Circuit

Figure 7 Communication Interface and Button Circuit



As shown in the figure, a USB-to-serial port and a fault indicator light are reserved in the APM32F035 MOTOR EVAL V1.0 board hardware for debugging by developers.

## 2.3 Physical System Hardware

The picture of the system is shown in the figure, and it mainly includes the following five interfaces:



- (1) AC power input interface
- (2) Three phase motor interface (phase sequence only affects the direction of rotation)
- (3) HALL input interface
- (4) SWD debugging interface
- (5) Isolated USB-to-UART interface

Figure 8 Hardware Picture





## 3 Software Introduction

## 3.1 **Overall Program Architecture**

The overall code architecture of this project can be divided into four layers: user layer, peripheral driver layer, motor control driver layer, and motor algorithm layer. The specific functional descriptions are as follows:

#### 3.1.1 USER Layer

main.c: The main function entry is responsible for switching of motor initialization parameters, underlying peripherals, interrupt priority, while cycle, and low-speed state machine loop;

apm32f035\_int.c: All interrupt handling functions, mainly including TMR1 interrupt function and ADC interrupt handler function;

user\_function.c: Includes initialization configuration, parameter reset, and other handler functions of motor parameters;

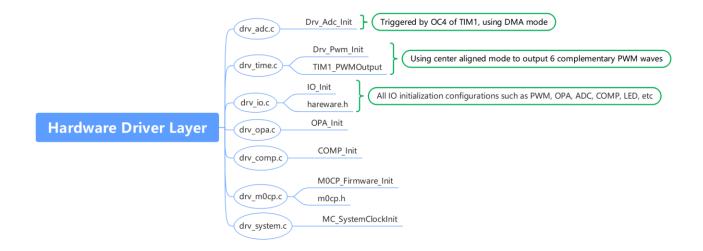
parameter.h: Includes all required configuration parameter information;

board.c: Includes initialization configuration functions of board-level underlying peripheral.

#### 3.1.2 Peripheral Driver Layer (HARDWARE Layer)

The peripheral driver layer is mainly responsible for the peripheral driver functions and configuration of the APM32F035 chip, mainly including GPIO, PWM, ADC, OPA, COMP and M0CP coprocessors, as shown in the following figure.

Figure 9 Peripheral Driver Layer





#### 3.1.3 Motor Control Drive Layer (MOTOR\_CONTROL Layer)

The motor control driver layer is mainly responsible for the control run logic and core processing algorithm call of the motor, as shown in the following figure.

Get ADC Result ADC quantization processing PMSM Obs Observer processing to obtain angle information FOC\_Ctrl.c FOC Current Controller Current loop processing M1\_RunCalibFast M1\_RunReadyFast M1\_RunAlignFast s\_M1\_STATE\_RUN\_TABLE\_FAST M1 RunStartupFast M1\_RunSpinFast M1\_RunFreewheelFast Execution functions of each sub state of the state machine StateMachine.c M1\_RunCalibSlow M1\_RunReadySlow M1\_RunAlignSlow s M1 STATE RUN TABLE SLOW M1\_RunStartupSlow M1 RunSpinSlow M1 RunSpinSlow

Figure 10 Motor Control Driver Layer

#### 3.1.4 Geehy Motor Algorithm Layer (Geehy\_MCLIB Layer)

The motor algorithm layer includes coordinate transformation, vector control and other related functions, as well as math libraries, sliding-mode observer and other library functions.

#### 3.2 Introduction to State Machine

In this case, the structure of embedding the sub-state machine into the main state machine is adopted, as shown below:

Four main states: INIT, STOP, FAIL, and RUN;

The six RUN sub-states of the main state are run calib, run-ready, run-align, run-startup, run-spin, and run-freewheel.

The main state machine is described below:

**Fault:** When an error occurs in the system, it will remain in this state until the error flag bit is cleared.

Then after delay for a period of time, it will jump from the Fault state to the STOP state and wait for the start command.

Init: This main state executes variable initialization.

**Stop:** The system waits for the speed command after completing initialization. In this state, the PWM output is turned off.

**Run:** In the running state, if a Stop command is issued, the system will stop running. www.geehy.com

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When the system is running in the Run state, its sub-states will be called and executed:

**Run-Calib:** The current biased ADC self-calibration function can be executed. After this state is executed, the system will switch to the Ready state and disable the PWM output.

**Ready:** Enable PWM output, synchronously sample the current, and conduct abnormal state inspection.

**Align:** Execute sampling current, call pre-positioning algorithm, and update the PWM. Execute the state within the specified time, and the system will switch to the Startup sub-state and sample the DC bus voltage for filtering.

**Startup:** Sample the current, use an open-loop starting motor, and call the observer to estimate the rotor speed and position, call the corresponding algorithm, and update the PWM. If the motor is started successfully, the system will spin the sub-state and sample the DC bus voltage for filtering.

**Spin:** Sample the current, call the observer to estimate the rotor speed and position, call the corresponding algorithm, update the PWM, and the motor starts to switch to closed-loop operation.

**Freewheel:** Enable PWM output and stop the machine through shorting the brake. Due to rotor inertia, the state can be switched only after the motor stops running and further switched to Ready state. If an error occurs, the system will enter the Fault state.

To sum up, the state machine flowchart of the system is shown in the figure below.

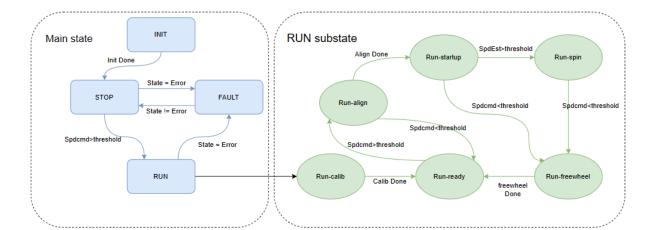


Figure 11 State Machine Flowchart



## 3.3 Top-layer Peripheral Configuration

#### 3.3.1 PWM Output Configuration

void Drv\_Pwm\_Init(uint16\_t u16\_Period,uint16\_t u16\_DeadTime)

1. The general configuration of PWM is as follows:

Set the PWM clock frequency division to 1, select the center-aligned mode 2, and set the repeat counter to 1, as shown in the figure below.

Figure 12 General Configuration of PWM

Figure 13 Center-aligned Mode Selection

Center-Aligned-Mode-Select -

In the Center-aligned mode, the counter counts up and down alternately; otherwise, it will only count up or down. Different Center-aligned modes affect the timing of setting the output comparison interrupt flag bit of the output channel to 1; when the counter is disabled (CNTEN=0), select the Center-aligned mode.

- 01: Center-aligned mode 1 (the output comparison interrupt flag bit of output channel is set to 1 when counting down). □
- 10: Center-aligned mode 2 (the output comparison interrupt flag bit of output channel is set to 1 when counting up) ₽
- 11: Center-aligned mode 3 (the output comparison interrupt flag bit of output channel is set to 1 when counting up/down)

#### 2. PWM output status configuration

Set the output status of upper and lower tubes of PWM and enable the configuration of PWM output of the upper and lower tubes to be effective,

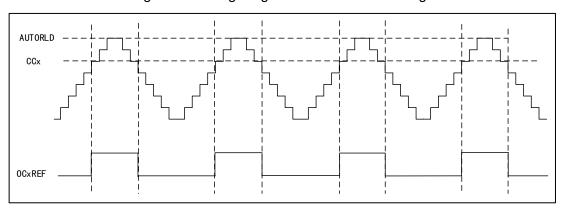
Configure the enabled brakes, configure the brake input polarity, and disable automatic recovery of brake hardware;



#### Figure 14 PWM Output Status Configuration

```
·/* Automatic Output enable, Break, dead time and lock configuration*/
TIM BDTRInitStructure.RMOS State TMR RMOS STATE ENABLE;
TIM BDTRInitStructure.IMOS_State ---- = TMR_IMOS_STATE_ENABLE;
TIM BDTRInitStructure.lockLevel .... TMR LOCK LEVEL OFF;
TIM BDTRInitStructure.deadTime .... = ul6 DeadTime;//
· * Brake configuration: enable brake
* * Brake input polarity: active in low level · · ·
· * · Auto · output · enable · configuration: · Disable · MOE · bit · hardware · control
TIM BDTRInitStructure.breakState --- TMR BREAK STATE ENABLE;
TIM BDTRInitStructure.breakPolarity - TMR BREAK POLARITY LOW;
TIM BDTRInitStructure.automaticOutput = TMR AUTOMATIC OUTPUT DISABLE;
TMR ConfigBDT (TMR1, &TIM BDTRInitStructure);
/*pwm driver set, channel 1,2,3,4set pwm mode*/
TIM OCInitStructure.OC Mode .... = TMR OC MODE PWM2;
TIM OCInitStructure.OC OutputState = TMR OUTPUT STATE ENABLE;
                                                                 //TMR OUTPUT STATE DISABLE;
TIM OCInitStructure OC OutputNState = TMR OUTPUT NSTATE ENABLE; //TMR OUTPUT NSTATE DISABLE;
TIM OCInitStructure.Pulse · · · · · · = · 0;
TIM_OCInitStructure.OC_Polarity ---- = TMR_OC_POLARITY_HIGH;
TIM_OCInitStructure.OC_NPolarity ---- TMR_OC_NPOLARITY_HIGH;
TIM_OCInitStructure.OC_Idlestate · · · = TMR_OCIDLESTATE_RESET; · // · TMR_OCIDLESTATE_SET; · //
TIM OCInitStructure.OC NIdlestate -= TMR OCNIDLESTATE RESET; // TMR OCNIDLESTATE SET;//
```

Figure 15 Timing Diagram of PWM2 Center-aligned Mode



In count-up mode, when TMR1\_CNT<TMR1\_CCR1, Channel 1 is invalid level; otherwise it is valid level;

In count-down mode, when TMR1\_CNT>TMR1\_CCR1, Channel 1 is valid level; otherwise it is invalid level.

#### 3.3.2 ADC Configuration

void Drv Adc Init(void)

#### (1) ADC underlying configuration

DMA mode is adopted, and the quantized data of ADC is directly transported to the ADC\_ConvertedValue array for storage. The ADC trigger condition uses CC4 of TMR1 as the trigger source, to enable ADC and configure ADC interrupt priority and its enable. Details are



shown below:

Figure 16 ADC Underlying Configuration

```
void Drv_Adc_Init(void)
   ADC_Config_T ADC_InitStructure;
  DMA_Config_T DMA_InitStructure;
  DMA_InitStructure.peripheralAddress = (uint32_t)&(ADC->DATA);/
 DMA_InitStructure.memoryAddress ---- (uint32_t)&ADC_ConvertedValue[0];
DMA InitStructure.direction = DMA DIR PERIPHERAL; //
DMA InitStructure.bufferSize = 4;//TOTAL CHANNEL; //
 DMA_InitStructure.peripheralInc ----- DMA_PERIPHERAL_INC_DISABLE; //
  DMA InitStructure.memoryInc DMA MEMORY INC ENABLE; //DMA MEMORY INC ENABLE;
 DMA InitStructure peripheralDataSize = DMA PERIPHERAL DATASIZE HALFWORD;
 DMA InitStructure.memoryDataSize ---- DMA MEMORY DATASIZE HALFWORD ;
 DMA InitStructure.circular = DMA CIRCULAR ENABLE;
DMA InitStructure.priority = DMA PRIORITY_LEVEL_VERYHIGH;
 DMA_InitStructure.memoryTomemory = DMA_M2M_DISABLE;
 DMA Config(DMA CHANNEL 1, &DMA InitStructure);
 DMA Enable (DMA CHANNEL 1);
 - ADC ClockMode (ADC CLOCK MODE ASYNCLK);
  - ADC ConfigStructInit(&ADC InitStructure);
 ADC InitStructure.convMode - - ADC CONVERSION SINGLE;
  ADC_InitStructure.scanDir = ADC_SCAN_DIR_UPWARD;
ADC_InitStructure.extTrigConvl = ADC_EXT_TRIG_CONV_TRG];
                                                                    // timerl CC4
  ADC_InitStructure.extTrigEdgel = ADC_EXT_TRIG_EDGE_RISING;
  ADC_InitStructure.dataAlign = ADC_DATA_ALIGN_RIGHT;
ADC_InitStructure.resolution = ADC_RESOLUTION_12B;
    ADC_Config(&ADC_InitStructure):
    ADC_ConfigChannel(ADC_CHANNEL_2 | ADC_CHANNEL_8 | ADC_CHANNEL_7 | ADC_CHANNEL_9 , ADC_SAMPLE_TIME_1_5);
    ADC->CFG1 B.OVRMAG = 1;
    ADC EnableInterrupt (ADC INT CS);
   NVIC_EnableIRQ(ADC_COMP_IRQn);
   NVIC_SetPriority(ADC_COMP_IRQn,0);
    ADC DMARequestMode (ADC DMA MODE CIRCULAR);
  ADC_EnableDMA();
ADC_Enable();
   ADC_StartConversion();//
```

#### 3.3.3 OPA and COMP Underlying Configuration

#### (1) OPA underlying configuration

To configure the underlying configuration of OPA, first configure the OPA pin, DISABLE the operational amplifier OPA, configure to use an external resistor network, and then ENABLE it, as shown in the figure below;



Figure 17 OPA Underlying Configuration

#### (2) COMP underlying configuration

COMP is used for overcurrent anomaly detection. To configure the underlying configuration of COMP, first configure the COMP pin, set the COMP output to the BKIN connected to TMR1, set the output reverse, and trigger the BKIN of TMR1 at a low level, as shown in the following figure;

Figure 18 COMP Underlying Configuration

## 3.4 Settings and Configuration Methods of Key Parameters

All parameters in this system are configured in parameter.h of the user layer, mainly including system parameters, related parameters of backplane, related parameters of state machine, and related parameters of motor, as follows:



## 3.4.1 System Parameters

Table 3 System Parameters

Parameter name	Parameter description	Set value
SYS_REFV	Supply voltage of the system	3.3 (V)
SYSCLK_HSE_72MHz	Main frequency of the system	72000000 (Hz)
PWMFREQ	PWM frequency	8000 (Hz)
DEAD_TIME	PWM dead band time	1.0 (µs)
SLOWLOOP_FREQ	Control frequency of slow loop	1000 (Hz)

## 3.4.2 Backplane Hardware Parameters

Table 4 Parameters of Backplane Hardware

Parameter name	Parameter description	Set value
ADC_REFV	ADC reference voltage	3.3 (V)
R_SHUNT	Sampling resistance value	0.02 (Ω)
CURRENT_OPA_GAIN	Amplification factor of	4.86
	operational amplifier	
I MAX	Current standardization	16.46 (A)
I_WAX	reference value	10.40 (A)
UDC MAX	Voltage standardization	676.5 (//)
ODC_WAX	reference value	676.5 (V)

#### 3.4.3 Parameters of State Machine

Table 5 Parameters of State Machine

Parameter name	Parameter description	Set value
STOP TO RUN SPEED	Threshold for speed command of jumping	180 (rpm)
3101 _10_1011_31 EED	from Stop to Run state	100 (Ipili)
STARTUP TO SPIN SPEED	Threshold for actual speed of jumping from	150 (rpm)
STARTOF_TO_SFIN_SFEED	Startup to Spin state	130 (ιριπ)
FREEWHEEL SPEED	Stop after the speed command is below the	30 (rpm)
FREEWHEEL_SPEED	threshold	30 (Ipili)
IQ_ALIGN	IQ command value in Align state	0.25 (A)
STARTUP SPEED RAMP	Slope value of speed command under open	50 (rpm/o)
STAINTOF_SPEED_RAIMP	loop	50 (rpm/s)
SPIN_SPD_INC	Closed-loop slope acceleration	150.0 (rpm/s)



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Parameter name	Parameter description	Set value
SPD_DEC	Closed loop slope deceleration	150.0 (rpm/s)

## 3.4.4 Motor Related Parameters

Table 6 Motor Related Parameters

Parameter name	Parameter description	Set value
Rs	Phase resistance of motor	15.4f (ohm)
Ls	Phase inductance of motor	0.185 (H)
POLEPAIRS	Number of motor pole-pairs	5 (unit)
SPEED_MAX	Speed calibration value	1500 (rpm)
MAX_DUTY	Maximum duty cycle	0.95 (unit)
M1_IQ_KP_Q15	Q-axis current loop KP parameter Q15 format	10000
M1_IQ_KI_Q15	Q-axis current loop KI parameter Q15 format	1000
M1_ID_KP_Q15	D-axis current loop KP parameter Q15 format	10000
M1_ID_KI_Q15	D-axis current loop KI parameter Q15 format	1000
M1_SPEED_KP_Q15	Speed loop KP parameter Q15 format	28383
M1_SPEED_KI_Q15	Speed loop KI parameter Q15 format	300



# 4 Debugging Experience Sharing

## 4.1 Debugging Steps

- (1) First, the parameters of the motor need to be clearly defined, such as phase resistance, phase inductance, and number of pole pairs of the motor, and confirm and modify them according to the parameters in "Motor Related Parameters" of Paramater.h;
- (2) Before powering on the board, check whether the main elements are welded in correct position, and after confirming no abnormality, power on, test and confirm whether various voltages of the system are stable (5V, 2.5V, operational amplifier bias voltage, etc.);
- (3) Based on the completion of the above steps, power on and try to run the motor for test. If the motor can run but the speed is unstable, further adjust the PI parameter of the SPEED LOOP. The PI regulator changes from small to large. Adjust KP first and then add KI;
- (4) If the motor cannot run directly, first use the open-loop operation method to synchronously check whether the current sampling part is normal and check the current range of driving IQ\_Align to ensure that the motor can run in the open loop first, and then synchronously check whether the current tracking response of the current loop is normal. In combination with the open-loop test, confirm the speed threshold parameter of switching from open loop to closed loop of the "STARTUP\_TO\_SPIN\_SPEED", and then ensure that it can run in the closed loop. If there is speed fluctuation, please refer to Step (3) synchronously.

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# 5 Revision History

Table 7 Document Revision History

Date	Revision	Revision History
July 26, 2023	1.0	New
August 14, 2022	1.1	(1) Modified the format
August 14, 2023	1.1	(2) Modified the production information form



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