

RoHS Compliant

4GB DDR3 1.35V SO-DIMM

Industrial / Halogen free

Product Specifications

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Version 1.4



Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan

Tel: +886-2-2267-8000 Fax: +886-2-2267-2261

www.apacer.com

General Description

Apacer **D21.16184N.002** is a 512M x 64 DDR3 SDRAM (Synchronous DRAM) SO-DIMM. This high-density memory module consists of 8 pieces 512M x 8 bits DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM. The module is a 204-pins small-outlined, dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
D21.16184N.002	12.8 GB/sec	1600 Mbps	800 MHz	CL11

Density	Organization	Component	Rank
4GB	512M x 64	512M x8*8	1

Key Parameters

MT/s	DDR3-1066	DDR3-1333	DDR3-1600	Unit
Grade	-CL7	-CL9	-CL11	
tCK (min)	1.875	1.5	1.25	ns
CAS latency	7	9	11	tCK
tRCD (min)	13.125	13.5	13.75	ns
tRP (min)	13.125	13.5	13.75	ns
tRAS (min)	37.5	36	35	ns
tRC (min)	50.625	49.5	48.75	ns
CL-tRCD-tRP	7-7-7	9-9-9	11-11-11	tCK

Specifications:

- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 512 words x 64 bits, 1 rank
- ◆ Integrating 8 pieces of 4G bits DDR3 SDRAM sealed in FBGA
- ◆ Package: 204-pin socket type small outline dual in-line memory module (SO-DIMM)
- ◆ PCB: height 30.0mm, lead pitch 0.6 mm (pin), lead-free (RoHS compliant)
- ◆ Power supply VDD: 1.35V (+0.1V ~ -0.067V)
- ◆ Backward compatible to VDD = VDDQ = 1.5V ± 0.075V
 - Supports DDR3L devices to be backward compatible in 1.5V applications
- ◆ Serial Presence Detect (SPD)
- ◆ Eight Internal banks for concurrent operation (components)
- ◆ Interface: SSTL_13
- ◆ Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- ◆ CAS Latency (CL): 6, 7, 8, 9, 10, 11
- ◆ CAS Write Latency (CWL): 5, 6, 7, 8
- ◆ Supports auto pre-charge option for each burst access
- ◆ Supports auto-refresh/self-refresh
- ◆ Support Industrial Temp (-40°C~95°C)
 - tREFI 7.8us at -40 °C ≤ TCASE ≤ 85°C
 - tREFI 3.9us at 85 °C < TCASE ≤ 95°C
- ◆ PCB: 30μ inch gold finger
- ◆ Halogen free

Features:

- ◆ Double-data-rate architecture: 2 data transfers per clock cycle
- ◆ The high-speed data transfer is realized by the 8-bits prefetch pipelined architecture.
- ◆ Bi-directional differential data strobe (DQS and /DQS) is transmitted / received with data for capturing data at the receiver
- ◆ DQS: edge-aligned with data for read; center-aligned with data for write
- ◆ Differential clock inputs (CK and /CK)
- ◆ DLL aligns DQ and DQS transitions with CK transitions
- ◆ Data mask (DM) for writing data
- ◆ Posted CAS by programmable additive latency for enhanced command and data bus efficiency
- ◆ On-Die-Termination (ODT) for improved signal quality: Synchronous ODT/Dynamic ODT/Asynchronous ODT
- ◆ Multi-Purpose Register (MPR) for temperature read out
- ◆ ZQ calibration for DQ drive and ODT
- ◆ Programmable Partial Array Self-Refresh (PASR)
- ◆ /Reset pin for power-up sequence and reset function
- ◆ SRT range: normal/extended, auto/manual self-refresh
- ◆ Programmable output driver impedance control

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.

Tel: +886-2-2267-8000

Fax: +886-2-2267-2261

amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.

46732 Lakeview Blvd., Fremont, CA 94538

Tel: 1-408-518-8699

Fax: 1-510-249-9568

sa@apacerus.com

Japan

Apacer Technology Corp.

5F, Matsura Bldg., Shiba, Minato-Ku

Tokyo, 105-0014, Japan

Tel: 81-3-5419-2668

Fax: 81-3-5419-0018

jpservices@apacer.com

Europe

Apacer Technology B.V.

Science Park Eindhoven 5051 5692 EB Son,
The Netherlands

Tel: 31-40-267-0000

Fax: 31-40-290-0686

sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd.

Room D, 22/FL, No.2, Lane 600, Jieyun Plaza,

Tianshan RD, Shanghai, 200051, China

Tel: 86-21-6228-9939

Fax: 86-21-6228-9936

sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd.

1874, South End C Cross, 9th Block Jayanagar,

Bangalore-560069, INDIA.

Tel: 91-80-4152-9061/62

Fax: 91-80-4170-0215

sales_india@apacer.com