PIC16(L)F1825/1829 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F1825/1829 family devices that you have received conform functionally to the current Device Data Sheet (DS40001440**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1825/1829 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1825/1829 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1),(2)		
	DEV<8:0>	Revision ID for Silicon Revision	
		A0	A2
PIC16F1825	10 0111 011	0 0000	0 0010
PIC16LF1825	10 1000 011	0 0000	0 0010
PIC16F1829	10 0111 111	0 0000	0 0010
PIC16LF1829	10 1000 111	0 0000	0 0010

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC12(L)F1822/PIC16(L)F182X Memory Programming Specification"* (DS41390) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions (1)	
				A0	A2
Oscillator	LFINTOSC	1.1	Wake from Sleep.	X	
Oscillator	HFINTOSC Ready/ Stable bit	1.2	Bits remained set to '1' after initial trigger.	X	X
Oscillator	Clock Switching	1.3	Clock switching can cause a single corrupted instruction.	X	
Oscillator	Oscillator Start-up Timer	1.4	OSTS bit remains set.	X	X
Timer1	T1 Gate Toggle mode	2.1	T1 Gate flip-flop does not clear.	X	
ADC	Error Parameters	3.1	Differential and gain error.	X	X
In-Circuit Serial Programming™ (ICSP™)	Low-Voltage Programming	4.1	Bulk Erase not available with LVP.	X	
Clock Switching	OSTS Status Bit	5.1	Remains clear when 4xPLL enabled.	X	X
MSSP (Master Synchronous Serial Port)	Slew Rate	6.1	Slow rate reduction on SSP2.	X	X
Enhanced Universal Synchronous Asynchronous Receiver (EUSART)	Auto-Baud Detect	7.1	Auto-Baud Detect may store incorrect count value in the SPBRG registers.	X	
Enhanced Universal Synchronous Asynchronous Receiver (EUSART)	16-Bit High-Speed Asynchronous mode	7.2	Works improperly at maximum rate.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Oscillator

1.1 LFINTOSC

The device may not wake-up from Sleep mode when the LFINTOSC is selected as the system clock.

Work around

Enable the Fail-Safe Clock Monitor (FSCM) feature before initiating Sleep mode. When the Fail-Safe Clock Monitor (FSCM) feature is enabled before entering Sleep mode, the device will wake from Sleep.

Affected Silicon Revisions

A0	A2						
X							

1.2 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set, they become "stuck", indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

1.3 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

This issue does not affect Two-Speed Start-up or the Fail-Safe Clock Monitor operation.

Work around

When switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired internal oscillator frequency.

When switching from an internal oscillator (INTOSC) to an external oscillator clock source, first switch to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A0	A2						
X							

1.4 Oscillator Start-up Timer

During the Two-Speed Start-up sequence, the Oscillator Start-up Timer is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = `1`), any of the following conditions will result in the Oscillator Start-up Timer failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

2. Module: Timer1

2.1 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A0	A2						
X							

3. Module: ADC

3.1 ADC Differential and Gain Error Parameters

The differential and gain error parameters are as follows:

Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
AD03	EDL	Differential Error	—	—	±1.5	LSb	VREF = 3.0V. Missing codes = 2
AD04	EOFF	Offset Error	—	—	±2	LSb	VREF = 3.0V. At -40°C offset is ±3
AD05	EGN	Gain Error	—	—	±2	LSb	VREF = 3.0V

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

4. Module: In-Circuit Serial Programming™ (ICSP™)

4.1 Bulk Erase Feature not available with Low-Voltage Programming mode

A bulk erase of the program Flash memory or data memory cannot be executed in Low-Voltage Programming mode.

Work around

Method 1: If ICSP Low-Voltage Programming mode is required, use row erases to erase the program memory, as described in the Program/Verify mode section of the Programming Specification. Data memory must be over-written with the desired values.

Method 2: Use ICSP High-Voltage Programming mode if a Bulk Erase is required.

> **Note:** Only the Bulk Erase feature will erase program or data memory if code or data protection is enabled. Method 2 must be used if code or data protection is enabled.

Affected Silicon Revisions

A0	A2						
X							

5. Module: Clock Switching

5.1 OSTS Status Bit

When the 4xPLL is enabled, the Oscillator Start-up Time-out Status (OSTS) bit always remains clear.

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

6. Module: MSSP (Master Synchronous Serial Port)

6.1 Unintentional SPI Slew Rate Reduction on SSP2

This issue is caused when SSP2 is configured for SPI Master mode while SSP1 is set up for I^2C™ Slave/Master mode with the slew rate (SMP) bit set. This limits SPI bit rates and can cause triangle wave output which is proportional to the speed of the clock. It is most noticeable when the SPI clock exceeds 500 kHz. The selected mode in SSP2 does not affect this issue (CKP/CKE bits).

Work around

1. Disable slew rate control on SSP1 by clearing the SMP bit;
2. Select the alternate pin for SSP2 output;
3. Swap the functionality of the modules;
4. Configure SSP2 with a slower SPI clock.

Affected Silicon Revisions

A0	A2						
X	X						

7. Module: Enhanced Universal Synchronous Asynchronous Receiver (EUSART)

7.1 Auto-Baud Detect

When using automatic baud detection (ABDEN), on occasion, an incorrect count value can be stored at the end of auto-baud detection in the SPBRGH:SPBRGL (SPBRG) registers. The SPBRG value may be off by several counts. This condition happens sporadically when the device clock frequency drifts to a frequency where the SPBRG value oscillates between two different values. The issue is present regardless of the baud rate Configuration bit settings.

Work around

When using auto-baud, it is a good practice to always verify the obtained value of SPBRG, to ensure it remains within the application specifications. Two recommended methods are shown below.

For additional auto-baud information, see Technical Brief TB3069*, "Use of Auto-Baud for Reception of LIN Serial Communications Devices: Mid-Range and Enhanced Mid-Range"*.

EXAMPLE 1: METHOD 1 – EUSART AUTO-BAUD DETECT WORK AROUND

In firmware, define default, minimum and maximum auto-baud (SPBRG) values according to the application requirements.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Compare if value is within limits
    SPBRG_16BIT = DEFAULT_BAUD);                     // if out of spec, use DEFAULT_BAUD
}
   •                                                 // if in spec, continue using the
   •                                                 // Auto-Baud value in SPBRG
   •
```


EXAMPLE 2: METHOD 2 – EUSART AUTO-BAUD DETECT WORK AROUND

Similar to Method 1, define default, minimum and maximum auto-baud (SPBRG) values. In firmware, compute a running average of SPBRG. If the new SPBRG value falls outside the minimum or maximum limits, then use the current running average value (Average_Baud), otherwise use the auto-baud SPBRG value and calculate a new running average.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;               // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                    // Default Auto-Baud value
const int TOL = 0x05;                               // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;            // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;            // Maximum Auto-Baud Limit

int Average_Baud;                                   // Define Average_Baud variable
int Integrator;                                     // Define Integrator variable
   •
   •
   •
Average_Baud = DEFAULT_BAUD;                        // Set initial average Baud rate
Integrator = DEFAULT_BAUD*15;                       // The running 16 count average
   •
   •
   •
ABDEN = 1;                                          // Start Auto-Baud
while (ABDEN);                                      // Wait until Auto-Baud completes

Integrator+ = SPBRG_16BIT;
Average_Baud = Integrator/16;
if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                   // Check if value is within limits
    SPBRG_16BIT = Average_Baud;                     // If out of spec, use previous average
}
else                                                // If in spec, calculate the running
{                                                   // average but continue using the
    Integrator+ = SPBRG_16BIT;                      // Auto-Baud value in SPBRG
    Average_Baud = Integrator/16;
    Integrator- = Average_Baud;
}
   •
   •
   •
```

Affected Silicon Revisions

A0	A2						
X							

7.2 16-Bit High-Speed Asynchronous Mode

EUSART provides unexpected operation when the 16-bit High-Speed Asynchronous mode is selected and the Baud Rate Generator Data register values are loaded with zero ('0'). The use of this configuration is not recommended for EUSART communication. The configuration is shown below in the following table:

Configuration Bits			BRG Data Registers	
SYNC	BRG16	BRGH	SPBRGH Value	SPBRGL Value
0	1	1	00000000	00000000

Work around

Ensure that the SPBRGH or the SPBRGL register is loaded with a non-zero value.

Affected Silicon Revisions

A0	A2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001440**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (01/2011)

Initial release of this document.

Rev B Document (11/2011)

Added Module 6, MSSP.

Rev C Document (02/2012)

Updated Table 1; Added Modules 1.3, 1.4, 1.5; Added Module 7, EUSART; Other minor corrections.

Data Sheet Clarifications: Added Module 1, Oscillator.

Rev D Document (11/2012)

Removed Module 1.1, HS Oscillator; Added Silicon Revision A2.

Rev E Document (10/2013)

Added Module 7.2, 16-Bit High-Speed Asynchronous Mode; Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

Printed on recycled paper.

ISBN: 9781620775370

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/20/13