Product Data – Advance Information

FT2232C

3rd Generation Dual USB UART/FIFO I.C.

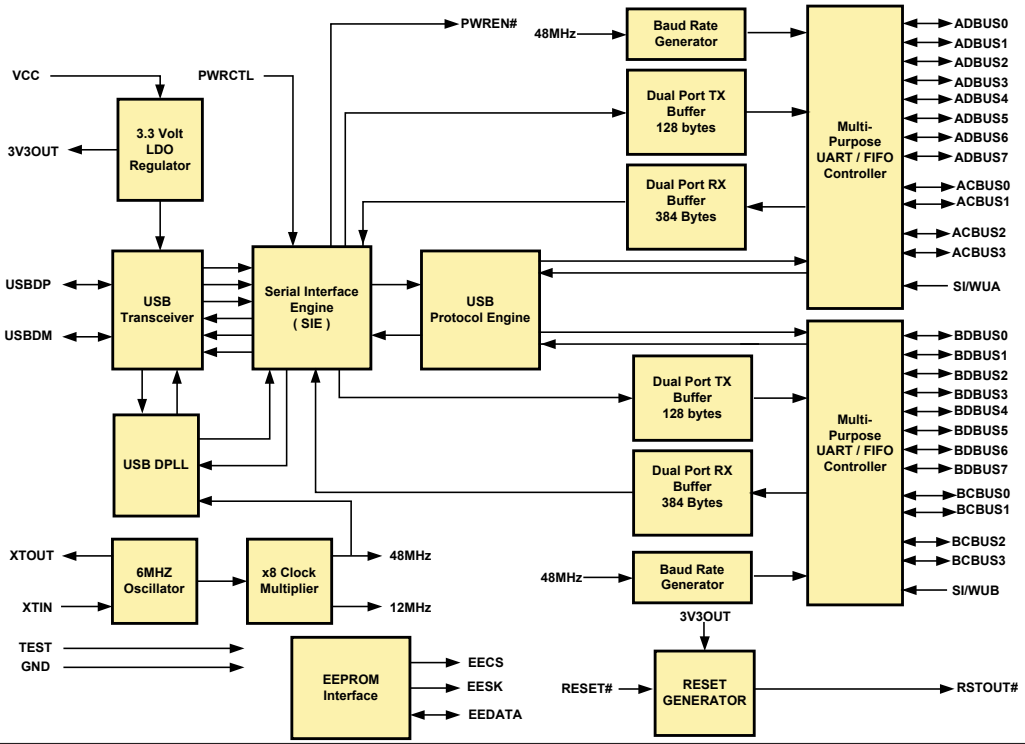
Introduction

FT2232C is the 3rd generation of FTDI USB UART / FIFO family. FT2232C features dual ports, each of which can be configured individually in several different modes. As well as the UART interface, FIFO interface and Bit-Bang IO modes of the second generation FT232BM and FT245BM devices, the FT2232C offers a variety of additional new modes of operation.

Features

- Dual interface with a wide variety of configurations
- FTDI VCP and D2XX drivers for Win 98 / ME / 2000 / XP
- FT232 style UART interface option with full modem handshaking
- Automatic Transmit enable control for RS485 serial applications
- FT245 style FIFO interface option
- Enhanced FT245 style Bit-Bang interface option
- New CPU style FIFO interface option
- New Synchronous Bit-Bang interface option
- New Multi-Protocol Synchronous Serial Engine interface option
- New MCU Host Bus Emulation option
- New Fast Opto-Isolated Serial interface option
- Interface and Description Strings Configurable via external EEPROM
- EEPROM programmable on board via USB
- Power Enable support for USB Suspend / Resume conditions
- Support for bus powered, self powered and high-power bus powered USB configurations
- USB2.0 full speed (12Mbits / sec) compatible
- Independent 5v / 3.3v logic IO interfacing with level translation logic on each channel
- Integrated 3.3v LDO regulator for USB IO
- Integrated 6MHz to 48MHz clock multiplier PLL
- Integrated Power-On Reset with optional Reset input and Reset Output pins
- 4.35 to 5.25 volt single supply operating voltage range
- Compact 48LD LQFP package

FT2232C – Block Diagram (simplified)



FT2232C Enhancements

FT2232C has the following additional modes compared to the 2nd generation FT232BM / FT245BM devices.

Enhanced FT245 style Bit-Bang interface

Internal RD# and WR# strobes are now brought out of the device which allow external logic to be clocked by accesses to the Bit Bang IO Bus

Synchronous Bit-Bang interface

With Synchronous Bit Bang, the device is only read when it is written to as opposed to asynchronously by the data rate generator. This makes it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data.

CPU style FIFO interface

The CPU style FIFO Interface is essentially the same function as the classic FT245 interface, however the bus signals have been re-defined to make them easier to interface to a CPU bus.

Multi-Protocol Synchronous Serial Engine interface

The MPSSE interface is a new option designed to interface efficiently with synchronous serial protocols such as JTAG and SPI bus. It is very flexible in that it can be configured for different industry standard or proprietary bus protocols. It can also be used to program SRAM based FPGA's over USB (see our MORPH-IC evaluation module for a practical example).

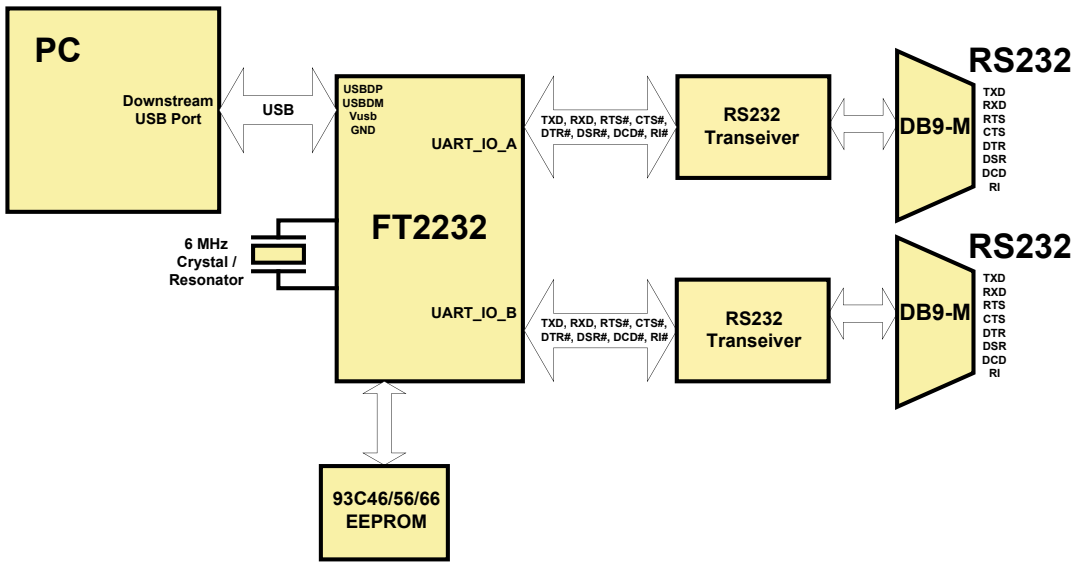
MCU Host Bus Emulation

This new mode combines the "A" and "B" bus interface to make the FT2232C interface emulate a standard 8048/8051 style MCU bus. This allows peripheral devices for these MCU families to be directly attached to the FT2232C with IO being performed over USB with the help of MPSSE technology.

Fast Opto-Isolated Serial interface

A new proprietary FTDI protocol allows galvanically isolated designs to communicate synchronously with the FT2232C using just 4 wires (two dual opto-isolators). The peripheral circuitry controls the data transfer rate in both directions whilst maintaining full data integrity. Maximum USB full speed data rates can be achieved. Both "A" and "B" channels can communicate over the same 4 wire interface if desired.

Application Example – Dual USB to RS232 Converter



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