STM32F302xB STM32F302xC

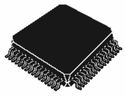
ARM®-based Cortex®-M4 32b MCU+FPU, up to 256KB Flash+ 32KB SRAM, 2 ADCs, 1 DAC ch., 4 comp, 2 PGA, timers, 2.0-3.6 V

Datasheet - production data

Features

- Core: ARM® Cortex®-M4 32-bit CPU with FPU (72 MHz max), single-cycle multiplication and HW division, 63 DMIPS (Dhrystone 2.1) performance at 0 wait state memory access, DSP instruction and MPU (memory protection unit)
- Operating conditions:
  - V_{DD}, V_{DDA} voltage range: 2.0 V to 3.6 V
- Memories
  - 128 to 256 Kbytes of Flash memory
  - Up to 40 Kbytes of SRAM, with HW parity check implemented on the first 16 Kbytes.
- CRC calculation unit
- Reset and supply management
  - Power-on/Power-down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low power modes: Sleep, Stop and Standby
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Up to 87 fast I/Os
  - All mappable on external interrupt vectors
  - Several 5 V-tolerant
- 12-channel DMA controller
- Two ADCs 0.20 µS (up to 39 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, single ended/differential input, separate analog supply from 2 to 3.6 V
- One 12-bit DAC channel with analog supply from 2.4 to 3.6 V
- Four fast rail-to-rail analog comparators with analog supply from 2 to 3.6 V
- Two operational amplifiers that can be used in PGA mode, all terminals accessible with analog supply from 2.4 to 3.6 V
- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touch sensors

LQFP48 (7 × 7 mm)
LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)



- Up to 11 timers
  - One 32-bit timer and two 16-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - One 16-bit 6-channel advanced-control timer, with up to 6 PWM channels, deadtime generation and emergency stop
  - One 16-bit timer with 2 IC/OCs, 1 OCN/PWM, deadtime generation and emergency stop
  - Two 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - Two watchdog timers (independent, window)
  - SysTick timer: 24-bit downcounter
  - One 16-bit basic timer to drive the DAC
- Calendar RTC with Alarm, periodic wakeup from Stop/Standby
- Communication interfaces
  - CAN interface (2.0B Active)
  - Two I^2C Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
  - Up to five USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
  - Up to three SPIs, two with multiplexed half/full duplex I2S interface,4 to 16 programmable bit frames
  - USB 2.0 full speed interface
  - Infrared transmitter
- Serial wire debug, Cortex®-M4 with FPU ETM, JTAG
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F302xB STM32F302xC	STM32F302CB, STM32F302CC, STM32F302RB, STM32F302RC, STM32F302VB, STM32F302VC

Contents

List of tables

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302xB/STM32F302xC microcontrollers.

This STM32F302xB/STM32F302xC datasheet should be read in conjunction with the RM0365 STM32F302x reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 core with FPU, please refer to:

- **Cortex®-M4 with FPU Technical Reference Manual**, available from ARM website www.arm.com.
- **STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214)** available from our website www.st.com.

2 Description

The STM32F302xB/STM32F302xC family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, up to 40 Kbytes of SRAM) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer up to two fast 12-bit ADCs (5 Msps), four comparators, two operational amplifiers, up to one DAC channel, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and one timer dedicated to motor control. They also feature standard and advanced communication interfaces: up to two I^2Cs, up to three SPIs (two SPIs are with multiplexed full-duplex I2Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I2S peripherals can be clocked via an external PLL.

The STM32F302xB/STM32F302xC family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F302xB/STM32F302xC family offers devices in three packages ranging from 48 pins to 100 pins.

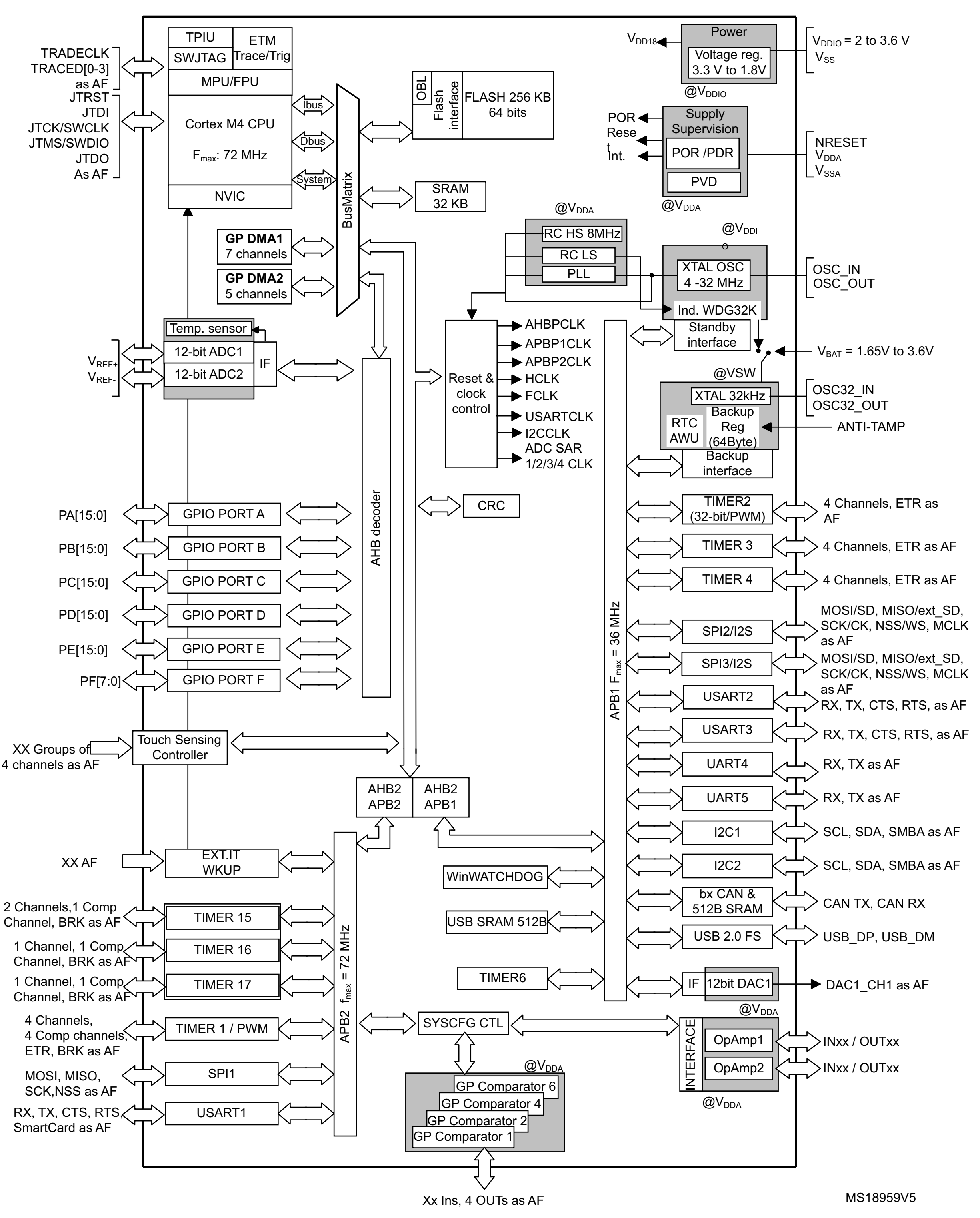
The set of included peripherals changes with the device chosen.

Table 2. STM32F302xx family device features and peripheral counts

Peripheral		STM32F302Cx		STM32F302Rx		STM32F302Vx	
Flash (Kbytes)		128	256	128	256	128	256
SRAM (Kbytes) on data bus		32	40	32	40	32	40
Timers	Advanced control	1 (16-bit)					
	General purpose	5 (16-bit) 1 (32-bit)					
	Basic	1 (16-bit)					
Communication interfaces	SPI(I2S)(1)	3(2)					
	I^2C	2					
	USART	3					
	UART	0		2			
	CAN	1					
	USB	1					
GPIOs	Normal I/Os (TC, TTa)	20		27		45	
	5-volt tolerant I/Os (FT, FTf)	17		25		42	
DMA channels		12					
Capacitive sensing channels		17		18		24	
12-bit ADCs		2					
12-bit DAC channels		1					
Analog comparator		4					
Operational amplifiers		2					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		LQFP48		LQFP64		LQFP100	

1. The SPI interfaces can work in an exclusive way in either the SPI mode or the I^2S audio mode.

Figure 1. STM32F302xB/STM32F302xC block diagram



1. AF: alternate function on I/O pins.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F302xB/STM32F302xC family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F302xB/STM32F302xC family devices.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded Flash memory

All STM32F302xB/STM32F302xC devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Embedded SRAM

STM32F302xB/STM32F302xC devices feature up to 40 Kbytes of embedded SRAM with hardware parity check on first 16 Kbytes of SRAM. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 63 Dhrystone Mips at 72 MHz.

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3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.7 Power management

3.7.1 Power supply schemes

- V_{SS}, V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DAC, comparators operational amplifiers, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the DAC and operational amplifiers are used). The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.7.2 Power supply supervision

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, VPOR/PDR, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.7.4 Low-power modes

The STM32F302xB/STM32F302xC supports three low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.
- Standby mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

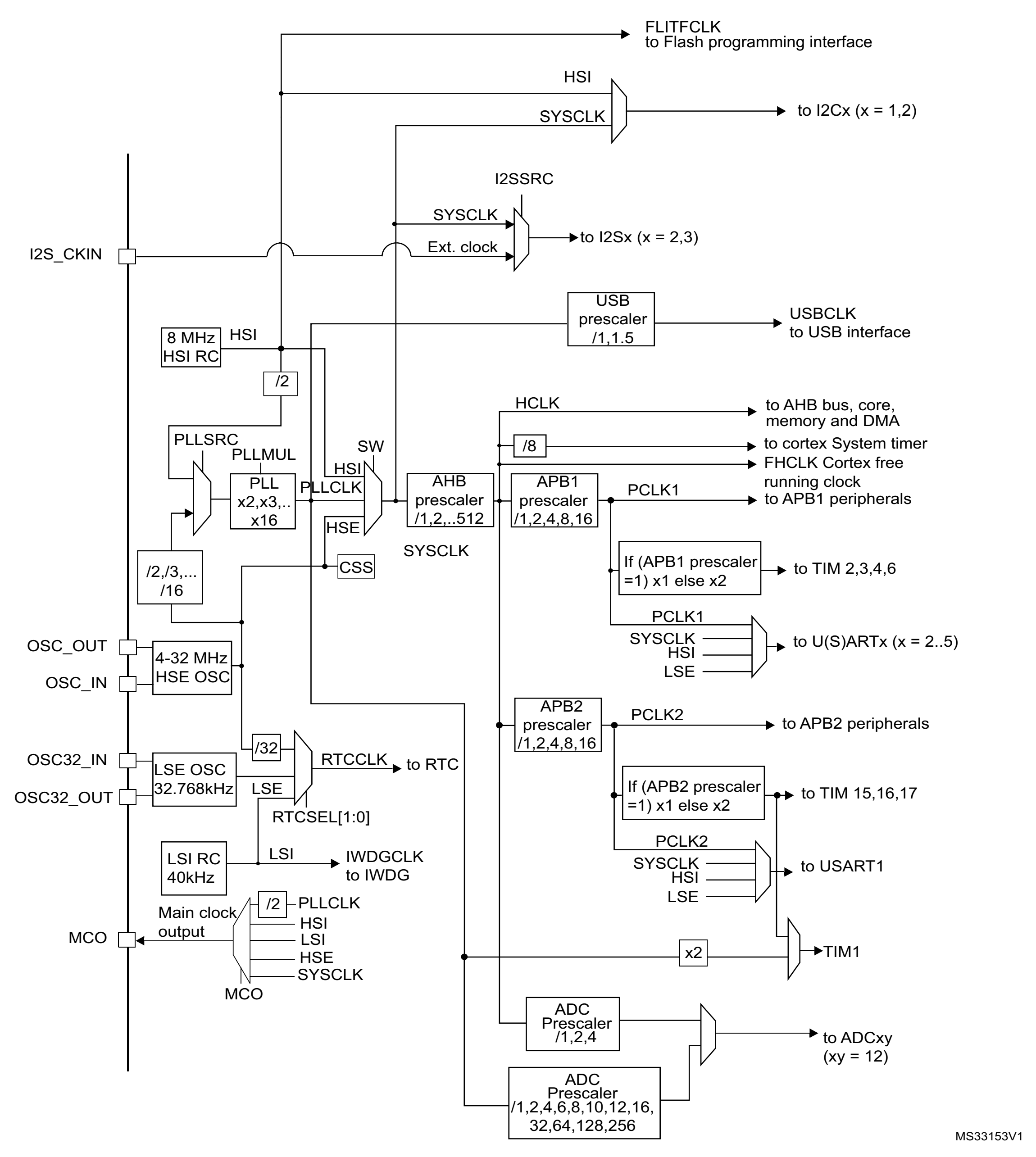
Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

Figure 2. Clock tree



3.9 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.10 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^{2}C, USART, general-purpose timers, DAC and ADC.

3.11 Interrupts and events

3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F302xB/STM32F302xC devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.12 Fast analog-to-digital converter (ADC)

Two fast analog-to-digital converters 5 MSPS, with selectable resolution between 12 and 6 bit, are embedded in the STM32F302xB/STM32F302xC family devices. The ADCs have up to 17 external channels (5 channels multiplexed between ADC1 and ADC2). Channels can be configured to be either single-ended input or differential input. The ADCs can perform conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs have also internal channels: Temperature sensor connected to ADC1 channel 16, $V_{BAT/2}$ connected to ADC1 channel 17, Voltage reference V_{REFINT} connected to the 2 ADCs channel 18, VREFOPAMP1 connected to ADC1 channel 15 and VREFOPAMP2 connected to ADC2 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller. 3 analog watchdogs per ADC are available.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

3.12.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADCx_IN18, x=1...2 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.12.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.12.4 OPAMP reference voltage (VREFOPAMP)

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel: VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17.

3.13 Digital-to-analog converter (DAC)

A single 12-bit buffered DAC channel can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- One DAC output channel
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- External triggers for conversion

3.14 Operational amplifier (OPAMP)

The STM32F302xB/STM32F302xC embeds two operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

3.15 Fast comparators (COMP)

The STM32F302xB/STM32F302xC devices embed four fast rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 26: Embedded internal reference voltage on page 59* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined per pair into a window comparator

3.16 Timers and watchdogs

The STM32F302xB/STM32F302xC includes one advanced control timer, up to six general-purpose timers, one basic timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 3. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
Advanced	TIM1	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.16.1 Advanced timer (TIM1)

The advanced-control timer, TIM1, can be seen as a three-phase PWM multiplexed on six channels. It has a complementary PWM output with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.16.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.16.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xB/STM32F302xC (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

  These are full-featured general-purpose timers:

  - TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler
  - TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  These three timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  - TIM15 has 2 channels and 1 complementary channel
  - TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.16.3 Basic timer (TIM6)

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

3.16.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.16.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.17 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter.It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stopand Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.18 Inter-integrated circuit interface (I^{2}C)

Up to two I^{2}C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 4. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 5* for the features available in I2C1 and I2C2.

Table 5. STM32F302xB/STM32F302xC I^{2}C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X

Table 5. STM32F302xB/STM32F302xC I^2C implementation (continued)

I2C features[1]	I2C1	I2C2
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

3.19 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F302xB/STM32F302xC devices have three embedded universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbits/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

3.20 Universal asynchronous receiver transmitter (UART)

The STM32F302xB/STM32F302xC devices have 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART4 interface can be served by the DMA controller.

Refer to *Table 6* for the features available in all U(S)ART interfaces.

Table 6. USART features

USART modes/features[1]	USART1	USART2	USART3	UART4	UART5
Hardware flow control for modem	X	X	X	-	-
Continuous communication using DMA	X	X	X	X	
Multiprocessor communication	X	X	X	X	X
Synchronous mode	X	X	X	-	-
Smartcard mode	X	X	X	-	-
Single-wire half-duplex communication	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X
LIN mode	X	X	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X	X	X
Receiver timeout interrupt	X	X	X	X	X
Modbus communication	X	X	X	X	X
Auto baud rate detection	X	X	X	-	-
Driver Enable	X	X	X	-	-

1. X = supported.

3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 7* for the features available in SPI1, SPI2 and SPI3.

Table 7. STM32F302xB/STM32F302xC SPI/I2S implementation

SPI features[1]	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	-	X	X
TI mode	X	X	X

1. X = supported.

3.22 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.23 Universal serial bus (USB)

The STM32F302xB/STM32F302xC devices embed an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator). The USB has a dedicated 512-bytes SRAM memory for data transmission and reception.

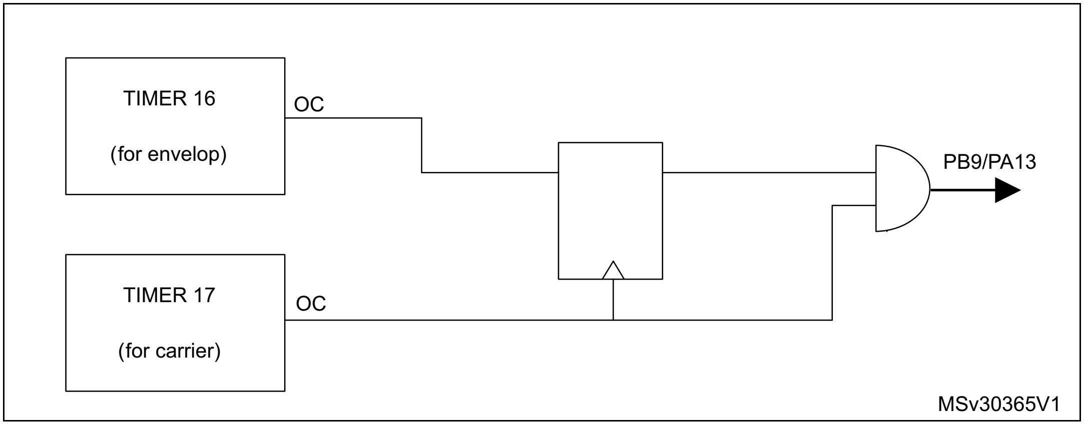
3.24 Infrared Transmitter

The STM32F302xB/STM32F302xC devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.25 Touch sensing controller (TSC)

The STM32F302xB/STM32F302xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 8. Capacitive sensing GPIOs available on STM32F302xB/STM32F302xC devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 9. No. of capacitive sensing channels available on STM32F302xB/STM32F302xC devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F302Vx	STM32F302Rx	STM32F302Cx
G1	3	3	3
G2	3	3	3
G3	3	3	2
G4	3	3	3
G5	3	3	3
G6	3	3	3
G7	3	0	0
G8	3	0	0
Number of capacitive sensing channels	24	18	17

3.26 Development support

3.26.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.26.2 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F302xB/STM32F302xC through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

4 Pinouts and pin description

Figure 4. STM32F302xB/STM32F302xC LQFP48 pinout

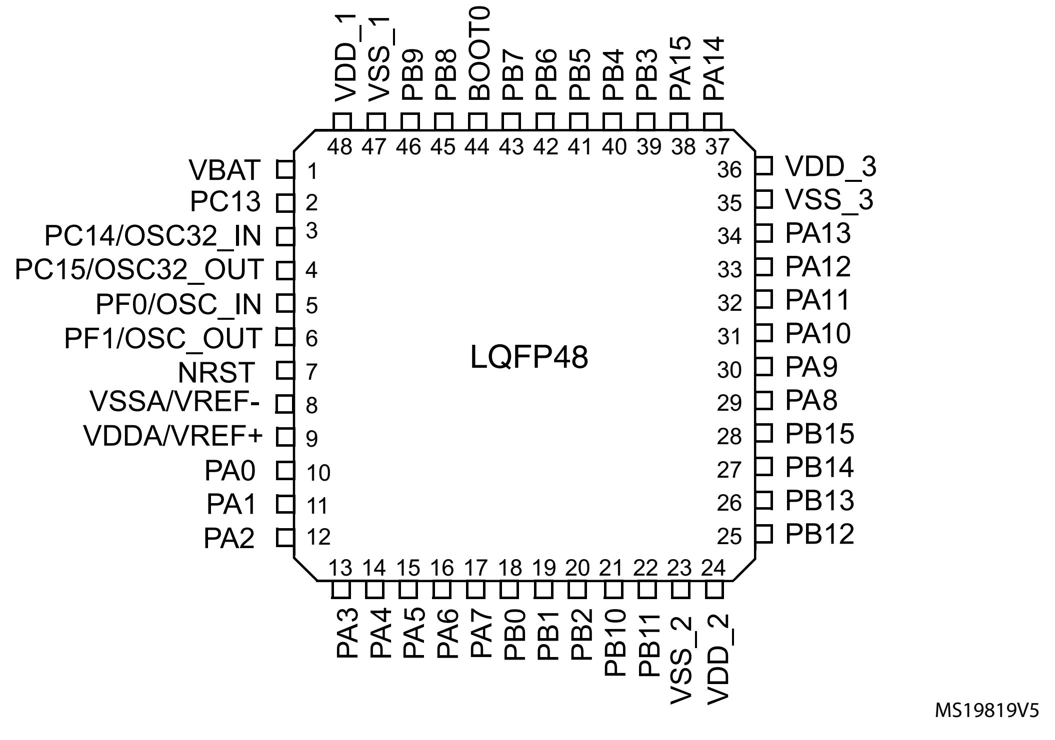


Figure 5. STM32F302xB/STM32F302xC LQFP64 pinout

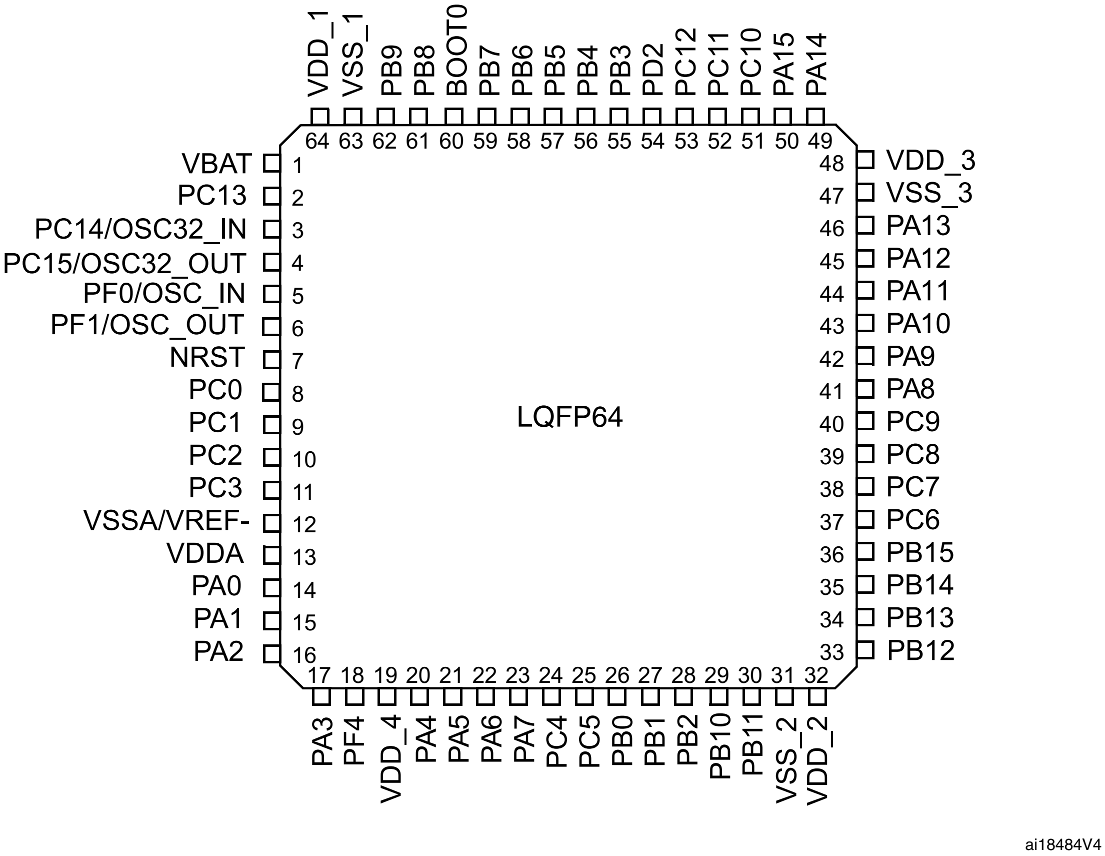


Figure 6. STM32F302xB/STM32F302xC LQFP100 pinout

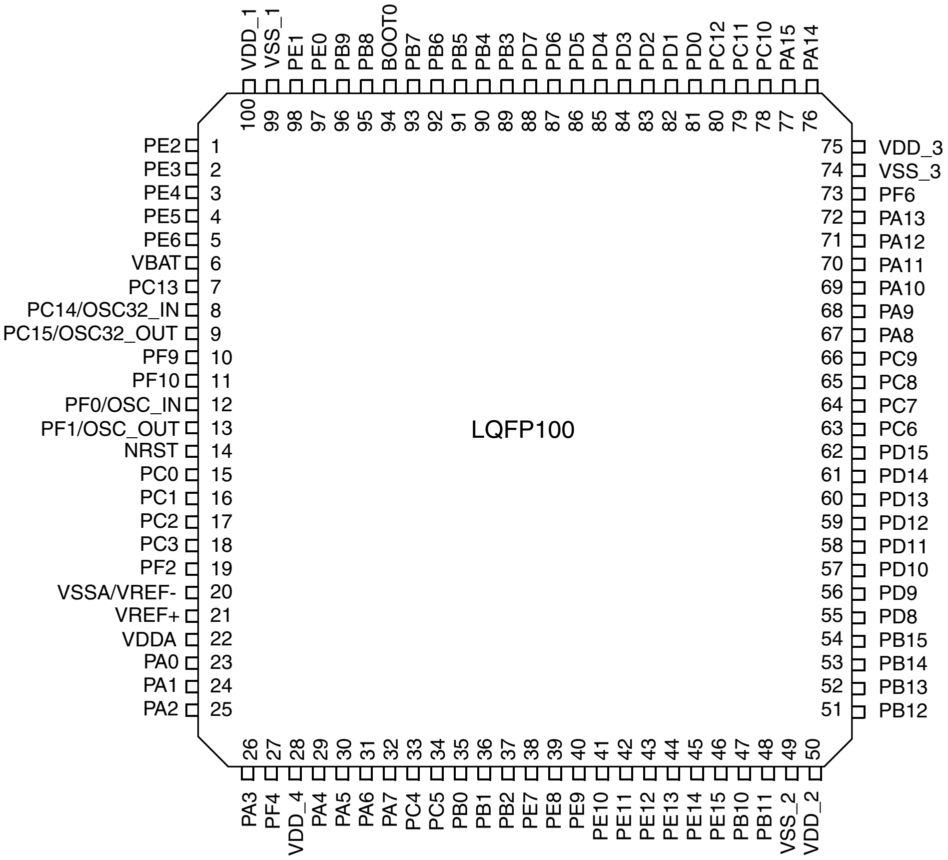


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Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. STM32F302xB/STM32F302xC pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
1	-	-	PE2	I/O	FT	(1)	TRACECK, TIM3_CH1, TSC_G7_IO1, EVENTOUT	-
2	-	-	PE3	I/O	FT	(1)	TRACED0, TIM3_CH2, TSC_G7_IO2, EVENTOUT	-
3	-	-	PE4	I/O	FT	(1)	TRACED1, TIM3_CH3, TSC_G7_IO3, EVENTOUT	-
4	-	-	PE5	I/O	FT	(1)	TRACED2, TIM3_CH4, TSC_G7_IO4, EVENTOUT	-
5	-	-	PE6	I/O	FT	(1)	TRACED3, EVENTOUT	WKUP3, RTC_TAMP3
6	1	1	V_{BAT}	S	-	-	Backup power supply	
7	2	2	PC13(2)	I/O	TC	-	TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
8	3	3	PC14(2) OSC32_IN (PC14)	I/O	TC	-	-	OSC32_IN
9	4	4	PC15(2) OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT
10	-	-	PF9	I/O	FT	(1)	TIM15_CH1, SPI2_SCK, EVENTOUT	-
11	-	-	PF10	I/O	FT	(1)	TIM15_CH2, SPI2_SCK, EVENTOUT	-
12	5	5	PF0-OSC_IN (PF0)	I/O	FTf	-	TIM1_CH3N, I2C2_SDA,	OSC_IN
13	6	6	PF1-OSC_OUT (PF1)	I/O	FTf	-	I2C2_SCL	OSC_OUT
14	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
15	8	-	PC0	I/O	TTa	(1)	EVENTOUT	ADC12_IN6
16	9	-	PC1	I/O	TTa	(1)	EVENTOUT	ADC12_IN7
17	10	-	PC2	I/O	TTa	(1)	EVENTOUT	ADC12_IN8
18	11	-	PC3	I/O	TTa	(1)	TIM1_BKIN2, EVENTOUT	ADC12_IN9
19	-	-	PF2	I/O	TTa	(1)	EVENTOUT	ADC12_IN10
20	12	8	VSSA/ VREF-	S	-	-	Analog ground/Negative reference voltage	
21			VREF+(3)	S	-	-	Positive reference voltage	
22			VDDA	S	-	-	Analog power supply	
-	13	9	VDDA/ VREF+	S	-	-	Analog power supply/Positive reference voltage	

Table 11. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
23	14	10	PA0	I/O	TTa	-	USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, COMP1_OUT, EVENTOUT	ADC1_IN1, COMP1_INM, RTC_ TAMP2, WKUP1
24	15	11	PA1	I/O	TTa	-	USART2_RTS, TIM2_CH2, TSC_G1_IO2, TIM15_CH1N, RTC_REFIN, EVENTOUT	ADC1_IN2, COMP1_INP, OPAMP1_VINP
25	16	12	PA2	I/O	TTa	-	USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3, COMP2_OUT, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT
26	17	13	PA3	I/O	TTa	-	USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4, EVENTOUT	ADC1_IN4, OPAMP1_VINP, COMP2_INP, OPAMP1_VINM
27	18	-	PF4	I/O	TTa	(1)	COMP1_OUT, EVENTOUT	ADC1_IN5
28	19	-	VDD_4	S	-	-	-	-
29	20	14	PA4	I/O	TTa	-	SPI1_NSS, SPI3_NSS, I2S3_WS, USART2_CK, TSC_G2_IO1, TIM3_CH2, EVENTOUT	ADC2_IN1, DAC1_OUT1, COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM
30	21	15	PA5	I/O	TTa	-	SPI1_SCK, TIM2_CH1_ETR, TSC_G2_IO2, EVENTOUT	ADC2_IN2 OPAMP1_VINP, OPAMP2_VINM COMP1_INM, COMP2_INM, COMP4_INM,COMP6_INM
31	22	16	PA6	I/O	TTa	-	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC2_IN3, OPAMP2_VOUT
32	23	17	PA7	I/O	TTa	-	SPI1_MOSI, TIM3_CH2, TIM17_CH1, TIM1_CH1N, TSC_G2_IO4, COMP2_OUT, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP2_VINP, OPAMP1_VINP
33	24		PC4	I/O	TTa	(1)	USART1_TX, EVENTOUT	ADC2_IN5
34	25		PC5	I/O	TTa	(1)	USART1_RX, TSC_G3_IO1, EVENTOUT	ADC2_IN11, OPAMP2_VINM, OPAMP1_VINM
35	26	18	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	COMP4_INPOPAMP2_VINP
36	27	19	PB1	I/O	TTa	-	TIM3_CH4, TIM1_CH3N COMP4_OUT, TSC_G3_IO3, EVENTOUT	-
37	28	20	PB2	I/O	TTa		TSC_G3_IO4, EVENTOUT	ADC2_IN12, COMP4_INM
38	-	-	PE7	I/O	TTa	(1)	TIM1_ETR, EVENTOUT	COMP4_INP
39	-	-	PE8	I/O	TTa	(1)	TIM1_CH1N, EVENTOUT	COMP4_INM
40	-	-	PE9	I/O	TTa	(1)	TIM1_CH1, EVENTOUT	-

Table 11. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
41	-	-	PE10	I/O	TTa	(1)	TIM1_CH2N, EVENTOUT	-
42	-	-	PE11	I/O	TTa	(1)	TIM1_CH2, EVENTOUT	-
43	-	-	PE12	I/O	TTa	(1)	TIM1_CH3N, EVENTOUT	-
44	-	-	PE13	I/O	TTa	(1)	TIM1_CH3, EVENTOUT	-
45	-	-	PE14	I/O	TTa	(1)	TIM1_CH4, TIM1_BKIN2, EVENTOUT	-
46	-	-	PE15	I/O	TTa	(1)	USART3_RX, TIM1_BKIN, EVENTOUT	-
47	29	21	PB10	I/O	TTa	-	USART3_TX, TIM2_CH3, TSC_SYNC, EVENTOUT	-
48	30	22	PB11	I/O	TTa	-	USART3_RX, TIM2_CH4, TSC_G6_IO1, EVENTOUT	COMP6_INP
49	31	23	VSS_2	S	-	-	Digital ground	
50	32	24	VDD_2	S			Digital power supply	
51	33	25	PB12	I/O	TTa	-	SPI2_NSS, I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, TSC_G6_IO2, EVENTOUT	-
52	34	26	PB13	I/O	TTa	-	SPI2_SCK, I2S2_CK, USART3_CTS, TIM1_CH1N, TSC_G6_IO3, EVENTOUT	-
53	35	27	PB14	I/O	TTa	-	SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4, EVENTOUT	OPAMP2_VINP
54	36	28	PB15	I/O	TTa	-	SPI2_MOSI, I2S2_SD, TIM1_CH3N, RTC_REFIN, TIM15_CH1N, TIM15_CH2, EVENTOUT	COMP6_INM
55	-	-	PD8	I/O	TTa	(1)	USART3_TX, EVENTOUT	
56	-	-	PD9	I/O	TTa	(1)	USART3_RX, EVENTOUT	
57	-	-	PD10	I/O	TTa	(1)	USART3_CK, EVENTOUT	COMP6_INM
58	-	-	PD11	I/O	TTa	(1)	USART3_CTS, EVENTOUT	COMP6_INP
59	-	-	PD12	I/O	TTa	(1)	USART3_RTS, TIM4_CH1, TSC_G8_IO1, EVENTOUT	-
60	-	-	PD13	I/O	TTa	(1)	TIM4_CH2, TSC_G8_IO2, EVENTOUT	-
61	-	-	PD14	I/O	TTa	(1)	TIM4_CH3, TSC_G8_IO3, EVENTOUT	OPAMP2_VINP
62	-	-	PD15	I/O	TTa	(1)	SPI2_NSS, TIM4_CH4, TSC_G8_IO4, EVENTOUT	-

Table 11. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
63	37	-	PC6	I/O	FT	(1)	I2S2_MCK,COMP6_OUT TIM3_CH1, EVENTOUT	-
64	38	-	PC7	I/O	FT	(1)	I2S3_MCK, TIM3_CH2, EVENTOUT	-
65	39	-	PC8	I/O	FT	(1)	TIM3_CH3, EVENTOUT	-
66	40	-	PC9	I/O	FT	(1)	TIM3_CH4, I2S_CKIN, EVENTOUT	-
67	41	29	PA8	I/O	FT	-	I2C2_SMBA, I2S2_MCK,USART1_CK, TIM1_CH1, TIM4_ETR, MCO, EVENTOUT	-
68	42	30	PA9	I/O	FTf	-	I2C2_SCL, I2S3_MCK,USART1_TX, TIM1_CH2, TIM2_CH3, TIM15_BKIN, TSC_G4_IO1, EVENTOUT	-
69	43	31	PA10	I/O	FTf	-	I2C2_SDA, USART1_RX, TIM1_CH3, TIM2_CH4, TIM17_BKIN, TSC_G4_IO2, COMP6_OUT, EVENTOUT	-
70	44	32	PA11	I/O	FT	-	USART1_CTS, USB_DM, CAN_RX, TIM1_CH1N, TIM1_CH4, TIM1_BKIN2, TIM4_CH1, COMP1_OUT, EVENTOUT	-
71	45	33	PA12	I/O	FT	-	USART1_RTS, USB_DP, CAN_TX, TIM1_CH2N, TIM1_ETR, TIM4_CH2, TIM16_CH1, COMP2_OUT, EVENTOUT	-
72	46	34	PA13	I/O	FT	-	USART3_CTS, TIM4_CH3, TIM16_CH1N, TSC_G4_IO3, IR_OUT, SWDIO-JTMS, EVENTOUT	-
73	-	-	PF6	I/O	FTf	(1)	I2C2_SCL, USART3_RTS, TIM4_CH4, EVENTOUT	-
74	47	35	VSS_3	S	-	-	Ground	
75	48	36	VDD_3	S	-		Digital power supply	
76	49	37	PA14	I/O	FTf	-	I2C1_SDA, USART2_TXTIM1_BKIN, TSC_G4_IO4, SWCLK-JTCK, EVENTOUT	-

Table 11. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
77	50	38	PA15	I/O	FTf	-	I2C1_SCL, SPI1_NSS, SPI3_NSS, I2S3_WS, JTDI, USART2_RX, TIM1_BKIN, TIM2_CH1_ETR, EVENTOUT	-
78	51	-	PC10	I/O	FT	(1)	SPI3_SCK, I2S3_CK, USART3_TX, UART4_TX, EVENTOUT	-
79	52	-	PC11	I/O	FT	(1)	SPI3_MISO, I2S3ext_SD, USART3_RX, UART4_RX, EVENTOUT	-
80	53	-	PC12	I/O	FT	(1)	SPI3_MOSI, I2S3_SD, USART3_CK, UART5_TX, EVENTOUT	-
81	-	-	PD0	I/O	FT	(1)	CAN_RX, EVENTOUT	-
82	-	-	PD1	I/O	FT	(1)	CAN_TX, EVENTOUT	-
83	54	-	PD2	I/O	FT	(1)	UART5_RX, TIM3_ETR, EVENTOUT	-
84	-	-	PD3	I/O	FT	(1)	USART2_CTS, TIM2_CH1_ETR, EVENTOUT	-
85	-	-	PD4	I/O	FT	(1)	USART2_RTS, TIM2_CH2, EVENTOUT	-
86	-	-	PD5	I/O	FT	(1)	USART2_TX, EVENTOUT	-
87	-	-	PD6	I/O	FT	(1)	USART2_RX, TIM2_CH4, EVENTOUT	-
88	-	-	PD7	I/O	FT	(1)	USART2_CK, TIM2_CH3, EVENTOUT	-
89	55	39	PB3	I/O	FT	-	SPI3_SCK, I2S3_CK, SPI1_SCK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TSC_G5_IO1, JTDO-TRACESWO, EVENTOUT	-
90	56	40	PB4	I/O	FT	-	SPI3_MISO, I2S3ext_SD, SPI1_MISO, USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TSC_G5_IO2, NJTRST, EVENTOUT	-
91	57	41	PB5	I/O	FT	-	SPI3_MOSI, SPI1_MOSI, I2S3_SD, I2C1_SMBA, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1, EVENTOUT	-

Table 11. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
92	58	42	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TIM4_CH1, TSC_G5_IO3EVENTOUT	-
93	59	43	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM3_CH4, TIM4_CH2, TIM17_CH1N, TSC_G5_IO4, EVENTOUT	-
94	60	44	BOOT0	I	B	-	Boot memory selection	
95	61	45	PB8	I/O	FTf	-	I2C1_SCL, CAN_RX, TIM16_CH1, TIM4_CH3 TIM1_BKIN, TSC_SYNC, COMP1_OUT, EVENTOUT	-
96	62	46	PB9	I/O	FTf	-	I2C1_SDA, CAN_TX, TIM17_CH1, TIM4_CH4, IR_OUT, COMP2_OUT, EVENTOUT	-
97	-	-	PE0	I/O	FT	(1)	USART1_TX, TIM4_ETR, TIM16_CH1, EVENTOUT	-
98	-	-	PE1	I/O	FT	(1)	USART1_RX, TIM17_CH1, EVENTOUT	-
99	63	47	VSS_1	S	-	-	Ground	
100	64	48	VDD_1	S	-	-	Digital power supply	

1. Function availability depends on the chosen device.
   When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).

   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0365 reference manual.
3. The VREF+ functionality is available only on the 100 pin package. On the 64-pin and 48-pin packages, the VREF+ is internally connected to VDDA.

Table 12. Alternate functions for port A

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA0	-	TIM2_CH1_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	-	-	-	-	-	EVENTOUT
PA1	RTC_REFIN	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS		TIM15_CH1N	-	-	-	-	EVENTOUT
PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	EVENTOUT
PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	EVENTOUT
PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_CK	-	-	-	-	-	-	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	EVENTOUT
PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	-	SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	-	-	-	-	EVENTOUT
PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	-	SPI1_MOSI	TIM1_CH1N	-	COMP2_OUT	-	-	-	-	-	EVENTOUT
PA8	MCO	-	-	-	I2C2_SMBA	I2S2_MCK	TIM1_CH1	USART1_CK	-	-	TIM4_ETR	-	-	-	EVENTOUT
PA9	-	-	-	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	-	TIM15_BKIN	TIM2_CH3	-	-	-	EVENTOUT
PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	-	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4	-	-	-	EVENTOUT
PA11	-	-	-	-	-	-	TIM1_CH1N	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2	USB_DM	EVENTOUT

Table 12. Alternate functions for port A (continued)

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA12	-	TIM16_CH1	-	-	-	-	TIM1_CH2N	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2	TIM1_ETR	-	USB_DP	EVENTOUT
PA13	SWDIO-JTMS	TIM16_CH1N	-	TSC_G4_IO3	-	IR_OUT	-	USART3_CTS	-	-	TIM4_CH3	-	-	-	EVENTOUT
PA14	SWCLK-JTCK	-	-	TSC_G4_IO4	I2C1_SDA	-	TIM1_BKIN	USART2_TX	-	-	-	-	-	-	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	I2C1_SCL	SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_RX	-	TIM1_BKIN	-	-	-	-	EVENTOUT

Table 13. Alternate functions for port B

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
PB0	-	-	TIM3_ CH3	TSC_ G3_IO2	-	-	TIM1_CH2N	-	-	-	-	-	EVENT OUT
PB1	-	-	TIM3_ CH4	TSC_ G3_IO3	-	-	TIM1_CH3N	-	COMP4_ OUT	-	-	-	EVENT OUT
PB2	-	-	-	TSC_ G3_IO4	-	-	-	-	-	-	-	-	EVENT OUT
PB3	JTDO- TRACES WO	TIM2_ CH2	TIM4_ ETR	TSC_ G5_IO1	-	SPI1_ SCK	SPI3_SCK, I2S3_CK	USART2_ TX	-	-	TIM3_ ETR	-	EVENT OUT
PB4	NJTRST	TIM16_ CH1	TIM3_ CH1	TSC_ G5_IO2	-	SPI1_ MISO	SPI3_MISO, I2S3ext_SD	USART2_ RX	-	-	TIM17_ BKIN	-	EVENT OUT
PB5	-	TIM16_ BKIN	TIM3_ CH2		I2C1_ SMBA	SPI1_ MOSI	SPI3_MOSI, I2S3_SD	USART2_ CK	-	-	TIM17_ CH1	-	EVENT OUT
PB6	-	TIM16_ CH1N	TIM4_ CH1	TSC_ G5_IO3	I2C1_SCL	-	-	USART1_ TX	-	-	-	-	EVENT OUT
PB7	-	TIM17_ CH1N	TIM4_ CH2	TSC_ G5_IO4	I2C1_ SDA	-	-	USART1_ RX	-	-	TIM3_ CH4	-	EVENT OUT
PB8	-	TIM16_ CH1	TIM4_ CH3	TSC_ SYNC	I2C1_SCL	-	-	-	COMP1_ OUT	CAN_RX	-	TIM1_ BKIN	EVENT OUT
PB9	-	TIM17_ CH1	TIM4_ CH4		I2C1_ SDA	-	IR_OUT	-	COMP2_ OUT	CAN_TX	-	-	EVENT OUT
PB10	-	TIM2_ CH3	-	TSC_ SYNC	-	-	-	USART3_ TX	-	-	-	-	EVENT OUT
PB11	-	TIM2_ CH4	-	TSC_ G6_IO1	-	-	-	USART3_ RX	-	-	-	-	EVENT OUT
PB12	-		-	TSC_ G6_IO2	I2C2_ SMBA	SPI2_NSS, I2S2_WS	TIM1_ BKIN	USART3_ CK	-	-	-	-	EVENT OUT

Table 13. Alternate functions for port B (continued)

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
PB13	-	-	-	TSC_ G6_IO3	-	SPI2_SCK, I2S2_CK	TIM1_ CH1N	USART3_ CTS	-	-	-	-	EVENT OUT
PB14	-	TIM15_ CH1	-	TSC_ G6_IO4	-	SPI2_MISO, I2S2ext_SD	TIM1_ CH2N	USART3_ RTS	-	-	-	-	EVENT OUT
PB15	RTC_ REFIN	TIM15_ CH2	TIM15_ CH1N	-	TIM1_ CH3N	SPI2_MOSI, I2S2_SD	-	-	-	-	-	-	EVENT OUT

Table 14. Alternate functions for port C

Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT	-	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-
PC2	EVENTOUT	-	COMP7_OUT	-	-	-	-
PC3	EVENTOUT	-	-	-	-	TIM1_BKIN2	-
PC4	EVENTOUT	-	-	-	-	-	USART1_TX
PC5	EVENTOUT	-	TSC_G3_IO1	-	-	-	USART1_RX
PC6	EVENTOUT	TIM3_CH1	-	-	-	I2S2_MCK	COMP6_OUT
PC7	EVENTOUT	TIM3_CH2	-	-	-	I2S3_MCK	-
PC8	EVENTOUT	TIM3_CH3	-	-	-	-	-
PC9	EVENTOUT	TIM3_CH4	-	-	I2S_CKIN	-	-
PC10	EVENTOUT	-	-	-	UART4_TX	SPI3_SCK, I2S3_CK	USART3_TX
PC11	EVENTOUT	-	-	-	UART4_RX	SPI3_MISO, I2S3ext_SD	USART3_RX
PC12	EVENTOUT	-	-	-	UART5_TX	SPI3_MOSI, I2S3_SD	USART3_CK
PC13	-	-	-	TIM1_CH1N	-	-	-
PC14	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-

Table 15. Alternate functions for port D

Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	-	-	-	-	-	CAN_RX
PD1	EVENTOUT	-	-	-	-	-	CAN_TX
PD2	EVENTOUT	TIM3_ETR	-	-	UART5_RX	-	-
PD3	EVENTOUT	TIM2_CH1_ETR	-	-	-	-	USART2_CTS
PD4	EVENTOUT	TIM2_CH2	-	-	-	-	USART2_RTS
PD5	EVENTOUT	-	-	-	-	-	USART2_TX
PD6	EVENTOUT	TIM2_CH4	-	-	-	-	USART2_RX
PD7	EVENTOUT	TIM2_CH3	-	-	-	-	USART2_CK
PD8	EVENTOUT	-	-	-	-	-	USART3_TX
PD9	EVENTOUT	-	-	-	-	-	USART3_RX
PD10	EVENTOUT	-	-	-	-	-	USART3_CK
PD11	EVENTOUT	-	-	-	-	-	USART3_CTS
PD12	EVENTOUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS
PD13	EVENTOUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-
PD14	EVENTOUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-
PD15	EVENTOUT	TIM4_CH4	TSC_G8_IO4	-	-	SPI2_NSS	-

Table 16. Alternate functions for port E

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF6	AF7
PE0	-	EVENTOUT	TIM4_ETR	-	TIM16_CH1	-	USART1_TX
PE1	-	EVENTOUT	-	-	TIM17_CH1	-	USART1_RX
PE2	TRACECK	EVENTOUT	TIM3_CH1	TSC_G7_IO1	-	-	-
PE3	TRACED0	EVENTOUT	TIM3_CH2	TSC_G7_IO2	-	-	-
PE4	TRACED1	EVENTOUT	TIM3_CH3	TSC_G7_IO3	-	-	-
PE5	TRACED2	EVENTOUT	TIM3_CH4	TSC_G7_IO4	-	-	-
PE6	TRACED3	EVENTOUT		-	-	-	-
PE7	-	EVENTOUT	TIM1_ETR	-	-	-	-
PE8	-	EVENTOUT	TIM1_CH1N	-	-	-	-
PE9	-	EVENTOUT	TIM1_CH1	-	-	-	-
PE10	-	EVENTOUT	TIM1_CH2N	-	-	-	-
PE11	-	EVENTOUT	TIM1_CH2	-	-	-	-
PE12	-	EVENTOUT	TIM1_CH3N	-	-	-	-
PE13	-	EVENTOUT	TIM1_CH3	-	-	-	-
PE14	-	EVENTOUT	TIM1_CH4	-	-	TIM1_BKIN2	-
PE15	-	EVENTOUT	TIM1_BKIN	-	-	-	USART3_RX

Table 17. Alternate functions for port F

Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	I2C2_SDA	-	TIM1_CH3N	-
PF1	-	-	-	I2C2_SCL	-	-	-
PF2	EVENTOUT	-	-	-	-	-	-
PF4	EVENTOUT	COMP1_OUT	-	-	-	-	-
PF6	EVENTOUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS
PF9	EVENTOUT	-	TIM15_CH1	-	SPI2_SCK	-	-
PF10	EVENTOUT	-	TIM15_CH2	-	SPI2_SCK	-	-

5 Memory mapping

Figure 7. STM32F302xB/STM32F302xC memory map

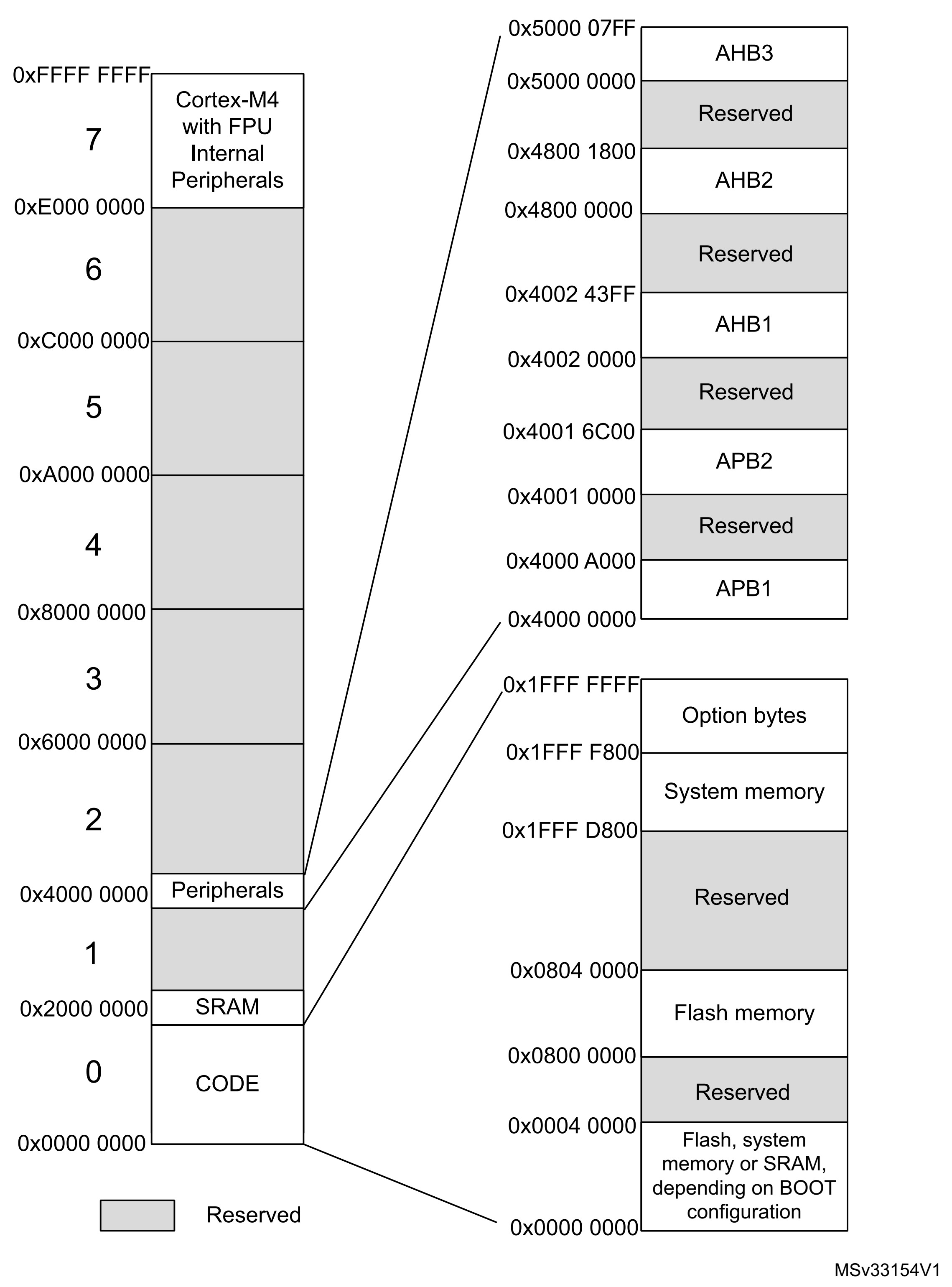


Table 18. STM32F302xB/STM32F302xC memory map and peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
	0x5000 0400 - 0x5000 07FF	1 K	Reserved
AHB3	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0800 - 0x4002 0FFF	2 K	Reserved
	0x4002 0400 - 0x4002 07FF	1 K	DMA2
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 4C00 - 0x4001 7FFF	13 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	Reserved
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP

Table 18. STM32F302xB/STM32F302xC memory map and peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
	0x4000 8000 - 0x4000 FFFF	32 K	Reserved
APB1	0x4000 7800 - 0x4000 7FFF	2 K	Reserved
	0x4000 7400 - 0x4000 77FF	1 K	DAC
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	2 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 6000 - 0x4000 63FF	1 K	USB SRAM 512 bytes
	0x4000 5C00 - 0x4000 5FFF	1 K	USB device FS
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	Reserved
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, $V_{DD} = V_{DDA}$ = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

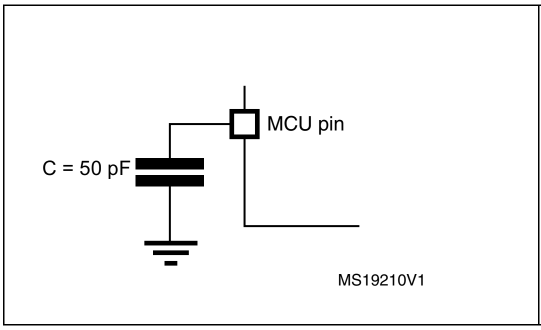
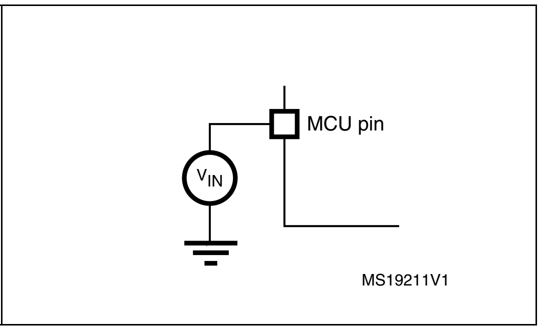
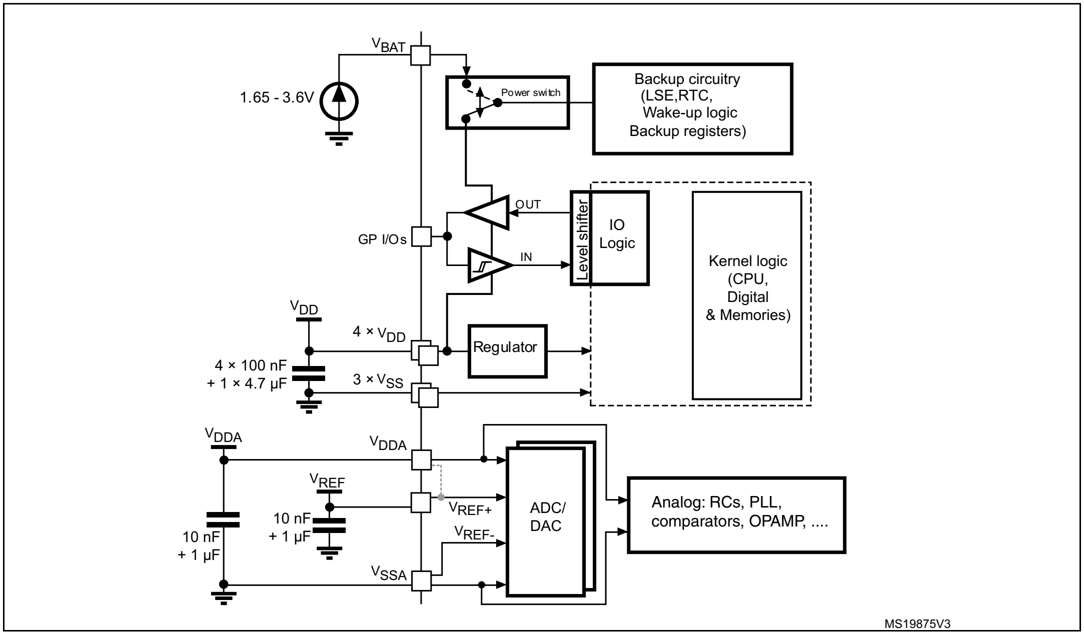


Figure 9. Pin input voltage



6.1.6 Power supply scheme

Figure 10. Power supply scheme

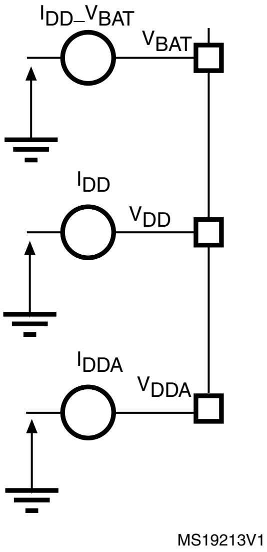


1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA}, V_{BAT} and V_{DD})	-0.3	4.0	V
$V_{DD}–V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
$V_{REF+}–V_{DDA}$(2)	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	
V_{IN}(3)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} –0.3	4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.
2. V_{REF+} must be always lower or equal than V_{DDA} ($V_{REF+} \leq V_{DDA}$). If unused then it must be connected to V_{DDA}.
3. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.

Table 20. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)	160	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)	–160	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	–100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	–25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	–80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 68*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than V_{DD}	2	3.6	V
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.65	3.6	V
V_{IN}	I/O input voltage	TC I/O	–0.3	V_{DD}+0.3	V
		TTa I/O	–0.3	V_{DDA}+0.3	
		FT and FTf I/O(1)	–0.3	5.5	
		BOOT0	0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP100	-	488	mW
		LQFP64	-	444	
		LQFP48	-	364	
TA	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
TJ	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 23. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	POR reset temporization	-	1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 25. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	
		Falling edge	2.56	2.68	2.8	
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
$V_{PVDhyst}$[2]	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	µA

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 26. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.2	1.25	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24(1)	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	2.2	-	-	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10(2)	mV
T_{Coeff}	Temperature coefficient	-	-	-	100(2)	ppm/°C

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Table 27. Internal reference voltage calibration values

Calibration value name	Description	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When f_{HCLK} > 8 MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 28* to *Table 32* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	61.2	65.8	67.6	68.5	27.8	30.3	30.7	31.5	mA
			64 MHz	54.7	59.1	60.2	61.1	24.6	27.2	27.6	28.3	
			48 MHz	41.7	45.1	46.2	47.2	19.2	21.1	21.4	21.8	
			32 MHz	28.1	31.5	32.5	32.7	12.9	14.6	14.8	15.3	
			24 MHz	21.4	23.7	24.4	25.2	10.0	11.4	11.4	12.1	
			8 MHz	7.4	8.4	8.6	9.4	3.6	4.1	4.4	5.0	
			1 MHz	1.3	1.6	1.8	2.6	0.8	1.0	1.2	2.1	
		Internal clock (HSI)	64 MHz	49.7	54.4	55.4	56.3	24.5	27.2	27.4	28.1	
			48 MHz	37.9	42.2	43.0	43.5	18.9	21.4	21.5	21.6	
			32 MHz	25.8	29.2	29.2	30.0	12.7	14.2	14.6	15.2	
			24 MHz	19.7	22.3	22.6	23.2	6.7	7.7	7.9	8.5	
			8 MHz	6.9	7.8	8.3	8.8	3.5	4.0	4.4	5.0	
	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	60.8	66.2(2)	69.7	70.4(2)	27.4	31.7(2)	32.2	32.5(2)	
			64 MHz	54.3	59.1	62.2	63.3	24.3	28.3	28.7	28.8	
			48 MHz	41.0	45.6	47.3	47.9	18.3	21.6	21.9	22.1	
			32 MHz	27.6	32.4	32.4	32.9	12.3	15.0	15.2	15.4	
			24 MHz	20.8	23.9	24.3	25.0	9.3	11.3	11.4	12.0	
			8 MHz	6.9	7.8	8.7	9.0	3.1	3.7	4.2	4.9	
			1 MHz	0.9	1.2	1.5	2.3	0.4	0.6	1.0	1.8	
		Internal clock (HSI)	64 MHz	49.2	53.9	55.2	57.4	23.9	27.8	28.2	28.4	
			48 MHz	37.3	40.8	41.4	44.1	18.2	21.0	21.6	21.9	
			32 MHz	25.1	27.6	29.1	30.1	12.0	14.0	14.5	15.1	
			24 MHz	19.0	21.6	22.1	22.9	6.3	7.2	7.7	8.1	
			8 MHz	6.4	7.3	7.9	8.4	3.0	3.5	4.0	4.7	

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	44.0	48.4	49.4	50.5	6.6	7.5	7.9	8.7	mA
			64 MHz	39.2	43.3	44.0	45.2	6.0	6.8	7.2	7.9	
			48 MHz	29.6	32.7	33.3	34.3	4.5	5.2	5.6	6.3	
			32 MHz	19.7	23.3	23.3	23.5	3.1	3.5	4.0	4.8	
			24 MHz	14.9	17.6	17.8	18.3	2.4	2.8	3.3	3.9	
			8 MHz	4.9	5.7	6.1	6.9	0.8	1.0	1.4	2.2	
			1 MHz	0.6	0.9	1.2	2.1	0.1	0.3	0.6	1.5	
		Internal clock (HSI)	64 MHz	34.2	38.1	39.2	40.3	5.7	6.3	6.8	7.5	
			48 MHz	25.8	28.7	29.6	30.3	4.3	4.8	5.2	5.9	
			32 MHz	17.4	19.4	19.9	20.7	2.9	3.2	3.7	4.5	
			24 MHz	13.2	15.1	15.6	15.9	1.5	1.8	2.2	2.9	
			8 MHz	4.5	5.0	5.6	6.2	0.7	0.9	1.2	2.1	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

Table 29. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run mode, code executing from Flash or RAM	HSE bypass	72 MHz	225	276	289	297	245	302	319	329	µA
			64 MHz	198	249	261	268	216	270	284	293	
			48 MHz	149	195	204	211	159	209	222	230	
			32 MHz	102	145	152	157	110	154	162	169	
			24 MHz	80	119	124	128	86	126	131	135	
			8 MHz	2	3	4	6	3	4	5	9	
			1 MHz	2	3	5	7	3	4	6	9	
		HSI clock	64 MHz	270	323	337	344	299	354	371	381	
			48 MHz	220	269	280	286	244	293	309	318	
			32 MHz	173	218	228	233	193	239	251	257	
			24 MHz	151	194	200	204	169	211	219	225	
			8 MHz	73	97	99	103	88	105	110	116	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.

Table 30. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	20.05	20.33	20.42	20.50	20.67	20.80	44.2(2)	350	735(2)	µA
		Regulator in low-power mode, all oscillators OFF	7.63	7.77	7.90	8.07	8.17	8.33	30.6(2)	335	720(2)	
	Supply current in Standby mode	LSI ON and IWDG ON	0.80	0.96	1.09	1.23	1.37	1.51	-	-	-	
		LSI OFF and IWDG OFF	0.60	0.74	0.83	0.93	1.02	1.11	5.0(2)	7.8	13.3(2)	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 31. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	µA
			Regulator in low-power mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	
	Supply current in Standby mode		LSI ON and IWDG ON	2.22	2.42	2.59	2.78	3.0	3.24	-	-	-	
			LSI OFF and IWDG OFF	1.69	1.82	1.94	2.08	2.23	2.40	3.5	5.4	9.2	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
			Regulator in low-power mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.44	1.52	1.60	1.71	1.84	1.98	-	-	-	
			LSI OFF and IWDG OFF	0.93	0.95	0.98	1.02	1.08	1.15	-	-	-	

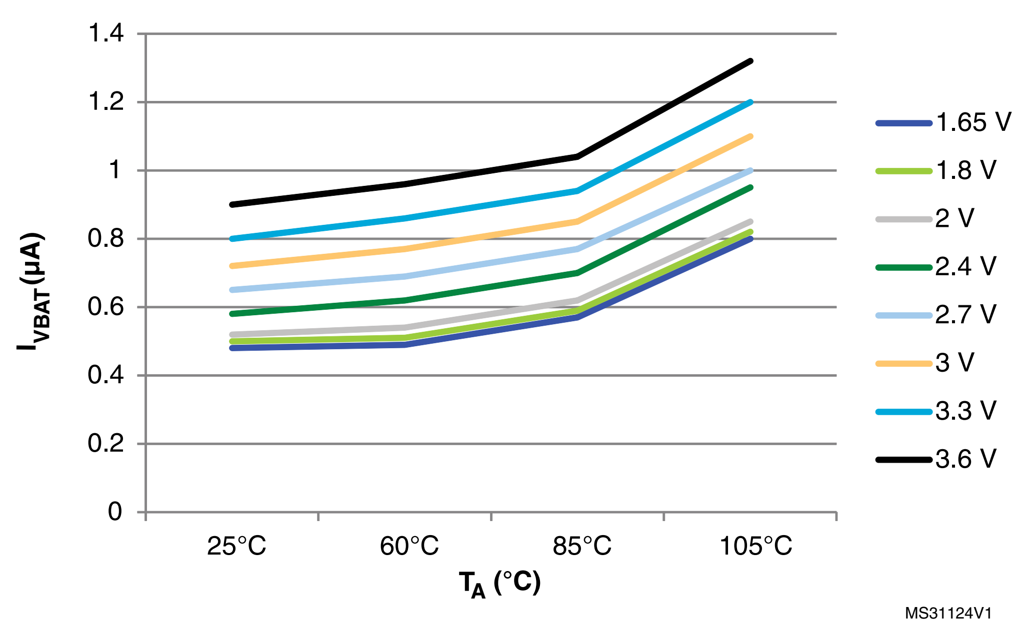
1. Data based on characterization results, not tested in production.

Table 32. Typical and maximum current consumption from V_{BAT} supply

Symbol	Parameter	Conditions (1)	Typ @V_{BAT}								Max @V_{BAT} = 3.6 V(2)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.48	0.50	0.52	0.58	0.65	0.72	0.80	0.90	1.1	1.5	2.0	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.83	0.86	0.90	0.98	1.03	1.10	1.20	1.30	1.5	2.2	2.9	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Data based on characterization results, not tested in production.

Figure 12. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = ’00’)



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	61.3	28.0	mA
			64 MHz	54.8	25.4	
			48 MHz	41.9	19.3	
			32 MHz	28.5	13.3	
			24 MHz	21.8	10.4	
			16 MHz	14.9	7.2	
			8 MHz	7.7	3.9	
			4 MHz	4.5	2.5	
			2 MHz	2.8	1.7	
			1 MHz	1.9	1.3	
			500 kHz	1.4	1.1	
			125 kHz	1.1	0.9	
I_{DDA}(1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	240.3	239.5	µA
			64 MHz	210.9	210.3	
			48 MHz	155.8	155.6	
			32 MHz	105.7	105.6	
			24 MHz	82.1	82.0	
			16 MHz	58.8	58.8	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 34. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	44.1	7.0	mA
			64 MHz	39.7	6.3	
			48 MHz	30.3	4.9	
			32 MHz	20.5	3.5	
			24 MHz	15.4	2.8	
			16 MHz	10.6	2.0	
			8 MHz	5.4	1.1	
			4 MHz	3.2	1.0	
			2 MHz	2.1	0.9	
			1 MHz	1.5	0.8	
			500 kHz	1.2	0.8	
			125 kHz	1.0	0.8	
I_{DDA}(1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.7	238.5	μA
			64 MHz	210.5	209.6	
			48 MHz	155.0	155.6	
			32 MHz	105.3	105.2	
			24 MHz	81.9	81.8	
			16 MHz	58.7	58.6	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 52: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see*Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V.

Table 36. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	12.6	µA/MHz
DMA1	7.6	
DMA2	6.1	
CRC	2.1	
GPIOA	10.0	
GPIOB	10.3	
GPIOC	2.2	
GPIOD	8.8	
GPIOE	3.3	
GPIOF	3.0	
TSC	5.5	
ADC1&2	17.3	
APB2-Bridge (3)	3.6	
SYSCFG	7.3	
TIM1	40.0	
SPI1	8.8	
USART1	23.3	
TIM15	17.1	
TIM16	10.1	
TIM17	11.0	
APB1-Bridge (3)	6.1	
TIM2	49.1	
TIM3	38.8	
TIM4	38.3	

Table 36. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
TIM6	9.7	µA/MHz
WWDG	6.4	
SPI2	40.4	
SPI3	40.0	
USART2	41.9	
USART3	40.2	
UART4	36.5	
UART5	30.8	
I2C1	10.5	
I2C2	10.4	
USB	26.2	
CAN	33.4	
PWR	5.7	
DAC	15.4	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 37* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 37. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @VDD, $V_{DD} = V_{DDA}$						Max	Unit
			2.0 V	**2.4 V**	**2.7 V**	**3 V**	**3.3 V**	**3.6 V**		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.1	3.9	3.8	3.7	3.6	3.5	4.5	µs
		Regulator in low power mode	7.9	6.7	6.1	5.7	5.4	5.2	9	
$t_{WUSTANDBY}$(1)	Wakeup from Standby mode	LSI and IWDG OFF	69.2	60.3	56.4	53.7	51.7	50	100	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	6						-	CPU clock cycles

1. Data based on characterization results, not tested in production.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

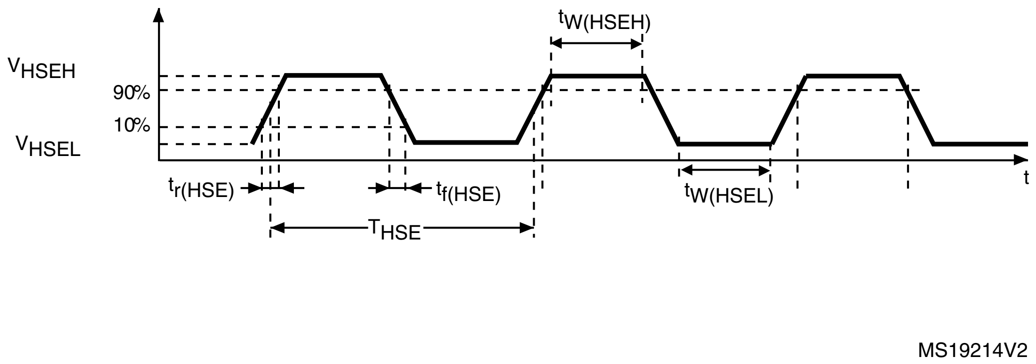
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 38. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency[1]	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time[1]		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time[1]		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 13. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

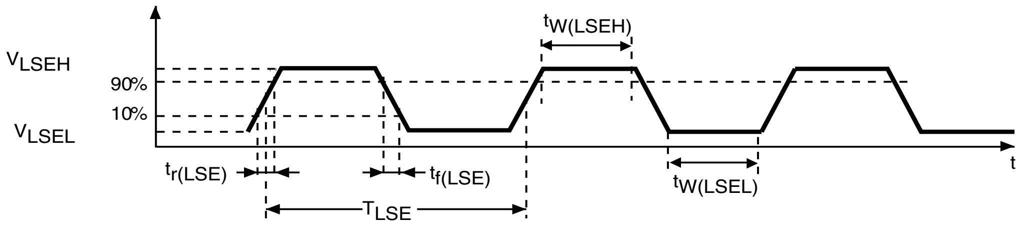
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 14*

Table 39. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency[1]	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time[1]		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time[1]		-	-	50	

1. Guaranteed by design, not tested in production.

Figure 14. Low-speed external clock source AC timing diagram



MS19215V2

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. HSE oscillator characteristics

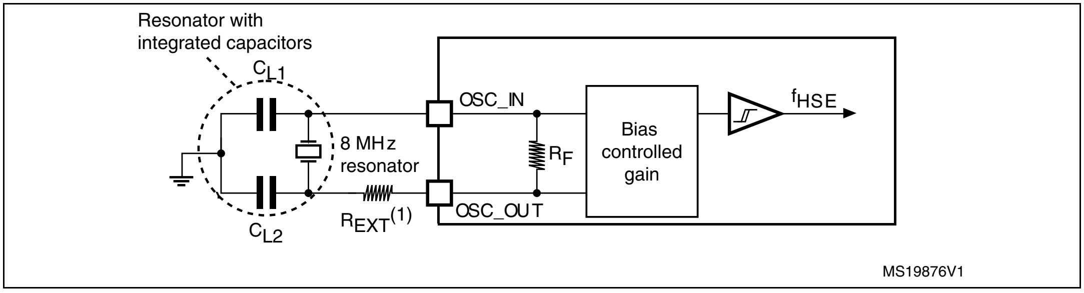
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200		kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD}=3.3 V, Rm= 30Ω, CL=10 pF@8 MHz	-	0.4	-	
		V_{DD}=3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}=3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	0.8	-	
		V_{DD}=3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1	-	
		V_{DD}=3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 15*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 15. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

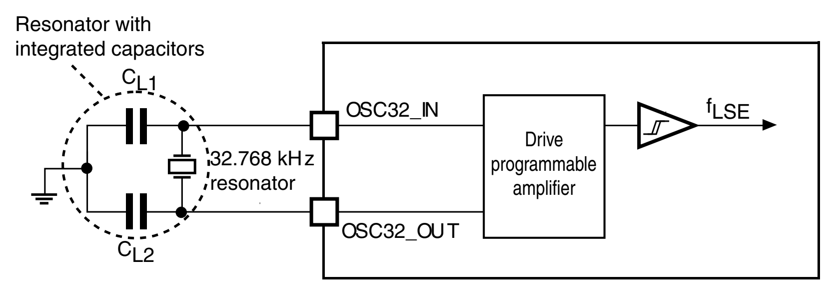
Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]=01 medium low driving capability	-	-	1	
		LSEDRV[1:0]=10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]=01 medium low driving capability	8	-	-	
		LSEDRV[1:0]=10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: *For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

Figure 16. Typical application with a 32.768 kHz crystal



Note: *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

6.3.8 Internal clock source characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

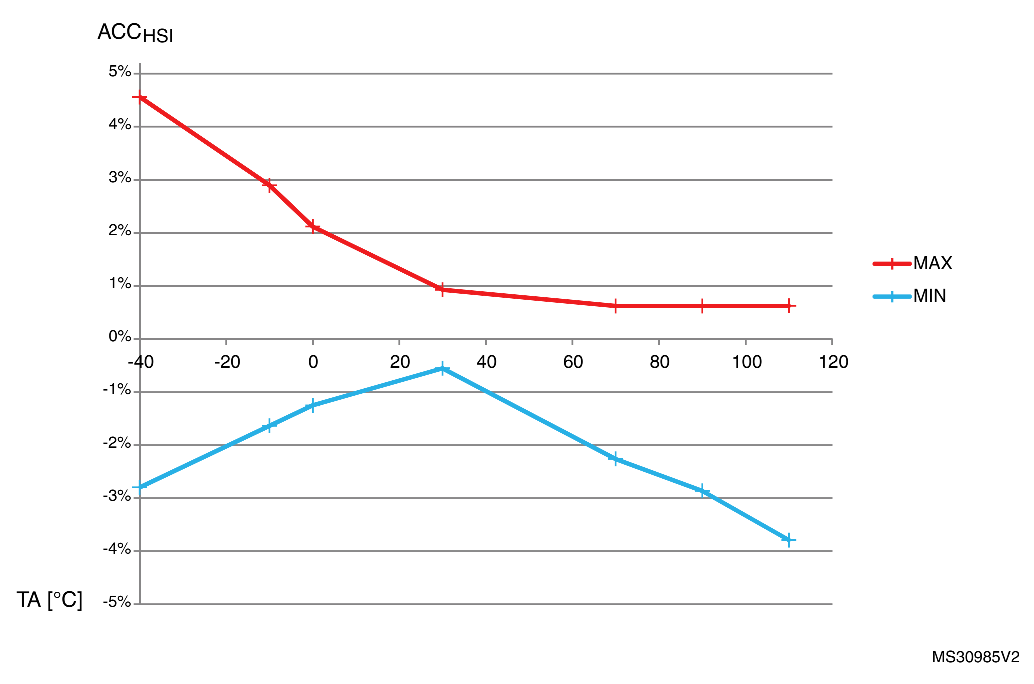
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1[2]	%
$DuCy_{(HSI)}$	Duty cycle	-	45[2]	-	55[2]	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–3.8[3]	-	4.6[3]	%
		T_A = –10 to 85 °C	–2.9[3]	-	2.9[3]	%
		T_A = 0 to 70 °C	-	-	-	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI)}$	HSI oscillator startup time	-	1[2]	-	2[2]	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	100[2]	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 17. HSI oscillator accuracy characterization results



1. The above curves are based on characterisation results, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 44. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 45. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 46. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 47*. They are based on the EMS levels and classes defined in application note AN1709.

Table 47. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 48. EMI characteristics

Symbol	**Parameter**	**Conditions**	**Monitored frequency band**	**Max vs. [f_{HSE}/f_{HCLK}]**	**Unit**
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	**7**	dBµV
			30 to 130 MHz	**20**	
			130 MHz to 1GHz	**27**	
			SAE EMI Level	**4**	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 49. ESD absolute maximum ratings

Symbol	**Ratings**	**Conditions**	**Class**	**Maximum value**[1]	**Unit**
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	II	500	

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 51*.

Table 51. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	– 0	NA	mA
	Injected current on PC0, PC1, PC2, PC3, PF2, PA0, PA1, PA2, PA3, PF4, PA4, PA5, PA6, PA7, PC4, PC5, PB2 with induced leakage current on other pins from this group less than -50 µA	– 5	-	
	Injected current on PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than -50 µA	– 5	-	
	Injected current on PC0, PC1, PC2, PC3, PF2, PA0, PA1, PA2, PA3, PF4, PA4, PA5, PA6, PA7, PC4, PC5, PB2, PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than 400 µA	-	+5	
	Injected current on any other FT and FTf pins	– 5	NA	
	Injected current on any other pins	– 5	+5	

Note: *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant.

Table 52. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DD}+0.07$ (1)	V
		FT and FTf I/O	-	-	$0.475\ V_{DD}-0.2$ (1)	
		BOOT0	-	-	$0.3\ V_{DD}-0.3$ (1)	
		All I/Os except BOOT0	-	-	$0.3\ V_{DD}$ (2)	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DD}+0.398$ (1)	-	-	
		FT and FTf I/O	$0.5\ V_{DD}+0.2$ (1)	-	-	
		BOOT0	$0.2\ V_{DD}+0.95$ (1)	-	-	
		All I/Os except BOOT0	$0.7\ V_{DD}$ (2)	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200 (1)	-	mV
		FT and FTf I/O	-	100 (1)	-	
		BOOT0	-	300 (1)	-	
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	±0.2	
		FT and FTf I/O(4) $V_{DD} \leq V_{IN} \leq 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance		-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. Leakage could be higher than the maximum value. if negative current is injected on adjacent pins. Refer to *Table 51: I/O current injection susceptibility*.
4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 18* and *Figure 19* for standard I/Os.

Figure 18. TC and TTa I/O input characteristics - CMOS port

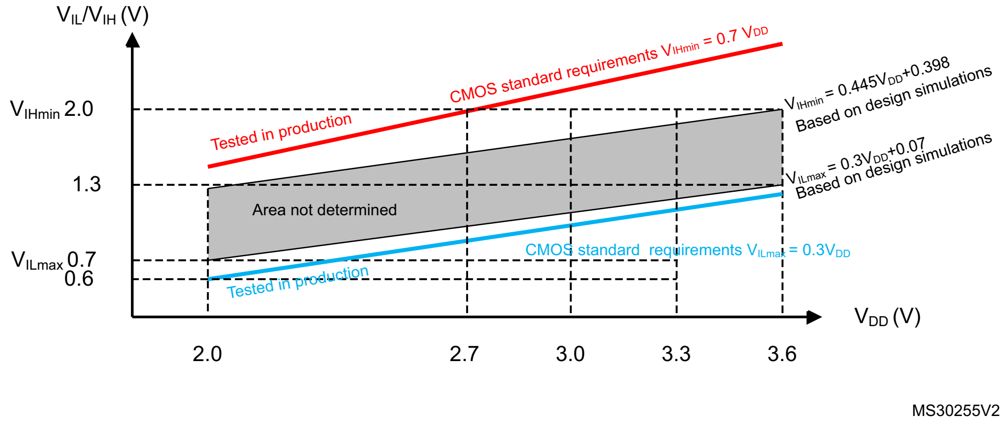


Figure 19. TC and TTa I/O input characteristics - TTL port

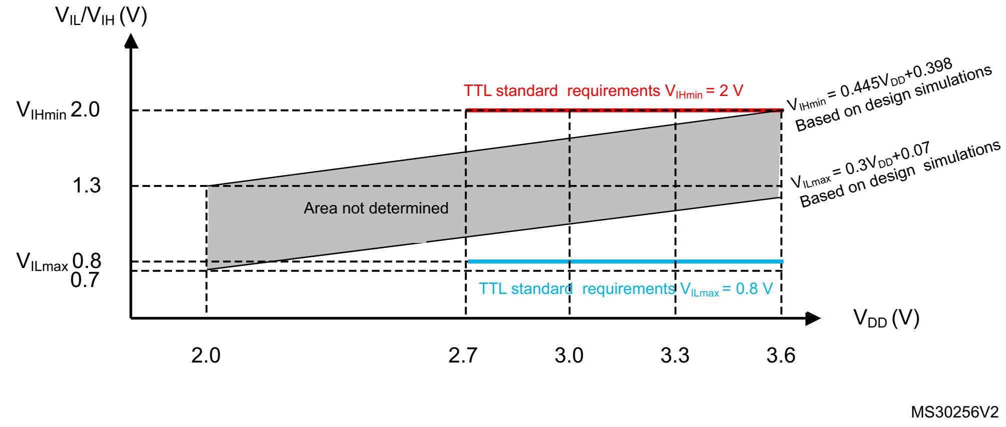


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

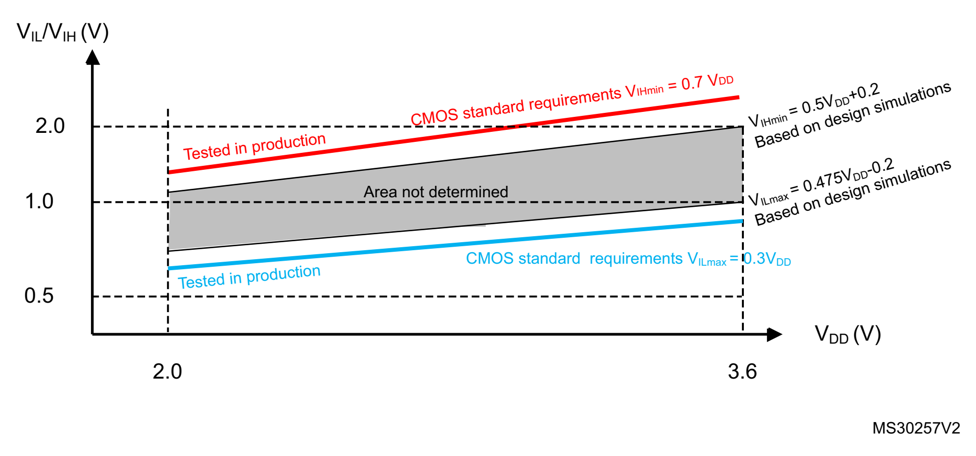
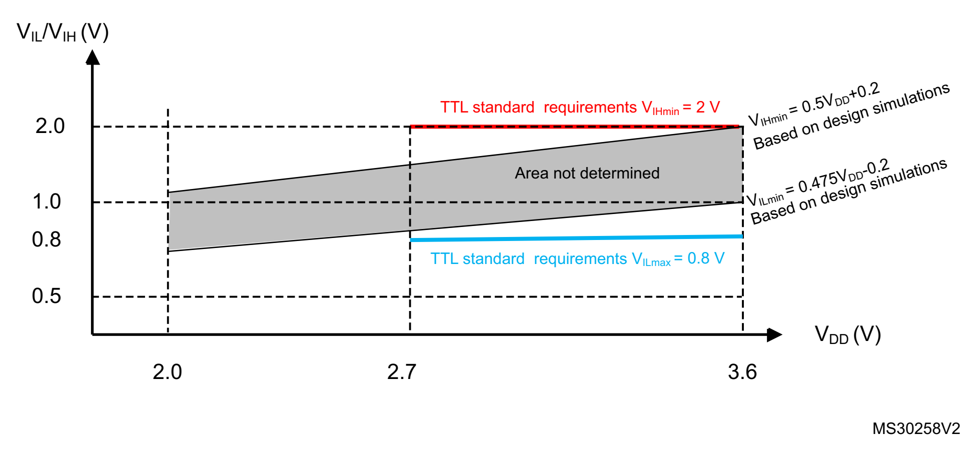


Figure 21. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 20*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 20*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 53. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(1)(4)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 22* and *Table 54*, respectively.

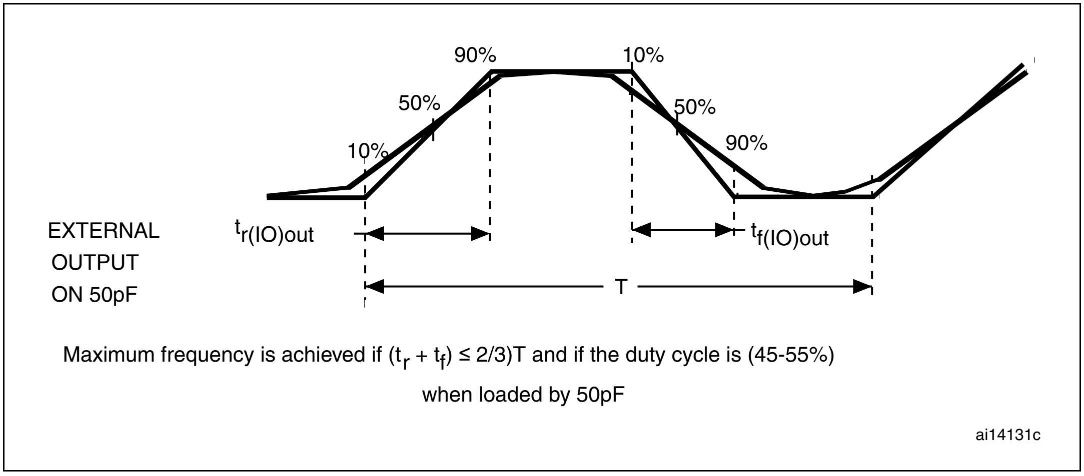
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 54. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50(3)	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30(3)	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(4)	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	12(4)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	34(4)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10(3)	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0365 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 22*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F302x STM32F312x reference manual RM0365 for a description of FM+ I/O mode configuration.

Figure 22. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ 2/3)T and if the duty cycle is (45-55%)

when loaded by 50pF

6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 52*).

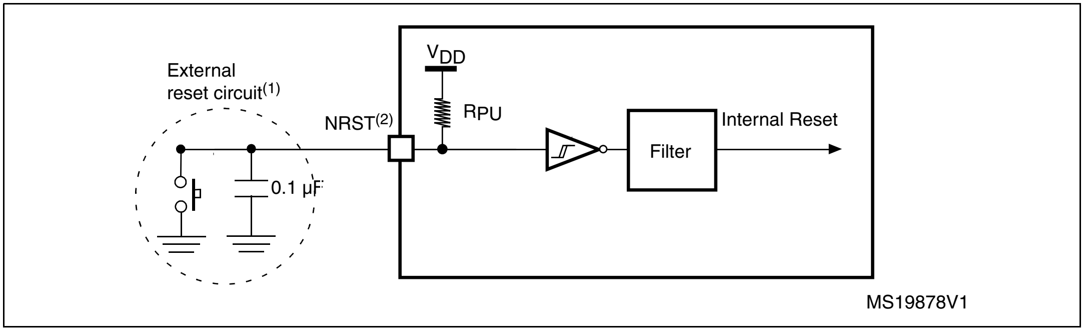
Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 55. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}$+ 0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD}$+ 0.398(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	500(1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 23. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 55*. Otherwise the reset will not be taken into account by the device.

6.3.16 Timer characteristics

The parameters given in *Table 56* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 56. TIMx[(1)(2)] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz (except TIM1)	13.9	-	ns
		$f_{TIM1CLK}$ = 144 MHz	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz (except TIM1)	0.0139	910	µs
		$f_{TIM1CLK}$ = 144 MHz	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIM1CLK}$ = 144 MHz	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

Table 57. IWDG min/max timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 58. WWDG min-max timeout value @72 MHz (PCLK)(1)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.17 Communications interfaces

I^{2}C interface characteristics

The I^{2}C interface meets the timings requirements of the I^{2}C-bus specification and user manual rev.03 for:

- Standard-mode (Sm) : with a bit rate up to 100 Kbits/s
- Fast-mode (Fm) : with a bit rate up to 400 Kbits/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1Mbits/s

The I^{2}C timings requirements are guaranteed by design when the I^{2}C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics*.

All I^{2}C I/Os embed an analog filter. refer to the*Table 60: I2C analog filter characteristics*.

Table 59. I2C timings specification (see I2C specification, rev.03, June 2007)(1)

Symbol	Parameter	Standard mode		Fast mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	μs
t_{HIGH}	High Period of the SCL clock	4		0.6		0.26	-	μs
t_r	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
t_f	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	μs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	μs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD:STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	μs
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26		μs
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	μs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF
t_{SP}	Pulse width of spikes that are suppressed by the analog filter for Standard and Fast mode	0	50(3)	0	50(3)	-	-	ns

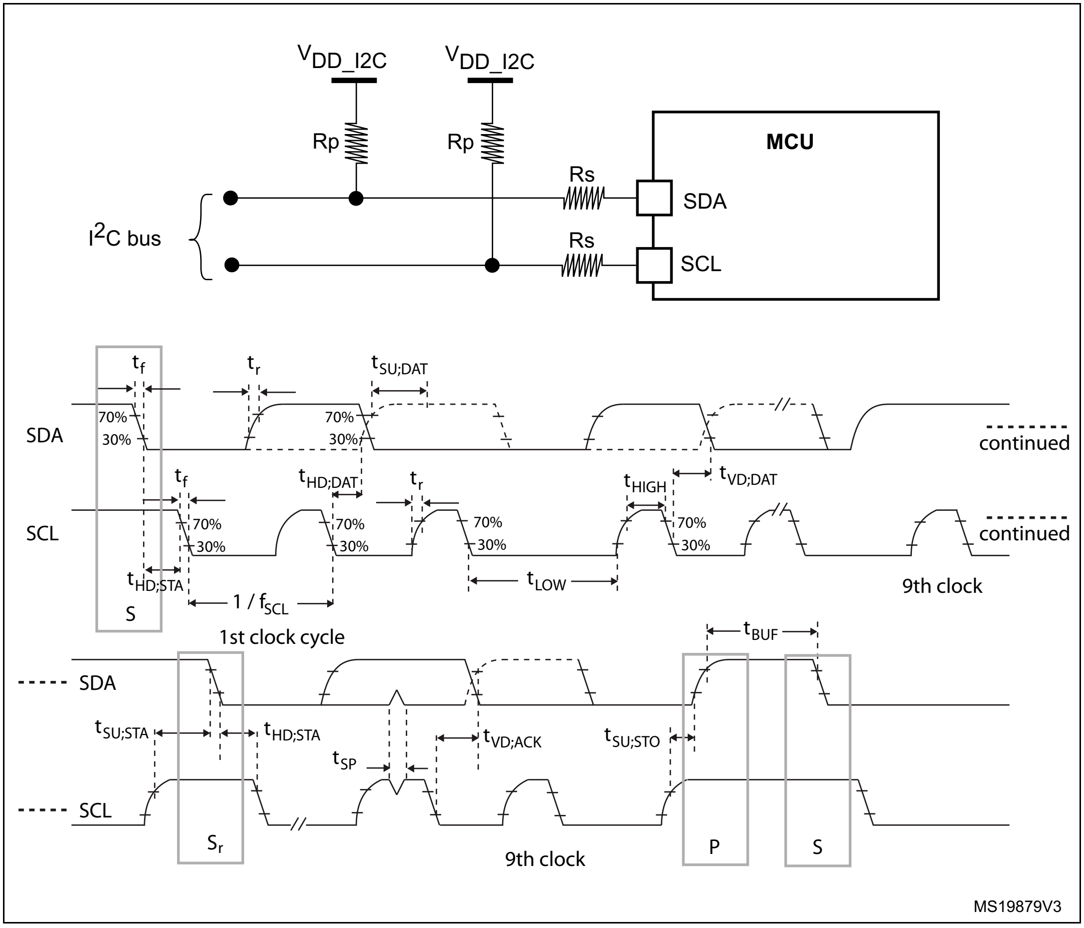
1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to the RM0365 reference manual). These characteristics are not tested in production.
2. The maximum tHD;DAT could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of tVD;DAT or tVD;ACK by a transition time.
3. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

Table 60. I2C analog filter characteristics[1]

Symbol	Parameter	Min	Max	Unit
t_{AF}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

Figure 24. I²C bus AC waveforms and measurement circuit



1. Rs: Series protection resistors, Rp: Pull-up resistors, VDD_I2C: I2C bus supply.

SPI/I^{2}S characteristics

Unless otherwise specified, the parameters given in *Table 61* for SPI or in *Table 62* for I^{2}S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^{2}S).

Table 61. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, SPI1 $2.7<V_{DD}<3.6$	-	-	24	MHz
		Slave mode, SPI1 $2.7<V_{DD}<3.6$			24	
		Master mode, SPI1/2/3 $2<V_{DD}<3.6$			18	
		Slave mode, SPI1/2/3 $2<V_{DD}<3.6$			18	
DuCy(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	5.5	-	-	
$t_{su(SI)}$		Slave mode	6.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	0	-	4*Tpclk	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	-	24	
$t_{v(SO)}$	Data output valid time	Slave mode	-	12	27	
		Slave mode, SPI1 $2.7<V_{DD}<3.6V$	-	12	18	
$t_{v(MO)}$		Master mode	-	1.5	3	
$t_{h(SO)}$	Data output hold time	Slave mode	11	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Data based on characterization results, not tested in production.

Figure 25. SPI timing diagram - slave mode and CPHA = 0

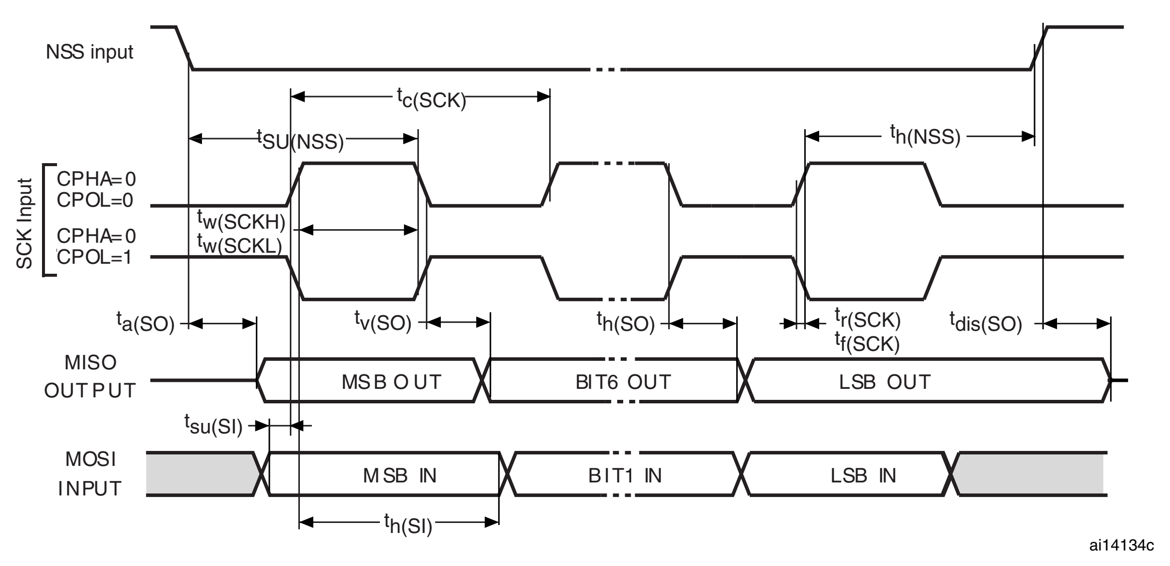
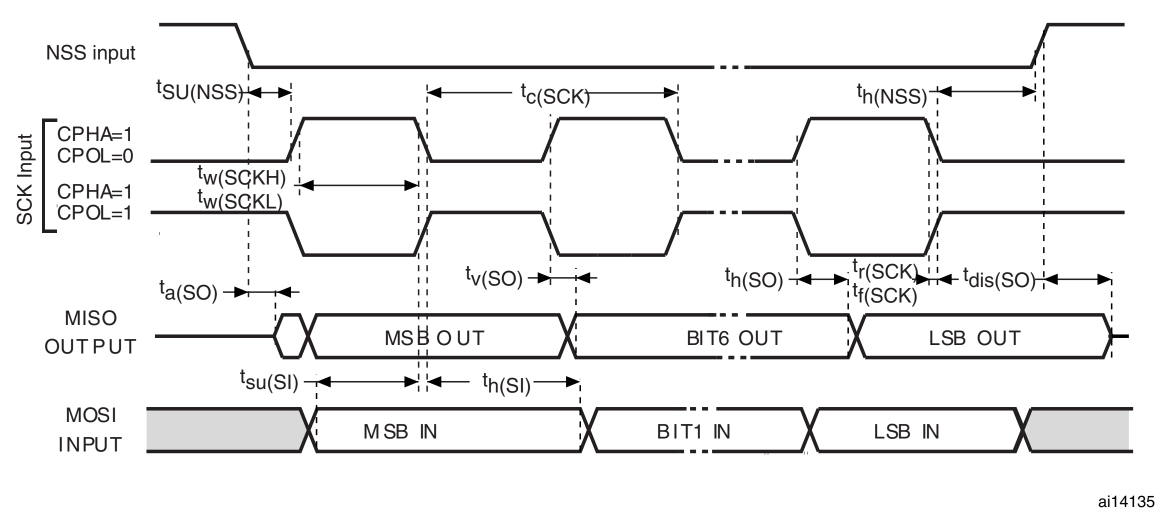
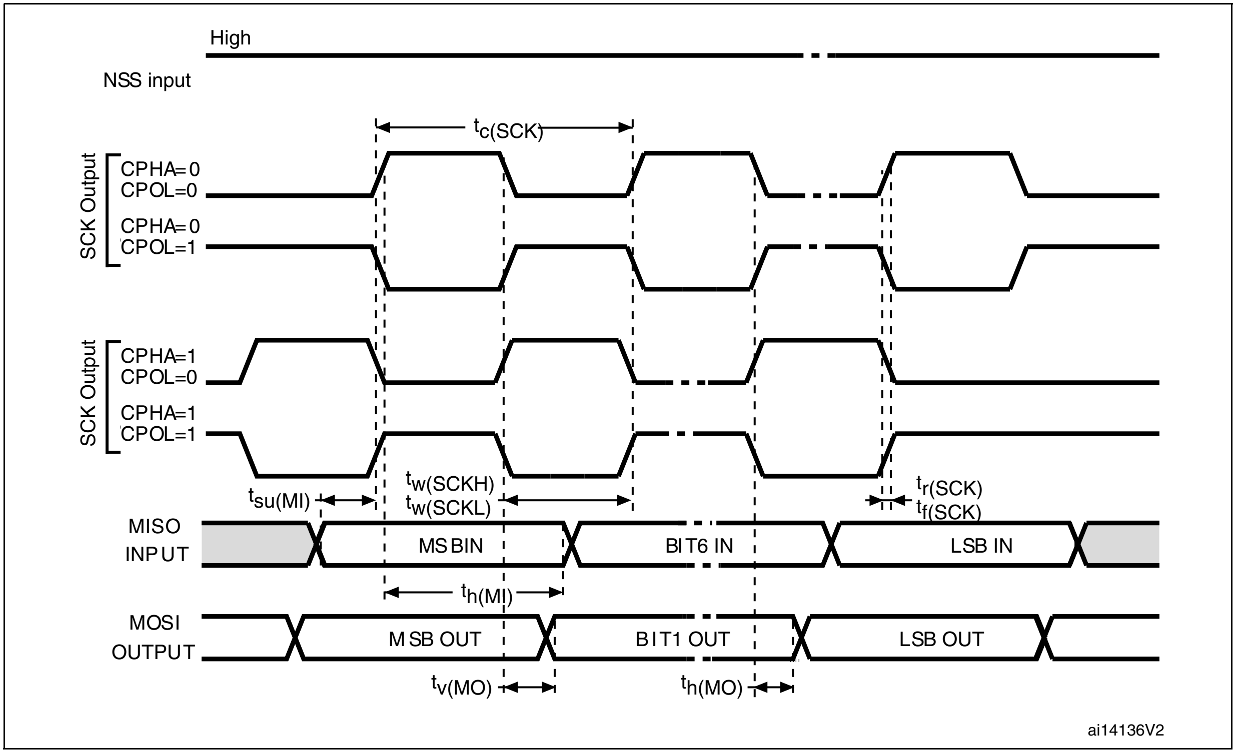


Figure 26. SPI timing diagram - slave mode and CPHA = 1[(1)]



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 27. SPI timing diagram - master mode[1]



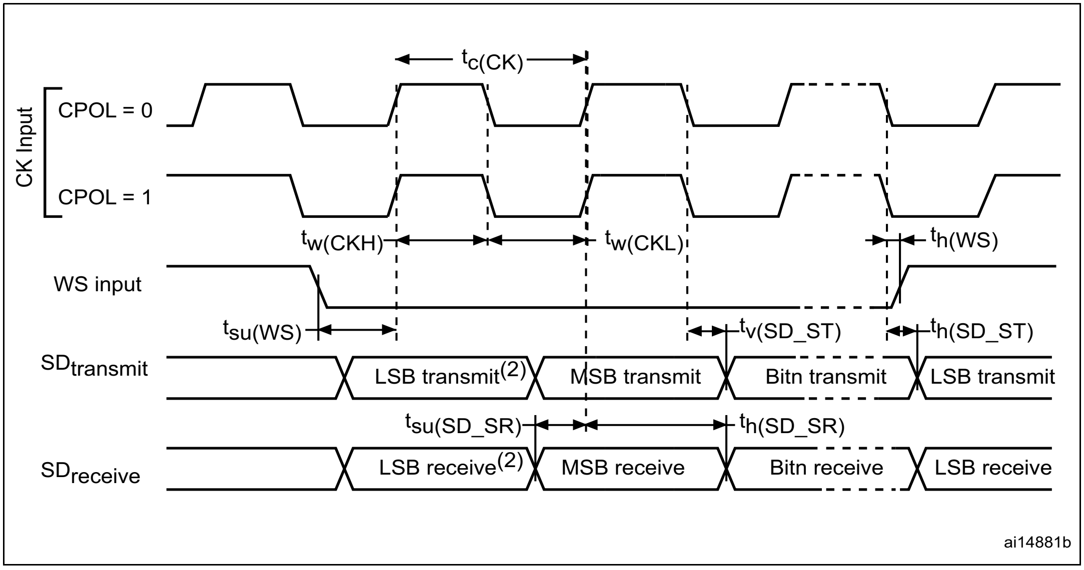
1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Table 62. I^{2}S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^{2}S clock frequency	Master data: 16 bits, audio freq=48 kHz	1.496	1.503	MHz
		Slave	0	12.288	
$t_{r(CK)}$ $t_{f(CK)}$	I^{2}S clock rise and fall time	Capacitive load C_L = 30 pF	-	8	ns
$t_{w(CKH)}$	I^{2}S clock high time	Master f_{PCLK}= 36 MHz, audio frequency = 48 kHz	331	-	
$t_{w(CKL)}$	I^{2}S clock low time		332	-	
$t_{v(WS)}$	WS valid time	Master mode	4	-	
$t_{h(WS)}$	WS hold time	Master mode	4	-	
$t_{su(WS)}$	WS setup time	Slave mode	4	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
Duty Cycle	I^{2}S slave input clock duty cycle	Slave mode	30	70	%
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	9	-	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	29	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	12	-	
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	3	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2	-	

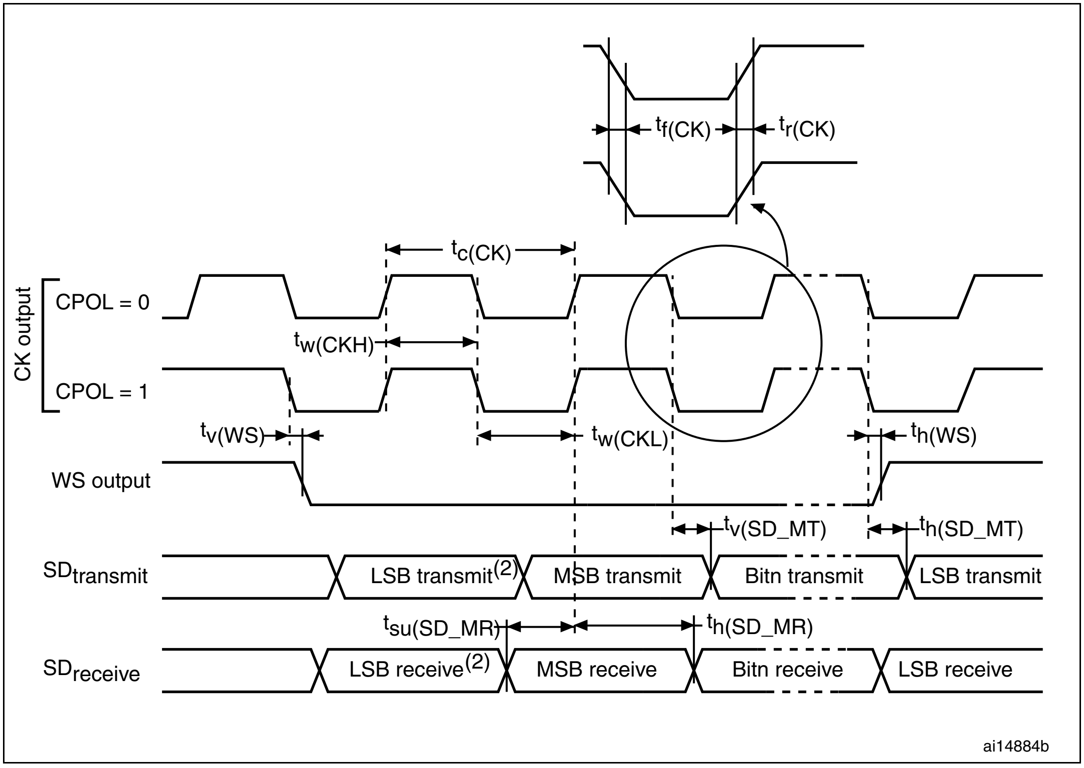
1. Data based on characterization results, not tested in production.

Figure 28. I^2S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 29. I^2S master timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB characteristics

Table 63. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 64. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.[1]	Max.[1]	Unit
Input levels					
V_{DD}	USB operating voltage[2]	-	3.0[3]	3.6	V
V_{DI}[4]	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}[4]	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}[4]	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V[5]	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}[5]	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F302xB/STM32F302xC USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB drivers.

Figure 30. USB timings: definition of data signal rise and fall time

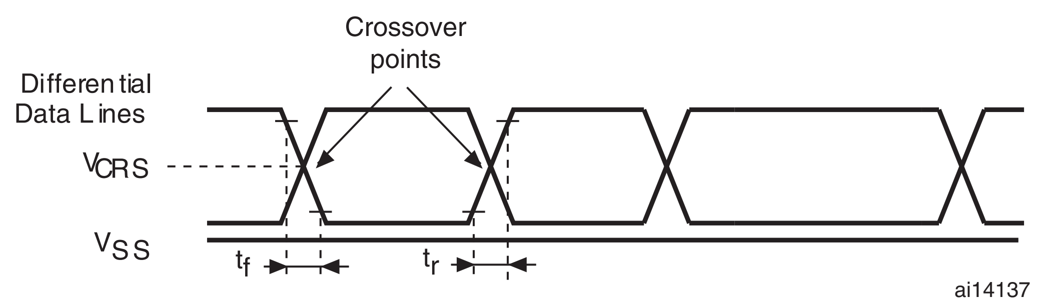


Table 65. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in *Table 66* to *Table 68* are guaranteed by design, with conditions summarized in *Table 22*.

Table 66. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	2	-	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_{S}(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	1/f_{ADC}
V_{AIN}	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	-	-	100	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}(1)	Power-up time	-	0	0	1	µs
t_{CAL}(1)	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			1/f_{ADC}
t_{latr}(1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	1/f_{ADC}
		CKMODE = 01	-	-	2	1/f_{ADC}
		CKMODE = 10	-	-	2.25	1/f_{ADC}
		CKMODE = 11	-	-	2.125	1/f_{ADC}
$t_{latrinj}$(1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	1/f_{ADC}
		CKMODE = 01	-	-	3	1/f_{ADC}
		CKMODE = 10	-	-	3.25	1/f_{ADC}
		CKMODE = 11	-	-	3.125	1/f_{ADC}
t_{S}(1)	Sampling time	f_{ADC} = 72 MHz	0.021	-	8.35	µs
		-	1.5	-	601.5	1/f_{ADC}
$T_{ADCVREG\_STUP}$(1)	ADC Voltage Regulator Start-up time	-	-	-	10	µs

Table 66. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 72 MHz Resolution = 12 bits	0.19	-	8.52	µs
		Resolution = 12 bits	14 to 614 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

1. Data guaranteed by design, not tested in Production.
2. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

Table 67. Maximum ADC R_{AIN} (1)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
12 bits	1.5	20.83	0.018	NA	NA
	2.5	34.72	0.150	NA	0.022
	4.5	62.50	0.470	0.220	0.180
	7.5	104.17	0.820	0.560	0.470
	19.5	270.83	2.70	1.80	1.50
	61.5	854.17	8.20	6.80	4.70
	181.5	2520.83	22.0	18.0	15.0
	601.5	8354.17	82.0	68.0	47.0
10 bits	1.5	20.83	0.082	NA	NA
	2.5	34.72	0.270	0.082	0.100
	4.5	62.50	0.560	0.390	0.330
	7.5	104.17	1.20	0.82	0.68
	19.5	270.83	3.30	2.70	2.20
	61.5	854.17	10.0	8.2	6.8
	181.5	2520.83	33.0	27.0	22.0
	601.5	8354.17	100.0	82.0	68.0
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00

Table 67. Maximum ADC R_{AIN} (1) (continued)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.
2. All fast channels, expect channels on PA2, PA6.
3. Channels available on PA2, PA6.

Table 68. ADC accuracy - limited test conditions, 100-pin packages (1)(2)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin package	Single ended	Fast channel 5.1 Ms	-	±3.5	±4.5	LSB
				Slow channel 4.8 Ms	-	±4	±4.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±2.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2.5	
				Slow channel 4.8 Ms	-	±2	±2.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±3	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
ENOB(4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.7	10.8	-	bits
				Slow channel 4.8 Ms	10.7	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.1	11.3	-	
SINAD(4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Table 68. ADC accuracy - limited test conditions, 100-pin packages [1][2] (continued)

Symbol	Parameter	Conditions			Min [3]	Typ	Max [3]	Unit
SNR[4]	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD[4]	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-76	-76	
				Slow channel 4.8 Ms	-	-76	-76	
			Differential	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-80	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 69. ADC accuracy, 100-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2 V ≤ V_{DDA} , V_{REF+} ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4	
EO	Offset error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
EG	Gain error		Single Ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
ED	Differential linearity error		Single Ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single Ended	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
ENOB (5)	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.2	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	

Table 69. ADC accuracy, 100-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
SINAD (5)	Signal-to-noise and distortion ratio	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, $2\ V \le V_{DDA}, V_{REF+} \le 3.6\ V$ 100-pin package	Single Ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio		Single Ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single Ended	Fast channel 5.1 Ms	-	-74	
				Slow channel 4.8 Ms	-	-74	
			Differential	Fast channel 5.1 Ms	-	-78	
				Slow channel 4.8 Ms	-	-76	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 70. ADC accuracy - limited test conditions, 64-pin packages(1)(2)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V_{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	-	±4	±4.5	LSB
				Slow channel 4.8 Ms	-	±5.5	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±2	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±5	±5.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±2	±3	
			Differential	Fast channel 5.1 Ms	-	±1.5	±1.5	
				Slow channel 4.8 Ms	-	±1.5	±2	
ENOB (4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.8	10.8	-	bit
				Slow channel 4.8 Ms	10.8	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.2	11.3	-	
SINAD (4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Table 70. ADC accuracy - limited test conditions, 64-pin packages(1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V_{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 71. ADC accuracy, 64-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps $2.0\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$ 64-pin package	Single ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB (5)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	

Table 71. ADC accuracy, 64-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
SNR(5)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, 2 V ≤ V_{DDA} ≤ 3.6 V 64-pin package	Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 72. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.14: I/O port characteristics* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 31. ADC accuracy characteristics

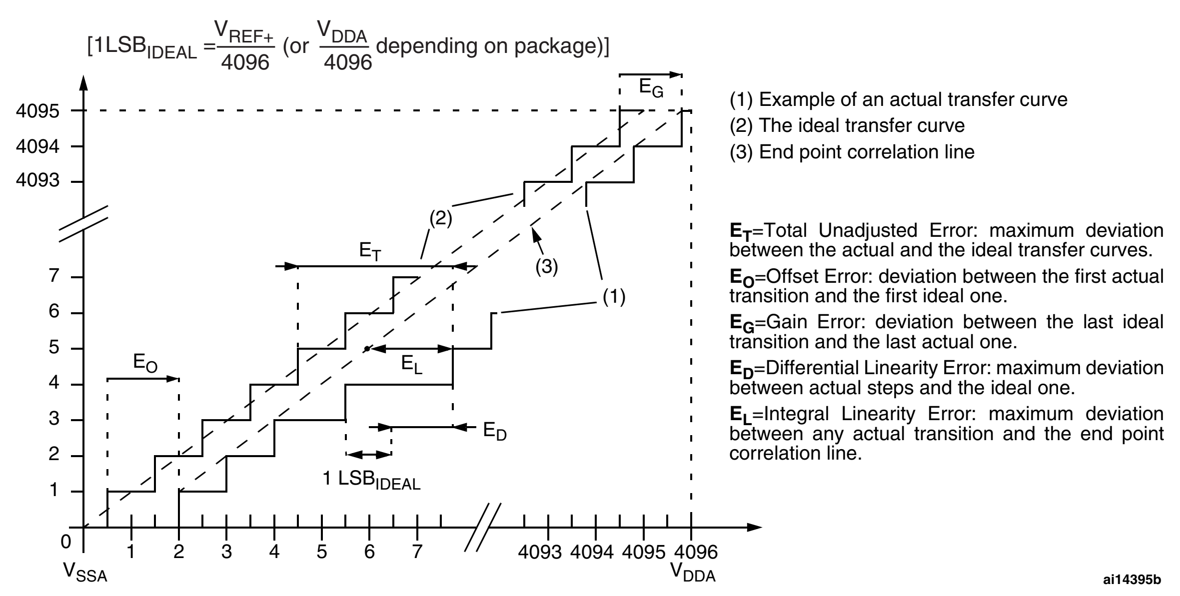
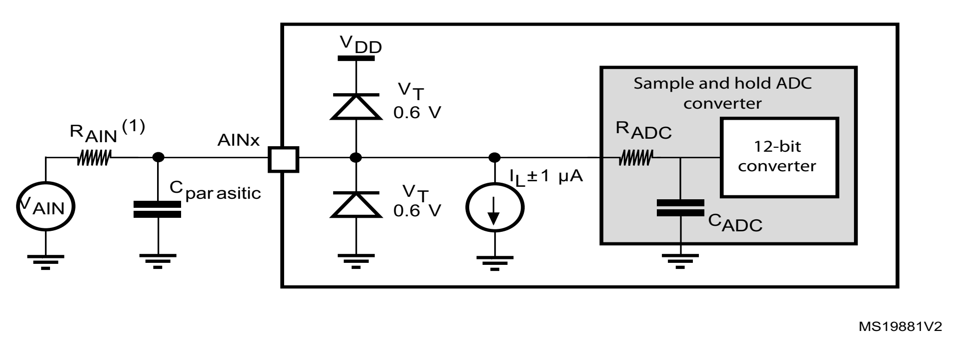


Figure 32. Typical connection diagram using the ADC



1. Refer to *Table 66* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.19 DAC electrical specifications

Table 73. DAC characteristics

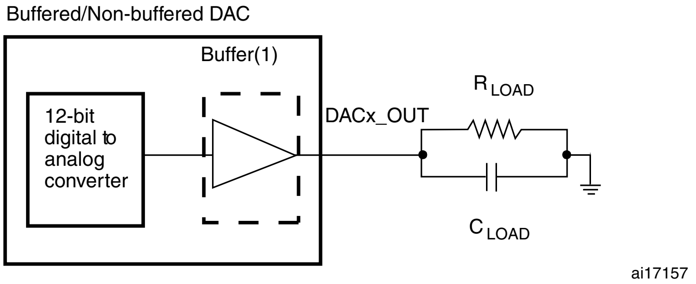
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	DAC output buffer ON	2.4	-	3.6	V
R_{LOAD}(1)	Resistive load	DAC output buffer ON	5	-	-	kΩ
R_O(1)	Output impedance	DAC output buffer ON	-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	DAC output buffer ON	-	-	50	pF
V_{DAC_OUT} (1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V DAC output buffer ON.	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	-	0.5	V_{DDA} - 1LSB	mV
I_{DDA}(3)	DAC DC current consumption in quiescent mode (Standby mode)(2)	With no load, middle code (0x800) on the input.	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code	-	-	±0.5	LSB
		Given for a 12-bit input code	-	-	±2	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	±1	LSB
		Given for a 12-bit input code	-	-	±4	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V	-	-	±3	LSB
		Given for a 12-bit input code at V_{DDA} = 3.6 V	-	-	±12	LSB
Gain error(3)	Gain error	Given for a 12-bit input code	-	-	±0.5	%
$t_{SETTLING}$(3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	C_{LOAD} ≤50 pF, R_{LOAD} ≥ 5 kΩ	-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	C_{LOAD} ≤50 pF, R_{LOAD} ≥ 5 kΩ	-	-	1	MS/s

Table 73. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WAKEUP}[3]	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	6.5	10	µs
PSRR+ [1]	Power supply rejection ratio (to V_{DDA}) (static DC measurement	$C_{LOAD} = 50$ pF, No $R_{LOAD} \geq 5$ kΩ,	-	–67	–40	dB

1. Guaranteed by design, not tested in production.
2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 33. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.20 Comparator characteristics

Table 74. Comparator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2	-	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-	-	1.2	-	
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
t_{S_SC}	Scaler startup time from power down	-	-	-	0.1	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification	-	-	60	µs

Table 74. Comparator characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Data guaranteed by design, not tested in production.

6.3.21 Operational amplifier characteristics

Table 75. Operational amplifier characteristics(1)

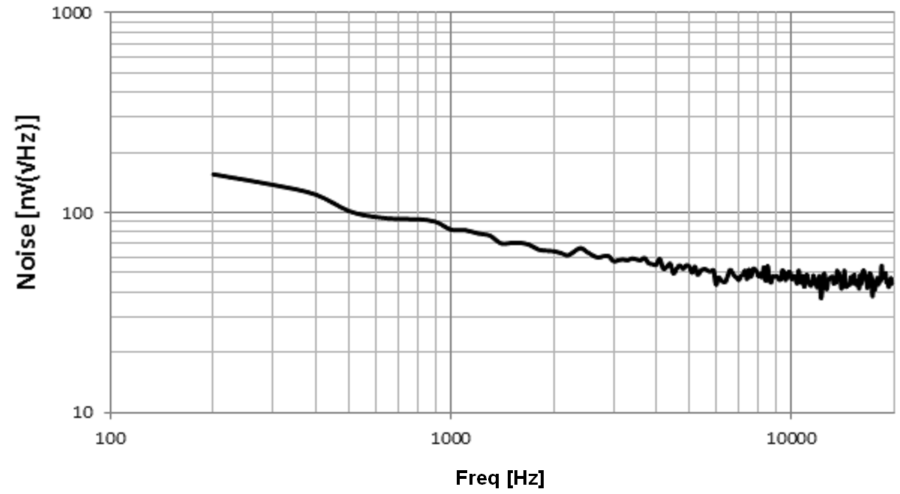
Symbol	Parameter		Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
IDDOPAMP	Consumption		No load, quiescent mode	-	690	1450	µA
TS_OPAMP_VOUT	ADC sampling time when reading the OPAMP output.		-	400	-	-	ns
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF
VOH_{SAT}	High saturation voltage		R_{load} = min, Input at V_{DDA}.	-	-	100	mV
			R_{load} = 20K, Input at V_{DDA}.	-	-	20	
VOL_{SAT}	Low saturation voltage		Rload = min, input at 0V	-	-	100	
			Rload = 20K, input at 0V.	-	-	20	
φm	Phase margin		-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		-	-	-	2	ms
t_{WAKEUP}	Wake up time from OFF state.		$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ, Follower configuration	-	2.8	5	µs

Table 75. Operational amplifier characteristics[1] (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode [2]	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	
I_{bias}	OPAMP input bias current	-	-	-	±0.2[3]	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design, not tested in production.
2. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
3. Mostly TTa I/O leakage, when used in analog mode.

Figure 34. OPAMP voltage noise versus frequency



6.3.22 Temperature sensor characteristics

Table 76. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 77. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

6.3.23 V_{BAT} monitoring characteristics

Table 78. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	µs

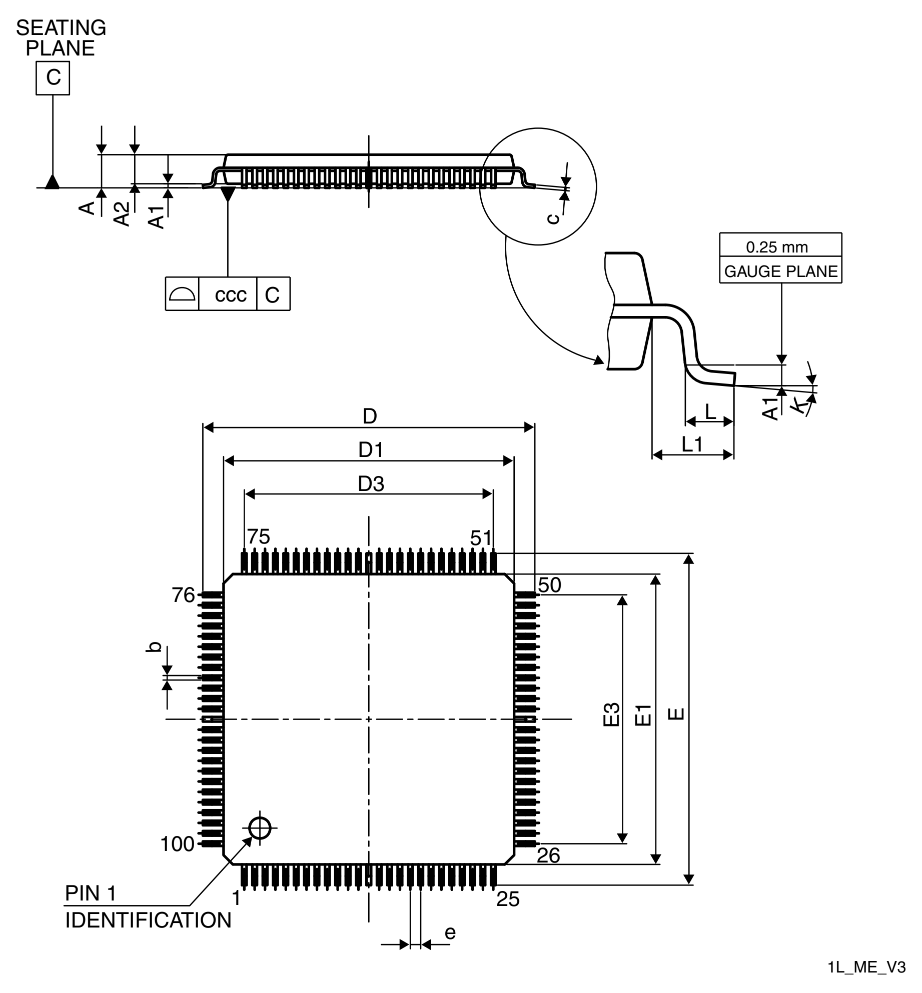
1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

7 Package characteristics

7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 35. LQFP100 – 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 79. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data

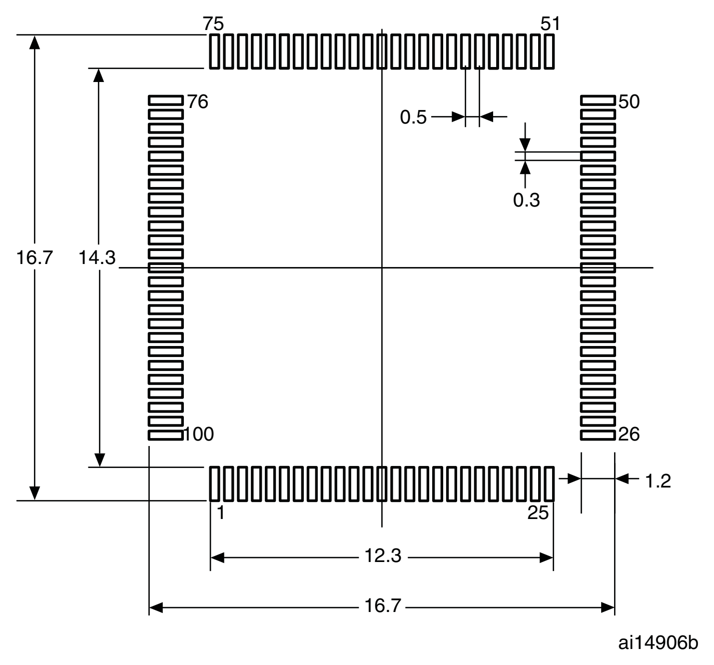
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.2	0.0035	-	0.0079
D	15.80	16.00	16.2	0.622	0.6299	0.6378
D1	13.80	14.00	14.2	0.5433	0.5512	0.5591
D3	-	12.00	-	-	0.4724	-
E	15.80	16.00	16.2	0.622	0.6299	0.6378

Table 79. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.80	14.00	14.2	0.5433	0.5512	0.5591
E3	-	12.00	-	-	0.4724	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

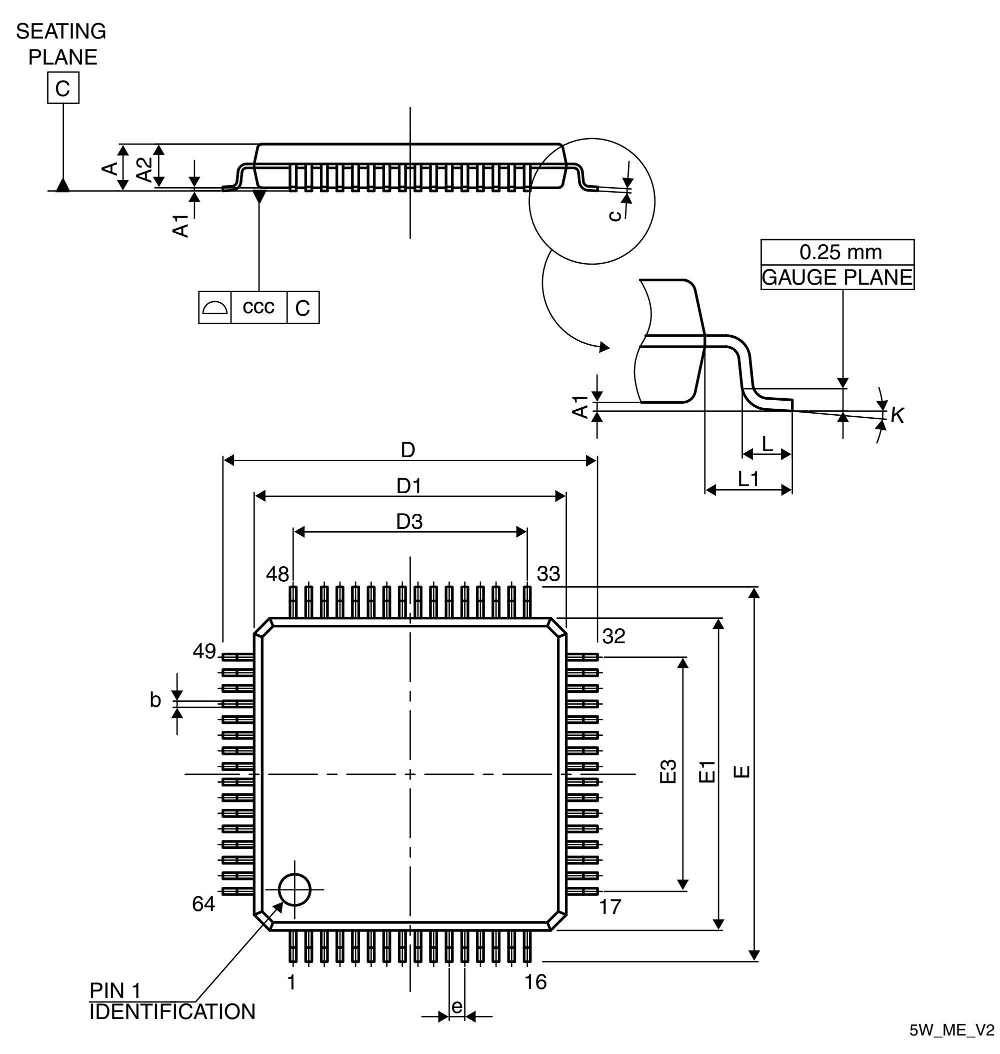
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. LQFP100 recommended footprint



1. Dimensions are in millimeters.

Figure 37. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 80. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data

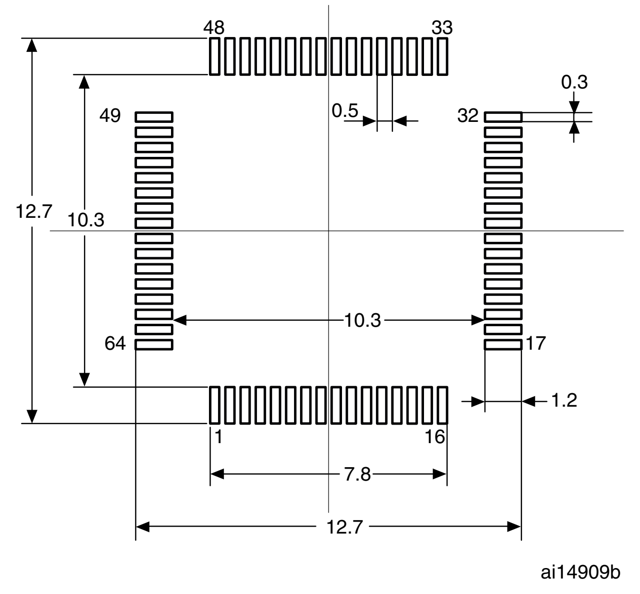
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.350	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106

Table 80. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.09	-	0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.4646	0.4724	0.4803
D1	9.80	10.00	10.20	0.3858	0.3937	0.4016
D3	-	7.50	-	-	0.2953	-
E	11.80	12.00	12.20	0.4646	0.4724	0.4803
E1	9.80	10.00	10.20	0.3858	0.3937	0.4016
E3	-	7.50	-	-	0.2953	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

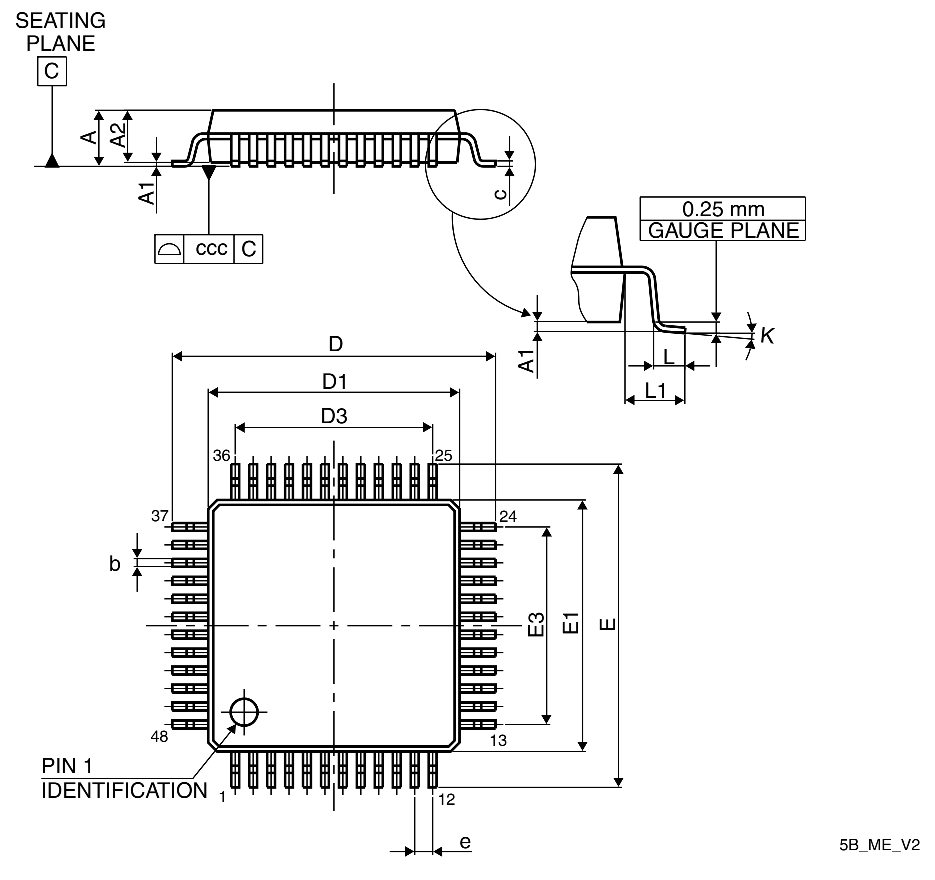
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. LQFP64 recommended footprint



1. Dimensions are in millimeters.

Figure 39. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 81. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

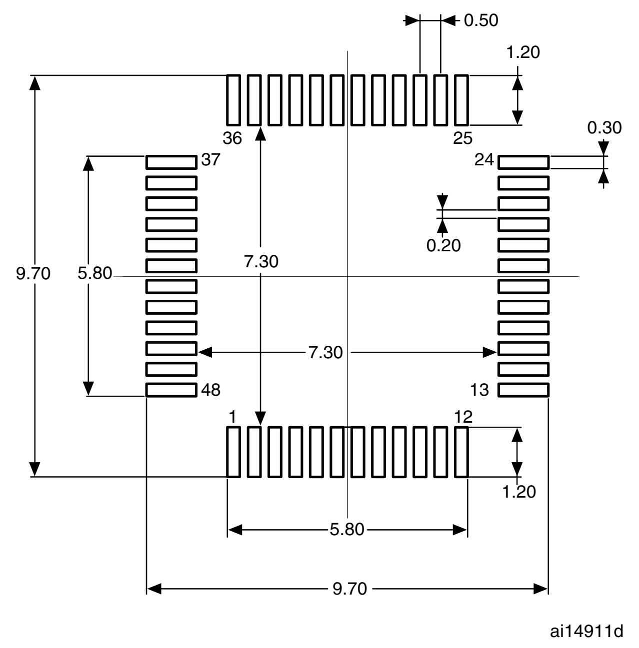
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.20	0.0035	-	0.0079
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.80	7.00	7.20	0.2677	0.2756	0.2835
D3	-	5.50	-	-	0.2165	-
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3	-	5.50	-	-	0.2165	-
e	-	0.50	-	-	0.0197	-

Table 81. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP48 recommended footprint



1. Dimensions are in millimeters.

7.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions on page 56*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max x } \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma\ (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 82. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	41	

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F302xB/STM32F302xC at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

> Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 3 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 2 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V
>
> P_{INTmax} = 50 mA × 3.5 V= 175 mW
>
> P_{IOmax} = 3 × 8 mA × 0.4 V + 2 × 20 mA × 1.3 V = 61.6 mW
>
> This gives: P_{INTmax} = 175 mW and P_{IOmax} = 61.6 mW:
>
> P_{Dmax} = 175 + 61.6 = 236.6 mW

Thus: P_{Dmax} = 236.6 mW

Using the values obtained in *Table 82* T_{Jmax} is calculated as follows:

- For LQFP64, 45°C/W

> T_{Jmax} = 82 °C + (45°C/W × 236.6 mW) = 82 °C + 10.65 °C = 92.65 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 9 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 9 × 8 mA × 0.4 V = 28.8 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 28.8 mW:

P_{Dmax} = 70 + 28.8 = 98.8 mW

Thus: P_{Dmax} = 98.8 mW

Using the values obtained in *Table 82* T_{Jmax} is calculated as follows:

– For LQFP100, 41°C/W

T_{Jmax} = 115 °C + (41°C/W × 98.8 mW) = 115 °C + 4.05 °C = 119.05 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*).

8 Part numbering

Table 83. Ordering information scheme

Example: STM32F302 R B T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

302 = STM32F302xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size

B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts
TR = tape and reel

9 Revision history

Table 84. Document revision history

Date	Revision	Changes
21-Nov-2013	1	Initial release
16-Apr-2014	2	Updated *Table 36: Peripheral current consumption*. Updated SRAM size in *Table 2: STM32F302xx family device features and peripheral counts*, Cover page and description. Updated *Section 6.3.17: Communications interfaces* I^2C interface. Updated *Table 48: EMI characteristics* conditions :3.3v replaced by 3.6V. Updated *Table 75: Operational amplifier characteristics* adding TS_OPAMP_VOUT row. Updated *Section 3.12: Fast analog-to-digital converter (ADC)*. updated ARM and Cortex trademark. Updated *Table 30: Typical and maximum VDD consumption in Stop and Standby modes* with Max value at 85°C and 105°C. Updated *Table 68: ADC accuracy - limited test conditions, 100-pin packages* and *Table 69: ADC accuracy, 100-pin packages* for 100-pin package. Added *Table 70: ADC accuracy - limited test conditions, 64-pin packages* and *Table 71: ADC accuracy, 64-pin packages*for 64-pin package. Added *Table 72: ADC accuracy at 1MSPS* for 1MSPS sampling frequency. Updated *Table 61: SPI characteristics*. Updated *Table 73: DAC characteristics*. Updated note 2 and note 3 of *Table 67: Maximum ADC RAIN*.

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