Apacer

RoHS Compliant

Embedded Multimedia Card 5.1

Commercial EM120 Product Specifications

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Version 1.1

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Product Features

- Packaged NAND flash memory with eMMC 5.1 interface
- Backward compatible with previous eMMC specification revisions
- 153-ball FBGA RoHS compliant package
- Package size: 11.5 x 13.0 x 1.0mm
- Capacity: 8GB
- NAND flash type: MLC
- Operating voltage range:
  - VCCQ = 1.8V/3.3V
  - VCC = 3.3V
- Temperature range:
  - Operating temperature (Tc): -25°C to 85°C
  - Storage temperature (Tc): -40°C to 85°C

eMMC-Specific Features

- High-speed eMMC protocol
- Variable clock frequencies of 0-200MHz
- Ten-wire bus interface (clock, 1 bit command, 8 bit data bus) with a hardware reset
- Supports three different data bus widths: 1 bit (default), 4 bits, 8 bits
- Bus modes:
  - Single data transfer rate: up to 52MB/s (using 8 parallel data lines at 52MHz)
  - High speed, single data rate mode (HS-200): up to 200MB/s @ 200MHz
  - High speed, dual data rate mode (HS-400): up to 400MB/s @ 200MHz
- Error free memory access
  - Internal error correction code (ECC) for improved data storage integrity
  - Internal enhanced data management algorithm
  - Data protection for sudden power failure during program operations
- Security
  - Secure bad block erase commands
  - Enhanced write protection with permanent and partial protection options
- Field firmware update (FFU)
- Device Health Report
- Pre EOL information
- Optimal size
- Production state awareness
- Power-off notification for sleep

Table of Contents

1. General Description

Apacer EM120 is an embedded, non-volatile memory system that combines multi-level cell (MLC) NAND flash memory with an onboard eMMC controller, supporting the JEDEC Standard eMMC 5.1 interface. The integrated eMMC controller directly manages NAND flash media, freeing the host processor from various tasks, including ECC, wear-leveling, IOPS optimization, and read sensing.

EM120 serves as the ideal storage solution for a wide range of commercial applications, including digital TVs, set-top boxes, home automation, camera drones, body-worn cameras, AR/VR systems, wearable gadgets, electronic learning products, and more. Its compact BGA package sizes and minimal power consumption render eMMC an affordable and efficient memory solution for mobile and embedded products.

Offering 8GB of capacity within a JEDEC-compatible form factor, EM120 provides an excellent solution for vendors looking for seamless integration, a quick market entry, and ample storage capacity.

2. Signal Assignments (153-Ball)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	VSS	NC	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	VDDI	NC	VSSQ	NC	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		NC	VCC	VSS	VSF1	VSF2	VSF3		NC	NC	NC	E
F	NC	NC	NC		VCC					VSF4		NC	NC	NC	F
G	NC	NC	NC		VSS					VSF5		NC	NC	NC	G
H	NC	NC	NC		DS					VSS		NC	NC	NC	H
J	NC	NC	NC		VSS					VCC		NC	NC	NC	J
K	NC	NC	NC		RST_n	NC	NC	VSS	VCC	VSF6		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	VSSQ	NC	VCCQ	VSSQ	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	VCCQ	VSSQ	VCCQ	VSSQ	NC	NC	NC	VSF7	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 2-1 Ball Assignments

3. Product Specifications

3.1 Partition Capacity

Table 3-1 Partition Capacity

Capacity	Boot Partition 1	Boot Partition 2	RPMB
8GB	4096 KB	4096 KB	4096 KB

3.2 User Density

Table 3-2 User Density

Capacity	User Density
8GB	7,837,581,312 Bytes

3.3 System Performance

Table 3-3 System Performance

Capacity	Dynamic Booster Value (MB/s)	
	Sequential Read	Sequential Write
8GB	280	105

Notes:
- Performance numbers may be subject to changes without notice
- Performance numbers can vary under different operating conditions. Values are given at an 8-bit bus width and HS400 bus mode.

3.4 Power Consumption

Table 3-4 Power Consumption

Capacity	Read (mA)		Write (mA)		Sleep Current (mA)	
	VCCQ = 1.8V	VCC=3.3V	VCCQ = 1.8V	VCC=3.3V	VCCQ = 1.8V	VCC=3.3V
8GB	165	80	90	50	0.07	0.07

Notes:
- Power consumption numbers may be subject to changes without notice
- Power consumption values are given at an 8-bit bus width, a clock frequency of 200MHz DDR mode, VCC = 3.3V±5%, VCCQ = 1.8V±5%
- Standby current is measured at VCC = 3.3V±5%, VCCQ = 3.3V±5%, 8-bit bus width without clock frequency.

3.5 Power Supply Voltage

Table 3-5 Operating Voltage

Parameter	Symbol	Min	Max	Unit
Supply voltage (NAND)	VCC	2.7	3.6	V
Supply voltage (I/O)	VCCQ	2.7	3.6	V
		1.7	1.95	V
Supply power-up for 3.3V	tPRUH	0.036	35	ms
Supply power-up for 1.8V	tPRUL	0.018	25	ms

Note: Power noise on the supply voltage shall not exceed ±3%.

3.6 Temperature

Table 3-6 Temperature

Parameter	Rating
Operating (Tc)	-25°C to 85°C
Storage (Tc)	-40°C to 85°C

Note: Tc: case temperature. The operating temperature is determined by the case temperature. Adequate airflow is advisable as it enables the device to maintain optimal temperatures, especially in environments with heavy workloads.

4. eMMC Device and System

4.1 eMMC System Overview

The eMMC specification addresses the behavior of the interface and the device controller. While this specification implies the presence of a host controller and a memory storage array, it does not fully define their operation.

Apacer EM120 comprises a single-chip MMC controller and a NAND flash memory module. The microcontroller interfaces with a host system, facilitating the reading and writing of data to and from the NAND flash memory module. This controller allows the host to operate independently from the intricacies of erasing and programming the flash memory.

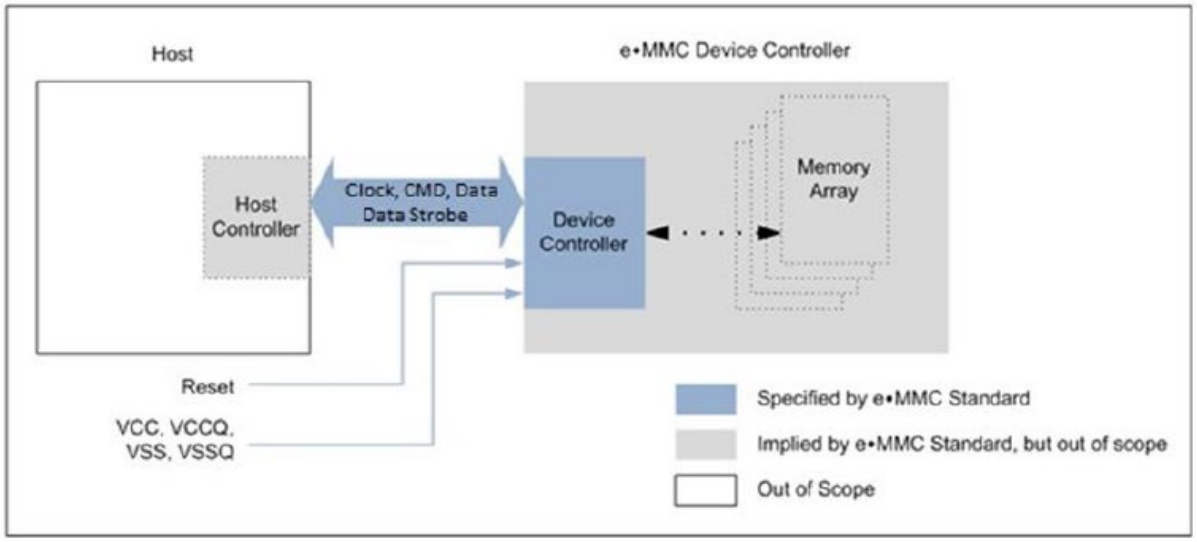


Figure 4-1 eMMC System Overview

4.2 Memory Addressing

Previous implementations of the eMMC specification followed byte addressing with a 32-bit field. This addressing mechanism allowed for eMMC densities up to and including 2GB.

To support larger densities, the addressing mechanism was updated to accommodate sector addresses (512B sectors). Sector addresses should be used for all devices with a capacity larger than 2GB.

To determine the addressing mode, the host should read bit [30:29] in the OCR register.

4.3 Signal Descriptions

Apacer EM120 transfers data via a number of data bus signals. The communication signals are summarized in the table below.

Table 4-1 Signal Descriptions

Name	Type	Description
CLK	I	Clock: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
DAT[7:0]	I/O/PP	Data: These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.
CMD	I/O/PP/OD	Command: This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the device to the host.
RST_n	I	Hardware Reset: By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected.
VCC	S	Supply voltage for core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for core
VSSQ	S	Supply voltage ground for I/O
DS	O/PP	Data Strobe: This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

Note: I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry that puts the device into a defined state after the power-on device.
- A reset signal
- Sending a special command

4.4 Bus Protocol

After a power-on reset, the host must initialize the device using a special message-based eMMC bus protocol. For more details, refer to Section 5.3.1 of the JEDEC Standard Specification No. JESD84-B51.

4.5 Bus Modes

Apacer EM120 supports all bus modes defined in the JEDEC eMMC 5.1 specification. These modes are summarized in the table below.

Table 4-2 Bus Modes

Mode	Data Rate	IO Voltage	Bus Width	CLK Frequency	Maximum Data Bus Throughput
Legacy MMC	Single	3.3V / 1.8V	1, 4, 8	0 – 26 MHz	26 MB/s
High Speed SDR	Single	3.3V / 1.8V	4, 8	0 – 52 MHz	52 MB/s
High Speed DDR	Dual	3.3V / 1.8V	4, 8	0 – 52 MHz	104 MB/s
HS200	Single	1.8V	4, 8	0 – 200 MHz	200 MB/s
HS400	Dual	1.8V	8	0 – 200 MHz	400 MB/s

4.5.1 HS200 Bus Speed Mode

The HS200 mode offers the following features:

- SDR data sampling method
- CLK frequency up to 200MHz data rate – up to 200MB/s
- Only 8-bit bus width supported
- Signaling levels of 1.8V
- Support up to 4 selectable Drive Strength
- Tuning concept for Read Operations

4.5.2 HS200 System Block Diagram

Figure 4-2 illustrates a typical HS200 host and device system. The host has a clock generator that provides CLK to the device. During write operations, the clock and data direction align, enabling synchronous data transfer with CLK, irrespective of transmission line delay. In read operations, clock and data direction are opposite, causing the read data received by the host to be delayed due to round-trip delay, output delay, and latency in both the host and the device. Consequently, during reads, the host needs an adjustable sampling point to ensure reliable reception of incoming data.

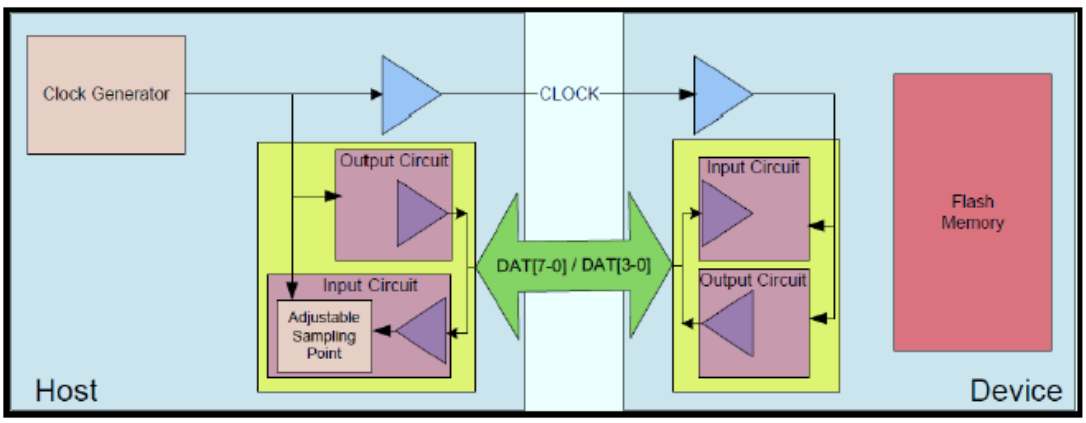


Figure 4-2 HS200 Host and Device Block Diagram

4.5.3 HS400 Bus Speed Mode

The HS400 mode offers the following features:

- DDR data sampling method
- CLK frequency up to 200MHz data rate – up to 200MB/s
- Only 8-bit bus width supported
- Signaling levels of 1.8V
- Support up to 5 selective Drive Strength
- Data strobe signal is toggled only for Data out and CRC response

4.5.4 HS400 System Block Diagram

Figure 4-3 illustrates a typical HS400 Host and device system. The host has a clock generator that provides CLK to the device. During read operations, Data Strobe is generated by the device's output circuit, allowing the host to receive data aligned with the edge of Data Strobe.

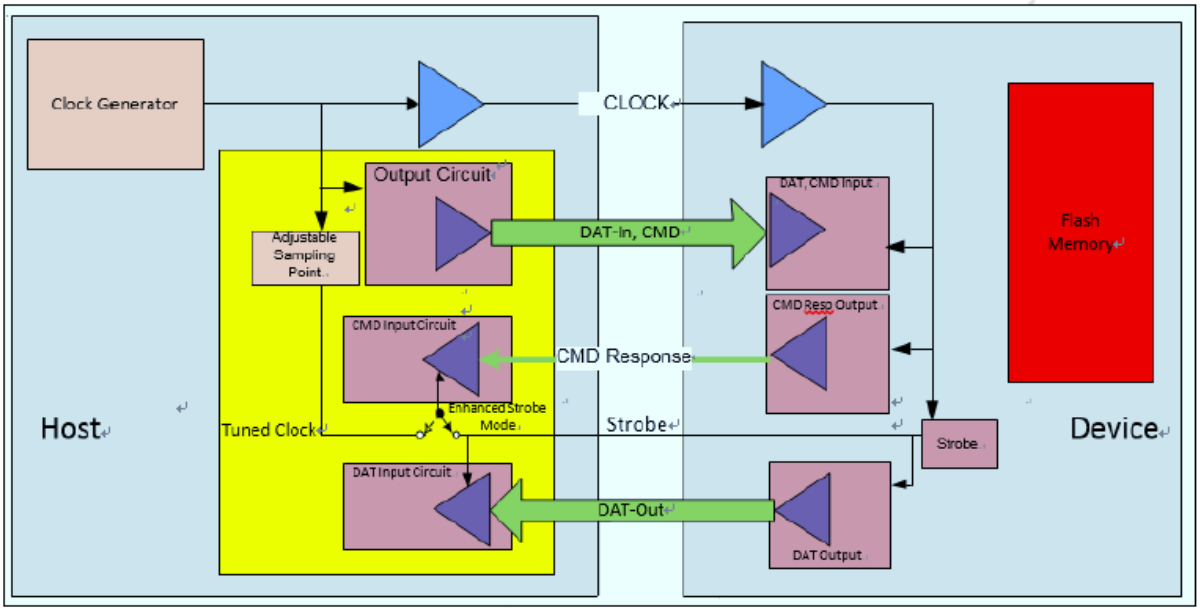


Figure 4-3 HS400 Host and Device Block Diagram

5. eMMC 5.1 Selected Features

5.1 eMMC Overview

All communication between the host and the device is controlled by the host (main chip). The host sends a command, which elicits a response from the device. For more details, refer to Section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

Five operation modes are defined for the eMMC system:

- Boot operation mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

5.1.1 Boot Operation Mode

In boot operation mode, the master (eMMC host) can read boot data from the slave (eMMC device) by keeping the CMD line low or by sending CMD0 with the argument + 0xFFFFFFFA before issuing CMD1. The data can be read from either the boot area or the user area, depending on the register settings. For more details, refer to Section 6.3 of the JEDEC Standard Specification No.JESD84-B51.

5.1.2 Device Identification Mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to Section 6.4 of the JEDEC Standard Specification No.JESD84-B51.

5.1.3 Interrupt Mode

The interrupt mode in the eMMC system enables the master (eMMC host) to allocate transmission allowances to the slaves (devices) simultaneously. This mode reduces the polling burden on the host, thus lowering the power consumption of the system, all while ensuring the host remains adequately responsive to a device's service request. Supporting the eMMC interrupt mode is an option for both the host and the devices. For more details, refer to Section 6.5 of the JEDEC Standard Specification No.JESD84-B51.

5.1.4 Data Transfer Mode

When the device is in Stand-by State, communication over the CMD and DAT lines will be conducted in push-pull mode. For more details, refer to Section 6.6 of the JEDEC Standard Specification No.JESD84-B51.

5.1.5 Inactive Mode

The device will enter an inactive mode if either the device's operating voltage range or access mode is not valid. The device can also enter the inactive mode using the GO_INACTIVE_STATE command (CMD15). A power cycle will reset the device to the Pre-idle state. For more details, refer to Section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

5.2 Field Firmware Update (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the eMMC device and instructs the eMMC device to install the new downloaded firmware into the device.

To initiate the FFU (Firmware Update) process, the host first verifies if the eMMC device supports FFU capabilities by reading the SUPPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the eMMC device supports the FFU feature, the host can proceed with the FFU process.

The FFU process begins by switching to FFU Mode in the MODE_CONFIG field of the EXT_CSD. In FFU Mode, the host should use either closed-ended or open-ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands as defined in the FFU_ARG field. Using different arguments for these commands is not defined, and the FFU process may fail.

The host should set the Block Length to be DATA_SECTOR_SIZE. The downloaded firmware bundle must be aligned to the DATA_SECTOR_SIZE (internal padding of the bundle might be required). In FFU Mode, the host can send the new firmware bundle to the device using one or more write commands.

To return to regular functionality for write and read commands, the host can switch the MODE_CONFIG field in the EXT_CSD back to the Normal state. Switching out of FFU Mode may abort the firmware download operation. When the host switches back to FFU Mode, it should check the FFU Status to determine the number of sectors that were successfully downloaded by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. If the number of sectors downloaded successfully is zero, the host should restart downloading the new firmware bundle from its first sector. If the number of successfully downloaded sectors is positive, the host can continue the download from the next sector, which will resume the firmware download operation.

In the event that the MODE_OPERATION_CODES field is not supported by the device, the host should return to the NORMAL state and initiate a CMD0/HW_Reset/Power cycle to install the new firmware. In such cases, the device doesn't need to use NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED. In both cases, if a CMD0/HW_Reset/Power cycle occurs before the host successfully downloads the new firmware bundle to the device, it may cause the firmware download process to be aborted.

5.3 Power-off Notifications for Sleep

The host should notify the device before powering the device off. This notification allows the device to better prepare itself for the impending power-off operation. "Powering the device off" refers to turning off all its power supplies. Specifically, the host should issue a power-off notification (POWER_OFF_LONG or POWER_OFF_SHORT) if it intends to turn off both VCC and VCCQ power. Alternatively, it may use a power-off notification (SLEEP_NOTIFICATION) if its intention is to turn off VCC after transitioning the device to the Sleep state.

To signal to the device that it supports power-off notifications, a supporting host should initially set the POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01). To perform a power-off operation, before shutting down the device, the host changes the value to either POWER_OFF_SHORT (0x02) or POWER_OFF_LONG (0x03). The host should then wait for the busy line to be de-asserted. Once the setting has changed to either 0x02 or 0x03, the host can safely power off the device.

If the host wants to enter or exit the Sleep state and has set the POWER_OFF_NOTIFICATION byte to POWERED_ON, it may issue the SLEEP_AWAKE command (CMD5). Before transitioning to the Standby state and then to the Sleep state, the host sets POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and waits for the DAT0 line to be de-asserted. While in the Sleep (slp) state, VCC (Memory supply) may be turned off as defined in Section 6.6.21 of the JEDEC Standard Specification No.JESD84-B51 other than VCC while the device is in the Sleep (slp) state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of the Sleep (slp) state back to the Transfer state using CMD5 and CMD7, and then execute a power-off notification by setting the POWER_OFF_NOTIFICATION byte to either POWER_OFF_SHORT or POWER_OFF_LONG.

If the host continues to send commands to the device after switching to the power-off settings (POWER_OFF_LONG, POWER_OFF_SHORT, or SLEEP_NOTIFICATION) or performs HPI during its busy condition, the device shall restore the POWER_OFF_NOTIFICATION byte to POWERED_ON. If the host attempts to change the POWER_OFF_NOTIFICATION to 0x00 after writing another value, a SWITCH_ERROR is generated.

The difference between the two power-off modes is how urgently the host wishes to turn the power off. The device should respond to POWER_OFF_SHORT quickly within the generic CMD6 timeout. If more time is acceptable, POWER_OFF_LONG may be used, and the device should respond to it within the POWER_OFF_LONG_TIME timeout.

While POWER_OFF_NOTIFICATION is set to POWERED_ON, the device expects the host to:

- Maintain the device power supplies in their active mode (both VCC and VCCQ).
- Avoid intentionally powering off the device before changing POWER_OFF_NOTIFICATION to either POWER_OFF_LONG or POWER_OFF_SHORT.
- Refrain from intentionally powering off VCC before changing POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and before transitioning the device to the Sleep state.

Before transitioning to the Sleep state, hosts may set the POWER_OFF_NOTIFICATION byte to SLEEP_NOTIFICATION (0x04) if they are aware that the device is capable of autonomously initiating background operations for potential performance improvements. The host should wait for the busy line to be de-asserted. The busy line may be asserted for a period defined in the SLEEP_NOTIFICATION_TIME byte in EXT_CSD [216]. Once the setting has changed to 0x04, the host can set the device into Sleep mode (CMD7+CMD5). After exiting Sleep mode, the POWER_OFF_NOTIFICATION byte will restore its value to POWERED_ON. HPI may interrupt the SLEEP_NOTIFICATION operation. In that case, the POWER_OFF_NOTIFICATION byte will be restored to POWERED_ON.

6. Register Settings

Within the device interface, six registers are defined: OCR, CID, CSD, EXT_CSD, RCA, and DSR. These can only be accessed by the corresponding commands (refer to Section 6.10 of JEDEC Standard Specification No.JESD84-B51 for details).

Table 6-1 eMMC Registers

Name	Width (Bytes)	Description	Implementation
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the device.	Mandatory
CID	16	Device Identification number, an individual number for identification.	Mandatory
CSD	16	Device Specific Data, information about the device operation conditions.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the device capabilities and selected modes. Introduced in standard v4.0.	Mandatory
RCA	2	Relative Device Address is the device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register. Used to configure the device's output drivers.	Optional

6.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the device-power-up procedure has been completed. The OCR register shall be implemented by all devices.

6.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the device identification information used during the device identification phase as required by eMMC protocol. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

6.3 CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format…etc. For details, refer to Section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

6.4 Extended CSD Register

The Extended CSD register defines the device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to Section 7.4 of the JEDEC Standard Specification No.JESD84-B51.

6.5 RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-device communication after the device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all devices into the Stand-by State with CMD7.

6.6 DSR Register

The 16-bit driver stage register (DSR) is described in detail in Section 7.6 of the JEDEC Standard Specification No.JESD84-B51. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or the number of devices). The CSD register carries the information about the DSR register usage.

7. Package Dimensions

Table 7-1 Package Dimensions

Capacity	Package Dimensions	A1	A2	A
		Min	Nom	Max
8GB	11.5 x 13.0 x 1.0mm	0.17mm	0.60mm	1.0mm

Top View

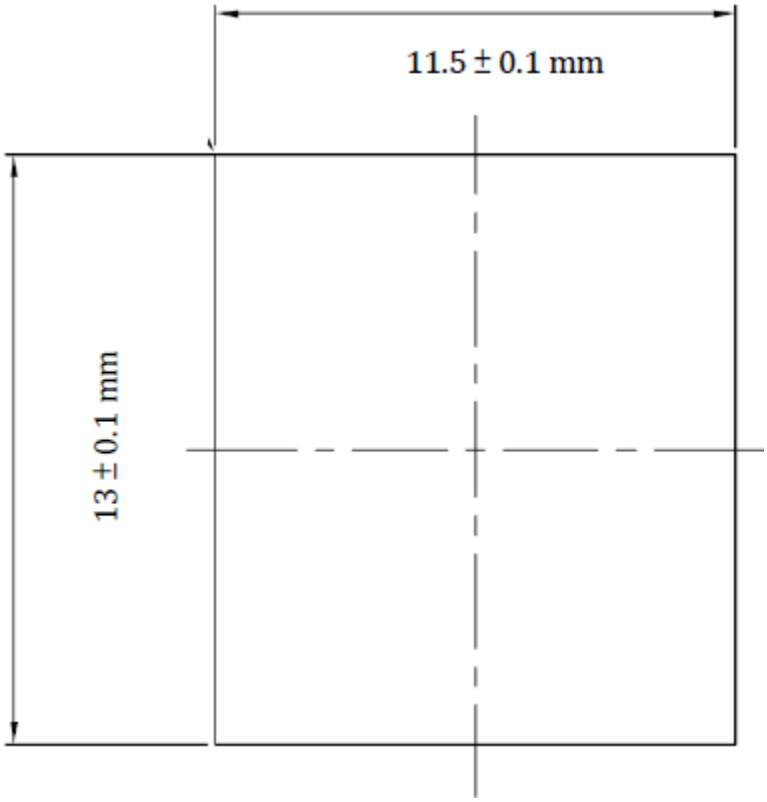


Figure 7-1 Top View

Side View

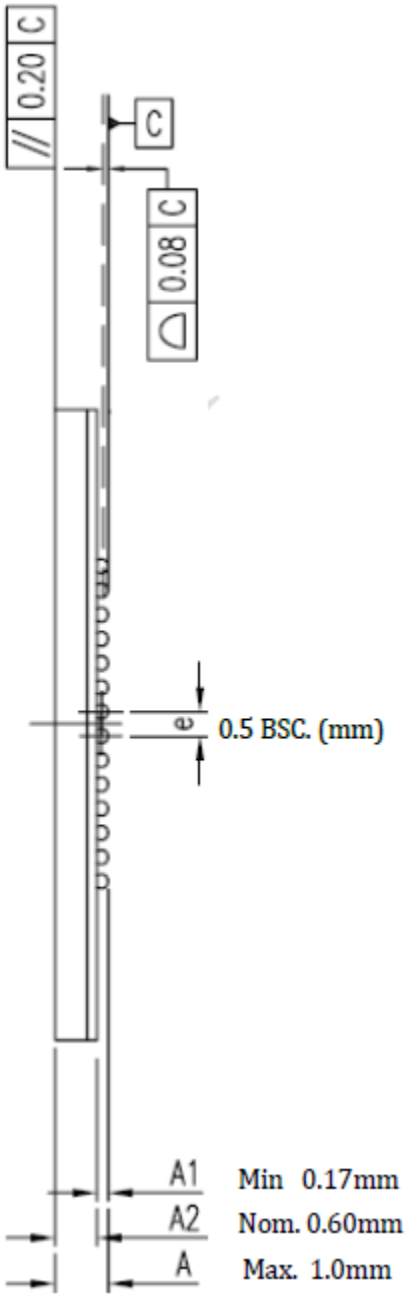
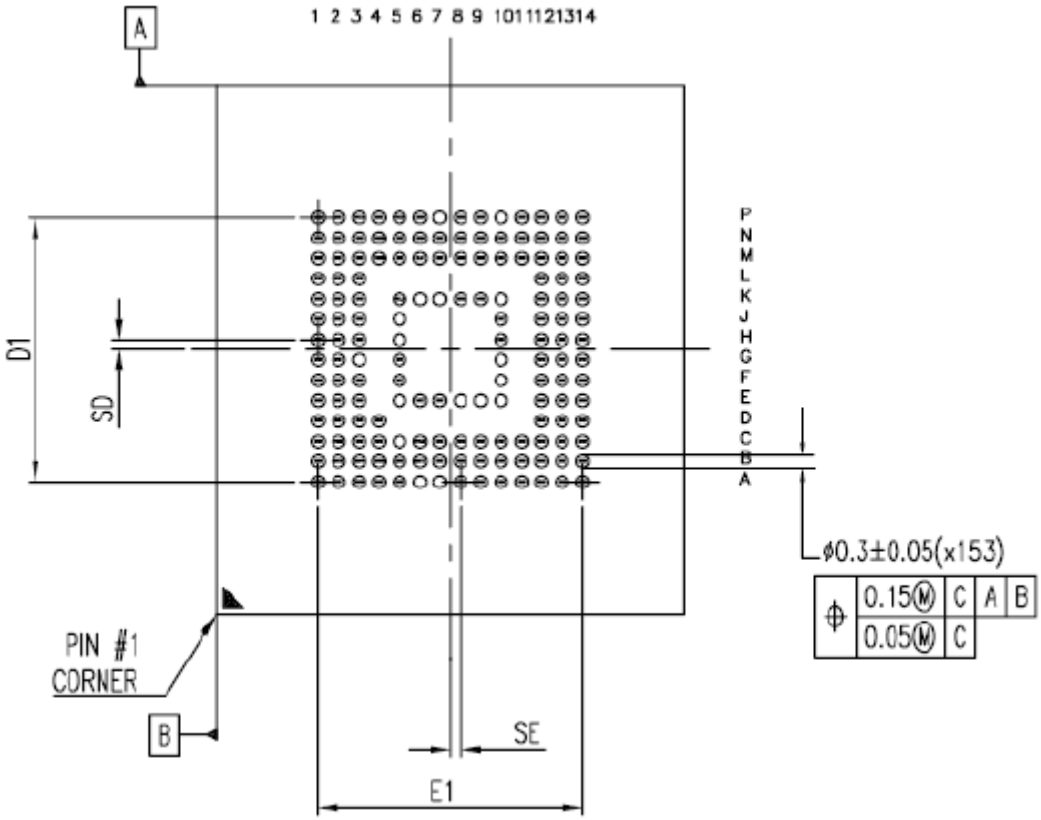


Figure 7-2 Side View

Bottom View



N	SE (MM)	SD (MN)	E1(MM)	D1(MM)	JEDEC(REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

Figure 7-3 Bottom View

8. Product Ordering Information

8.1 Product Code Designations

Apacer EM120 is available in different configurations and densities. See the chart below for a comprehensive list of options for the EM120 series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	M	6	.	1	2	2	D	A	A	.	0	0	1	0	1

Code 1-3 (Model Name)	EM120
Code 5-6 (Model/Solution)	Embedded MuiltiMedia Card
Code 7-8 (Product Capacity)	8GB
Code 9 (Flash Type & Product Temp)	2D MLC Standard Temperature
Code 10 (Product Spec)	eMMC
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	Standard Temperature

8.2 Valid Combinations

The following table lists the available model of the Apacer EM120 series which is in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Valid Combination
8GB	AM6.122DAA.00101

Revision History

Revision	Description	Date
0.1	Preliminary release	11/7/2023
1.0	Official release	11/9/2023
1.1	Added Tc to operating and storage temperatures at Product Features and Table 3-6	5/9/2024

Global Presence

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