# CMT8100, CMT8101 High Reliability Bidirectional I2C Isolators

## Features

- Up to 5000 Vrms insulation voltage
- I2C Clock rate: up to 2 MHz
- Power supply voltage: 2.5 V to 5.5 V
- AEC-Q100 Grade 1 qualified
- High CMTI: 150 kV/us
- Chip level ESD: HBM: ± 8 kV
- High system level EMC performance:
  - Enhanced system level ESD, EFT, surge immunity
- Isolation barrier life: > 60 years
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15 ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  - SOIC-8 narrow body
  - SOIC-16 wide body
  - SOW-8 wide body
- Safety regulatory approvals
  - UL recognition: up to 5000 Vrms for 1 minute per UL1577
  - CQC certification per GB4943.1-2011
  - CSA component notice 5A
  - DIN VDE V 0884-11:2017-01

## Applications

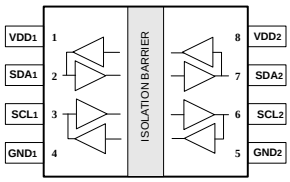
- Power over Ethernet
- Isolated I2C, SMBus, or PMBus interface
- I2C level shifting
- Battery management

## Description

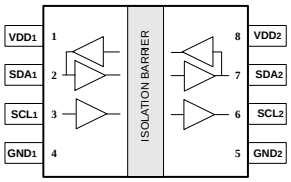
The (CMT8100, CMT8101) devices are high reliability bidirectional isolators that are compatible with I2C interface. The CMT810X devices are AEC-Q100 qualified. The CMT810X devices are safety certified by UL1577 supporting several insulation withstand voltages (3.75 kVrms, 5 kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The I2C clock of the CMT810X is up to 2 MHz, and the common-mode transient immunity (CMTI) is up to 150 kV/us. Wide supply voltage of the CMT810X devices supports to connect with most digital interfaces directly, easy to do the level shift. High system level EMC performance enhances device reliability and stability.

### Device Information

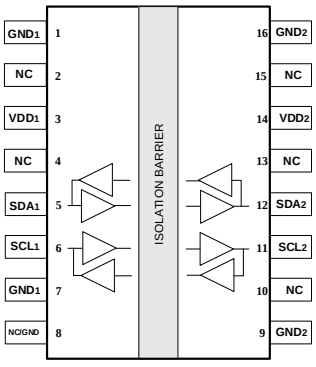
| Part No. | Package | Body Size (mm x mm) |
|---|---|---|
| CMT810X | NB(N) SOIC-8 | 5.0 x 4.0 |
| | WB(W) SOW-8 | 5.85 x 7.5 |
| | WB(W) SOIC-16 | 10.4 x 7.5 |
| Refer to section 8 for ordering information. | | |



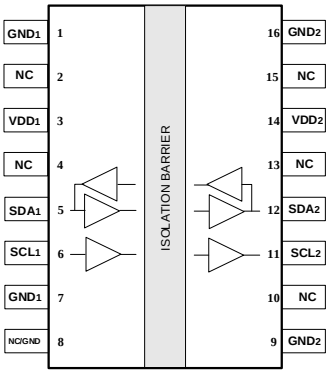

**CMT8100 NB SOIC-8/ WB SOW-8**




**CMT8101 NB SOIC-8/WB SOW-8**




**CMT8100 WB SOIC-16**




**CMT8101 WB SOIC-16**

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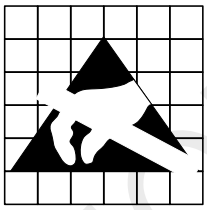
# 1 Absolute Maximum Ratings

**Table 1. Absolute Maximum Ratings[1]**

| Parameters | Symbol | Condition | Min. | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage | VDD1, VDD2 | | -0.5 | | 6.5 | V |
| Maximum input voltage | SDA1, SDA2, SCL1, SCL2 | | -0.4 | | VDD+0.4[1] | V |
| Maximum input pulse voltage | SDA1, SDA2, SCL1, SCL2 | Pulse width should be less than 100 ns, and the duty cycle should be less than 10% | -0.8 | | VDD+0.8 | V |
| Common-Mode transients | CMTI | | | | ±150 | kV/us |
| Output current | Io | | -15 | | 15 | mA |
| Maximum surge isolation voltage | VIOSM | | | | 5.3 | kV |
| Operating temperature | Topr | | -40 | | 125 | ℃ |
| Storage temperature | Tstg | | -40 | | 150 | ℃ |
| Electrostatic discharge | HBM | | | | ±8000 | V |
| | CDM | | | | ±2000 | V |

Notes:

[1]. The maximum voltage must not exceed 6.5 V.



**Caution!** ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

# 2 Pin Description

Narrow-body (N) 8-pin and wide-body (W) 16-pin SOIC / wide-body(W) 8-pin SOW packages are available for the series part number of CMT8100x, CMT8101x. The pin lists are shown as follows.

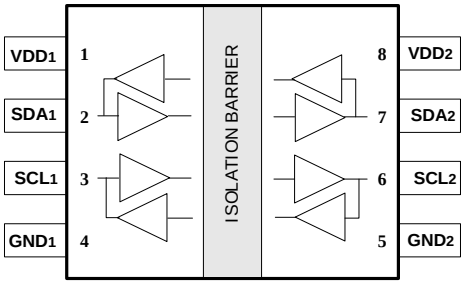



**Figure 1. CMT8100N Pin List of SOIC-8 NB/ SOW-8 WB**

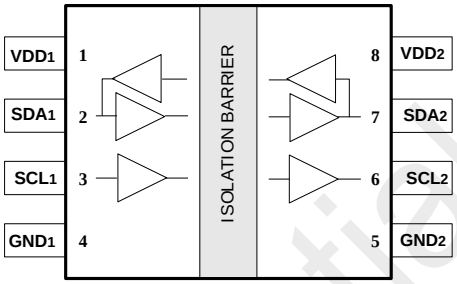



**Figure 2. CMT8101N Pin List of SOIC-8 NB/ SOW-8 WB**

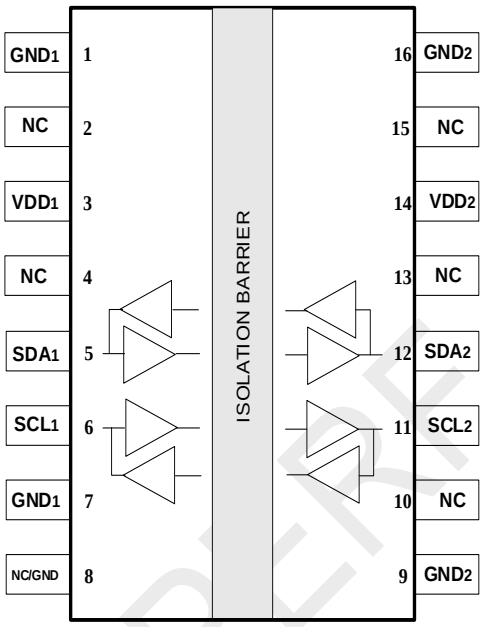



**Figure 3 CMT8100W SOIC-16 Pin List**

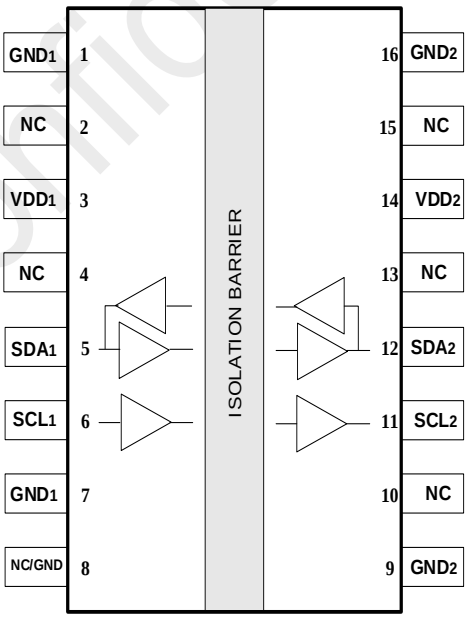



**Figure 4. CMT8101W SOIC-16 Pin List**

**Table 2. CMT8100N/8101N Pin Description**

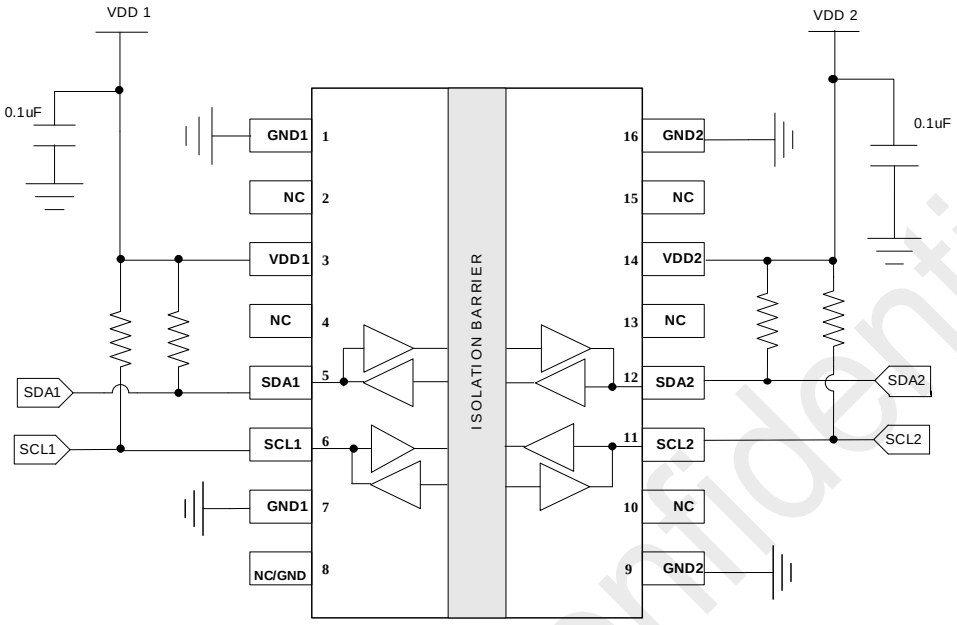
| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | $VDD_1$ | - | Power supply for isolator side 1. |
| 2 | $SDA_1$ | I/O | Serial data input /output, side 1 |
| 3 | $SCL_1$ | I/O | Serial clock input /output, side 1. |
| 4 | $GND_1$ | - | The ground reference for isolator side 1. |
| 5 | $GND_2$ | - | The ground reference for isolator side 2. |
| 6 | $SCL_2$ | I/O | Serial clock input /output, side 2. |
| 7 | $SDA_2$ | I/O | Serial data input /output, side 2 |
| 8 | $VDD_2$ | - | Power supply for isolator side 2. |

**Table 3 CMT8100W/8101W Pin Description**

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | $GND_1$ | - | Ground 1, the ground reference for Isolator Side 1 |
| 2 | NC | - | No Connection. |
| 3 | VDD1 | - | Power Supply for Isolator Side 1. |
| 4 | NC | - | No Connection. |
| 5 | $SDA_1$ | I/O | Serial data input /output, Side 1. |
| 6 | $SCL_1$ | I/O | Serial clock input /output, Side 1. |
| 7 | $GND_1$ | I/O | Ground 1, the ground reference for Isolator Side 1. |
| 8 | NC/GND | - | No Connection/ Connect to the Ground. |
| 9 | $GND_2$ | - | Ground 2, the ground reference for Isolator Side 2. |
| 10 | NC | - | No Connection. |
| 11 | $SCL_2$ | I/O | Serial clock input /output, Side 2. |
| 12 | $SDA_2$ | I/O | Serial data input /output, Side 2. |
| 13 | NC | - | No Connection. |
| 14 | $VDD_2$ | - | Power Supply for Isolator Side 2. |
| 15 | NC | - | No Connection. |
| 16 | $GND_2$ | - | Ground 2, the ground reference for Isolator Side 2. |

# 3 Typical Application

## 3.1 Typical Application Schematic




## 3.2 PCB Layout Guidelines

The CMT810X requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. The figure below shows the recommended PCB layout. Make sure the space under the chip should keep free from planes, traces, pads and via. The pull-up resistors are required for both side 1 and side 2 buses. And the value of the resistors depends on the number of I2C devices on the bus.

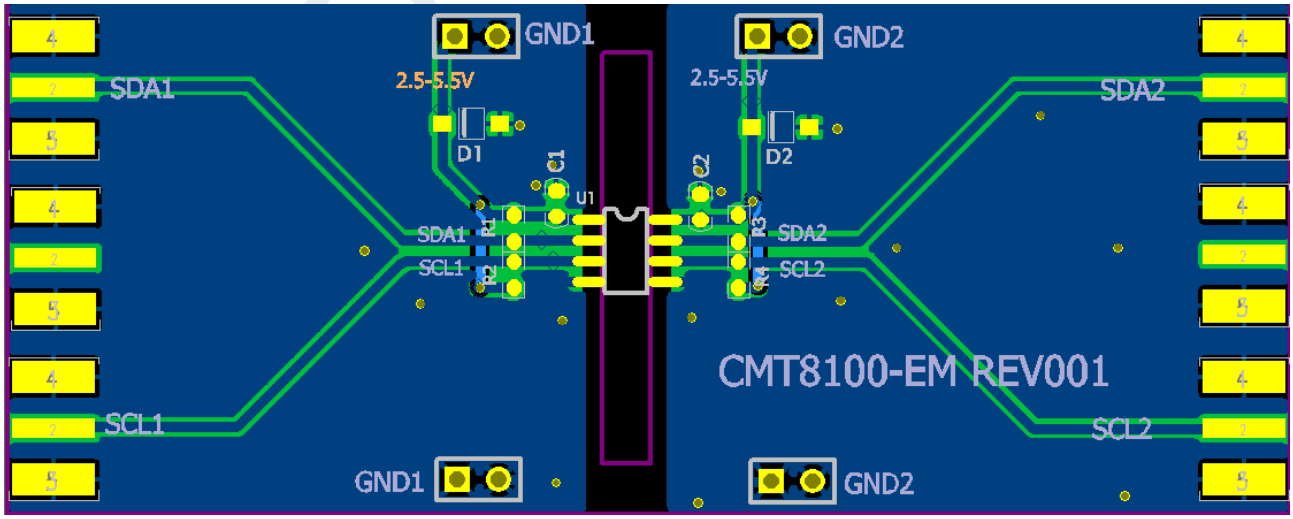



**Figure 5. Recommended PCB Layout**

# 4 Specifications

VDD1 = 2.5 ~ 5.5 V, VDD2 = 2.5 ~ 5.5 V, Ta = -40℃ to 125℃. Unless otherwise noted, typical values are at VDD1 = 5 V, VDD2 = 5 V, Ta = 25℃.

## 4.1 Electrical Characteristics

**Table 4. Electrical Characteristics**

| Parameters | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power on reset | $VDD_{POR}$ | POR threshold as during power-up | | 2.2 | | V |
| | $VDD_{HYS}$ | POR threshold Hysteresis | | 0.1 | | V |
| Start up time after POR | $t_{rbs}$ | | | 10 | | usec |
| Common mode transient immunity | CMTI | | ±100 | | ±150 | kV/us |
| **Side 1 logic level** | | | | | | |
| Input threshold | $V_{ILT1}$ | Input threshold at rising edge | 400 | | | mV |
| | $V_{IHT1}$ | | | | 600 | mV |
| | $V_{IT\_HYS1}$ | Input threshold hysteresis | | 100 | | mV |
| Low level output voltage | $V_{OL1}$ | $I_{OL}$ ≤ 4mA，$R_{PULL\ UP}$=1K | 650 | | 800 | mV |
| Low-level output voltage to high-level input voltage threshold difference | $\Delta V_{OIT1}$ | | 70 | | | mV |
| **Side 2 Logic Level** | | | | | | |
| Input threshold | $V_{ILT2}$ | Input threshold at rising edge | | 1.6 | | V |
| | $V_{IT\_HYS2}$ | Input threshold hysteresis | | 0.4 | | V |
| High level input voltage | $V_{IH2}$ | | 2.0 | | | V |
| Low level input voltage | $V_{IL2}$ | | | | 0.8 | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ ≤ 30mA | | | 0.5 | V |

## 4.2 Supply Current Characteristics with 5 V Supply

VDD1 = 5 V ± 10%, VDD2 = 5 V ± 10%, Ta = -40 ℃ to 125 ℃. Unless otherwise noted, Typical values are at VDD1 = 5 V, VDD2 = 5 V, Ta = 25 ℃.

**Table 5. Supply Current Characteristics with 5 V Supply**

| Parameter | Symbol | Condition | Min. | Typ. | Unit |
|---|---|---|---|---|---|
| **CMT8100** | | | | | |
| Supply current All Input 0 V | $I_{DD1}$(Q0) | | | 4.89 | mA |
| | $I_{DD2}$(Q0) | | | 3.99 | mA |

| Parameter | Symbol | Condition | Min. | Typ. | Unit |
|---|---|---|---|---|---|
| Supply current:<br>All Input at supply | $I_{DD1}$(Q1) | | | 2.56 | mA |
| | $I_{DD2}$(Q1) | | | 1.97 | mA |
| Supply current:<br>All Input with 2MHz, $C_L$=15pF | $I_{DD1}$(2M) | | | 3.72 | mA |
| | $I_{DD2}$(2M) | | | 2.64 | mA |
| CMT8101 | | | | | |
| Supply current<br>All Input 0V | $I_{DD1}$ | | | 4.19 | mA |
| | $I_{DD2}$ | | | 2.94 | mA |
| Supply current:<br>All Input at supply, | $I_{DD1}$ | | | 1.97 | mA |
| | $I_{DD2}$ | | | 1.92 | mA |
| Supply current:<br>All Input with 2MHz, $C_L$=15pF | $I_{DD1}$ | | | 2.63 | mA |
| | $I_{DD2}$ | | | 2.37 | mA |
| Clock rate | DR | | 0 | 2 | MHz |
| Propagation delay | $t_{PLH12}$ | See figure .6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 46.66 | ns |
| | $t_{PHL12}$ | See figure .6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 66.66 | ns |
| | $t_{PLH21}$ | See figure .6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 38.34 | ns |
| | $t_{PHL21}$ | See figure .6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 72.34 | ns |
| Pulse width distortion | $PWD_{12}$ | $\lvert t_{PHL12} - t_{PLH12} \rvert$ | | 34 | ns |
| | $PWD_{21}$ | $\lvert t_{PHL21} - t_{PLH21} \rvert$ | | 20 | ns |
| Falling time | $t_{f1}$ | $C_L$ = 30pF | | 17.1 | ns |
| | $t_{f2}$ | $C_L$ = 300pF | | 26.2 | ns |

## 4.3 Supply Current Characteristics with 3.3 V Supply

VDD1 = 3.3 V ± 10%, VDD2 = 5 V ± 10%, Ta = -40 ℃ to 125 ℃. Unless otherwise noted, Typical values are at VDD1 = 3.3 V, VDD2 = 3.3 V, Ta = 25 ℃.

**Table 6. Supply Current Characteristics with 3.3 V Supply**

| Parameter | Symbol | Condition | Min. | Typ. | Unit |
|---|---|---|---|---|---|
| CMT8100 | | | | | |
| Supply current<br>All Input 0V | $I_{DD1}$(Q0) | | | 4.87 | mA |
| | $I_{DD2}$(Q0) | | | 3.98 | mA |
| Supply current:<br>All Input at supply, | $I_{DD1}$(Q1) | | | 2.53 | mA |
| | $I_{DD2}$(Q1) | | | 1.95 | mA |
| Supply current:<br>All Input with 2MHz, $C_L$=15pF | $I_{DD1}$(2M) | | | 3.51 | mA |
| | $I_{DD2}$(2M) | | | 2.78 | mA |

| Parameter | Symbol | Condition | Min. | Typ. | Unit |
|---|---|---|---|---|---|
| **CMT8101** | | | | | |
| Supply current<br>All Input 0V | $I_{DD1}$ | | | 4.17 | mA |
| | $I_{DD2}$ | | | 2.93 | mA |
| Supply current:<br>All Input at supply, | $I_{DD1}$ | | | 1.94 | mA |
| | $I_{DD2}$ | | | 1.89 | mA |
| Supply current:<br>All Input with 2MHz, $C_L$=15pF | $I_{DD1}$ | | | 2.73 | mA |
| | $I_{DD2}$ | | | 2.29 | mA |
| Clock rate | DR | | 0 | 2 | MHz |
| Propagation delay | $t_{PLH12}$ | See figure 6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 46.66 | ns |
| | $t_{PHL12}$ | See figure 6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 66.66 | ns |
| | $t_{PLH21}$ | See figure 6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 38.34 | ns |
| | $t_{PHL21}$ | See figure 6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 72.34 | ns |
| Pulse width distortion | $PWD_{12}$ | $\lvert t_{PHL12} - t_{PLH12} \rvert$ | | 34 | ns |
| | $PWD_{21}$ | $\lvert t_{PHL21} - t_{PLH21} \rvert$ | | 20 | ns |
| Falling time | $t_{f1}$ | CL = 30pF | | 17.1 | ns |
| | $t_{f2}$ | CL = 300pF | | 26.2 | ns |

## 4.4 Supply Current Characteristics with 2.5 V Supply

VDD1 = 2.5 V ± 10%, VDD2 = 2.5 ± 10%, Ta = -40 ℃ to 125 ℃. Unless otherwise noted, Typical values are at VDD1 = 2.5 V, VDD2 = 2.5 V, Ta = 25 ℃.

**Table 7. Supply Current Characteristics with 2.5 V Supply**

| Parameter | Symbol | Condition | Min. | Typ. | Unit |
|---|---|---|---|---|---|
| **CMT8100** | | | | | |
| Supply current<br>All Input 0V | $I_{DD1}$(Q0) | | | 4.85 | mA |
| | $I_{DD2}$(Q0) | | | 3.96 | mA |
| Supply current:<br>All Input at supply, | $I_{DD1}$(Q1) | | | 2.53 | mA |
| | $I_{DD2}$(Q1) | | | 1.94 | mA |
| Supply current:<br>All Input with 2MHz, $C_L$=15pF | $I_{DD1}$(2M) | | | 3.43 | mA |
| | $I_{DD2}$(2M) | | | 2.85 | mA |
| **CMT8101** | | | | | |
| Supply current<br>All Input 0V | $I_{DD1}$ | | | 4.15 | mA |
| | $I_{DD2}$ | | | 2.91 | mA |
| Supply current: | $I_{DD1}$ | | | 1.97 | mA |

| Parameter | Symbol | Condition | Min. | Typ. | Unit |
|---|---|---|---|---|---|
| All Input at supply, | $I_{DD2}$ | | | 1.91 | mA |
| Supply current:<br>All Input with 2MHz, $C_L$=15pF | $I_{DD1}$ | | | 2.8 | mA |
| | $I_{DD2}$ | | | 2.25 | mA |
| Clock rate | DR | | 0 | 2 | MHz |
| Propagation delay | $t_{PLH12}$ | See figure 6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 47.5 | ns |
| | $t_{PHL12}$ | See figure .6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 89.5 | ns |
| | $t_{PLH21}$ | See figure .6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 40.84 | ns |
| | $t_{PHL21}$ | See figure .6,<br>R1=1500 Ω,<br>R2= 500Ω, no load | | 96.64 | ns |
| Pulse width distortion | $PWD_{12}$ | $\lvert t_{PHL12} - t_{PLH12} \rvert$ | | 42 | ns |
| | $PWD_{21}$ | $\lvert t_{PHL21} - t_{PLH21} \rvert$ | | 55.8 | ns |
| Falling time | $t_{f1}$ | $C_L$ = 30pF | | 31 | ns |
| | $t_{f2}$ | $C_L$ = 300pF | | 42 | ns |

## 4.5 Parameter Measurement Circuit Setup

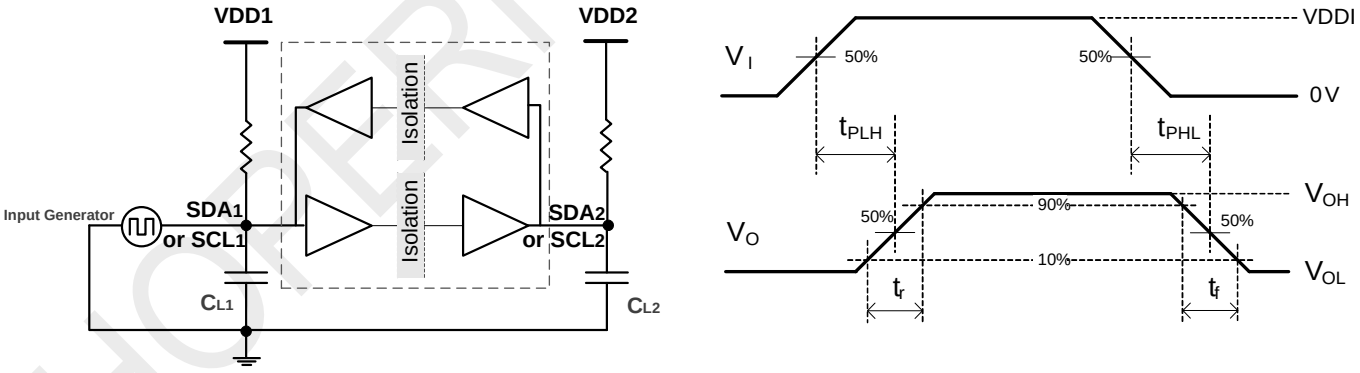



**Figure 6. Switching Characteristic Test Circuit and Voltage Waveforms**

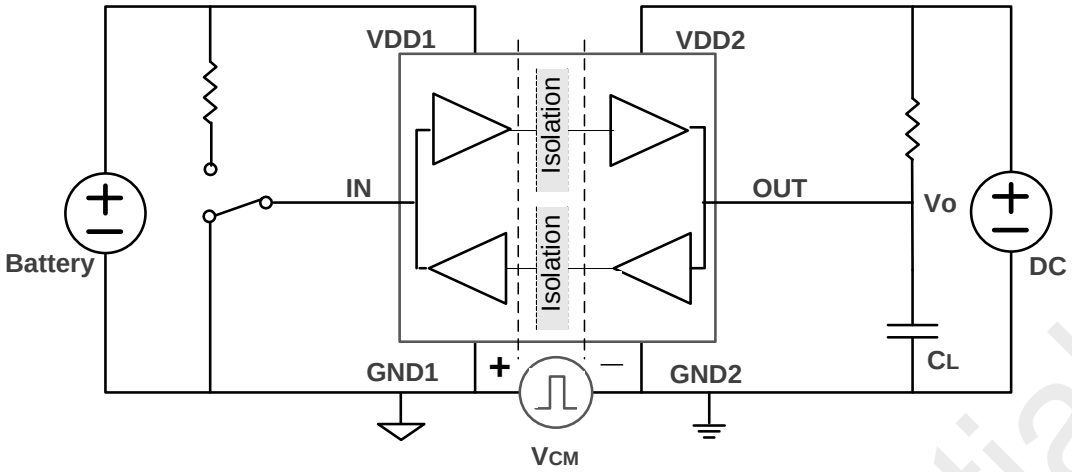



**Figure 7. Common-Mode Transient Immunity Test Circuit**

# 5 High Voltage Feature Specifications

## 5.1 Insulation and Safety Related Specifications

**Table 8. Insulation and Safety Related Specifications**

| Parameter | Symbol | Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | SOIC-8 | SOW-8/SOIC-16 | |
| Minimum External Air Gap (Clearance) | L(I01) | Shortest terminal-to-terminal distance through air | 4.0 | 8.0 | mm |
| Minimum External Tracking (Creepage) | L(I02) | Shortest terminal-to-terminal distance across the package surface | 4.0 | 8.0 | mm |
| Minimum internal gap | DTI | Distance through insulation | 25 | | um |
| Tracking Resistance (Comparative Tracking Index) | CTI | DIN EN 60112 (VDE 0303-11); IEC 60112 | >400 | | V |
| Material Group | | | 1 | | |

## 5.2 DIN VDE V 0884-11(VDE V 0884-11):2017-01 Insulation Characteristics

**Table 9. DIN VDE V 0884-11(VDE V 0884-11):2017-01 Insulation Characteristics**

| Description | Symbol | Test Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | SOIC-8 | SOW-8/SOIC-16 | |
| Installation classification per DIN VDE 0110 | | | | | |
| For rated mains voltage ≤ 150 $V_{rms}$ | | | I to IV | I to IV | |
| For rated mains voltage ≤ 300 $V_{rms}$ | | | I to III | I to IV | |
| For rated mains voltage ≤ 400 $V_{rms}$ | | | I to III | I to IV | |
| Climatic classification | | | 10/105/21 | 10/105/21 | |

| | | | | | |
|---|---|---|---|---|---|
| Pollution degree per DIN VDE 0110, table 1 | | | 2 | 2 | |
| Maximum repetitive isolation voltage | $V_{IORM}$ | | 565 | 849 | Vpeak |
| Input to output test voltage, method B1 | $V_{pd\ (m)}$ | V IORM × 1. 5 = $V_{pd\ (m)}$, 100% production test, $t_{ini}$ = $t_m$ = 1 sec, partial discharge < 5 pC | 847 | 1273 | Vpeak |
| Input to output test voltage, method A | | | | | |
| After environmental tests subgroup 1 | $V_{pd\ (m)}$ | $V_{IORM}$ × 1.2 = $V_{pd\ (m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5 pC | 678 | 1019 | Vpeak |
| After Input and /or safety test subgroup 2 and subgroup 3 | $V_{pd\ (m)}$ | $V_{IORM}$ × 1.2= $V_{pd\ (m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5 pC | 678 | 1019 | Vpeak |
| Maximum transient isolation voltage | $V_{IOTM}$ | t = 60 sec | 5300 | 7000 | Vpeak |
| Maximum surge isolation voltage | $V_{IOSM}$ | Test method per IEC 60065,1.2/50us waveform, VTEST=1.3×VIOSM | 5300 | 7000 | Vpeak |
| Isolation resistance | $R_{IO}$ | $V_{IO}$ =500V | >$10^9$ | >$10^9$ | Ω |
| UL1577 | | | | | |
| Isolation withstand voltage | $V_{ISO}$ | $V_{TEST}$ = $V_{ISO}$, t = 60 s (certified); $V_{TEST}$ = 1.2 × $V_{ISO}$, t = 1 s (100% mass production) | 3750 | 5000 | Vrms |
| Isolation capacitance | $C_{IO}$ | f = 1MHz | 0.6 | 0.6 | pF |
| Input capacitance | $C_I$ | | 2 | 2 | pF |
| Total power dissipation at 25℃ | Ps | | | 1499 | mW |
| Case temperature | Ts | | 150 | 150 | ℃ |

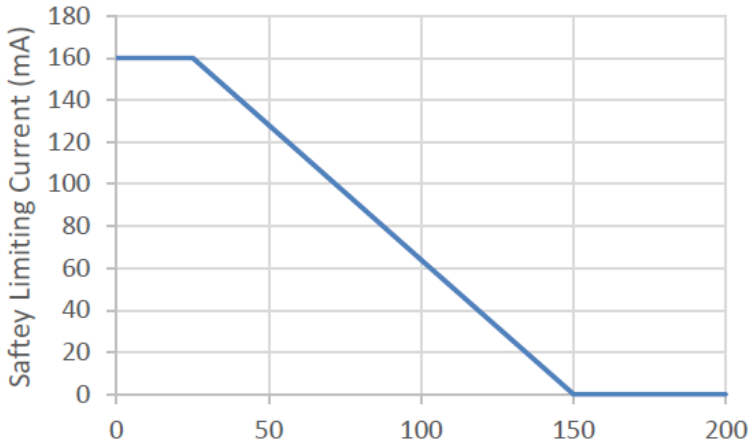



**Figure 8. CMT8100N/8101N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11**

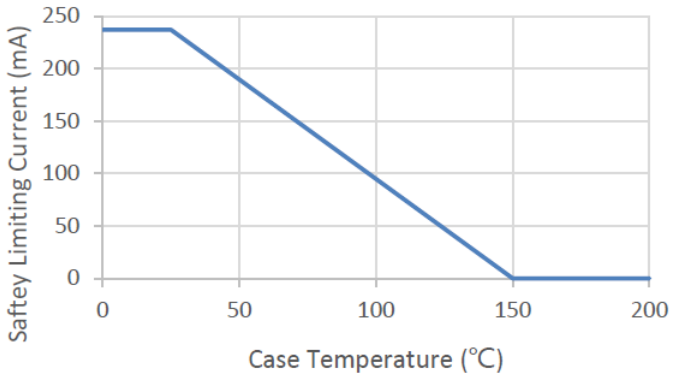



**Figure 9. CMT8100W/8101W Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11**

## 5.3 Regulation Information

The CMT8100N/CMT8101N are approved by the organizations listed in table below.

**Table 10. CMT8100N / CMT8101N Regulation Conformation**

| CUL | CSA | VDE | CQC |
|---|---|---|---|
| UL 1577 Component Recognition Program [1]<br>(Applying) | Approved under CSA Component Acceptance Notice 5A<br>(Applying) | DIN VDE V 0884- 11(VDE V 0884-11):2017-01[2]<br>(Applying) | Certified by CQC11-471543-2012<br>GB4943.1-2011 |
| File (pending) | File (pending) | File (pending) | File:<br>CQC23001382478 |
| [1]. In accordance with UL 1577, each CMT8100N/ CMT 8101N is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.<br>[2]. In accordance with DIN VDE V 0884-11, each CMT8100N/ CMT 8101N is proof tested by applying an insulation test voltage ≥ 847 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11. | | | |

The CMT8100W/CMT8101W are approved by the organizations listed in table below.

**Table 11. CMT8100W / CMT8101 Regulation Conformation**

| CUL | CSA | VDE | CQC |
|---|---|---|---|
| UL 1577 Component Recognition Program[1]<br>(Applying) | Approved under CSA Component Acceptance Notice 5A<br>(Applying) | DIN VDE V 0884- 11(VDE V 0884-11):2017-012<br>(Applying) | Certified by CQC11-471543-2012<br>GB4943.1-2011 |
| File (pending) | File (pending) | File (pending) | File:<br>CQC23001385762 |
| [1]. In accordance with UL 1577, each CMT 8100W/ CMT 8101W is proof tested by applying an insulation test voltage ⩾ 6000 V rms for 1 sec.<br>[2]. In accordance with DIN VDE V 0884-11, each CMT 8100W/ CMT 8101W is proof tested by applying an insulation test voltage ⩾ 1273 V peak for 1 sec (partial discharge detection limit = 5 pC ). The * marking branded on the component designates DIN VDE V 0884-11 approval. | | | |

# 6 Function Description

## 6.1 Function Overview

The CMT810X is a bidirectional isolator based on a capacitive isolation barrier technique. The CMT810X devices are compatible with I2C interface. Internally, the I2C interface is split into two unidirectional channels communicating in opposite directions via a dedicate capacitive isolation channel for each. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The CMT8100 devices are high reliability dual-channel bidirectional isolators for clock and data lines while CMT8101 has a bidirectional data and a unidirectional clock channel. The CMT8100 is suitable for multi-master application while CMT8101 is useful in a single master application.

The side 2 logic levels of CMT810X are standard I2C value, and the maximum load for side 2 is $\leqslant$ 400 pF. So multiple CMT810X devices connected to a bus by their Side 2 pins can communicate with each other and with other I2C compatible devices.

The side 1 logic levels of CMT810X are not standard value. The output low level of CMT810X is 650mV, while low-level output voltage to high-level input voltage threshold is 50 mV. This prevents an output logic low at Side 1 being transmitted back to Side 2 and pulling down the I2C bus.

The CMT810X devices are AEC-Q100 qualified. The CMT810X device is safety certified by UL1577 support several insulation withstand voltages (3.75 kVrms, 5 kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The I2C clock of the CMT810X is up to 2 MHz, and the common-mode transient immunity (CMTI) is up to 150 kV/us. Wide supply voltage of the CMT810X device supports to connect with most digital interfaces directly, easy to do the level shift. High system level EMC performance enhances reliability and stability.

The table below shows the functional status of CMT810X. The CMT810X is high impedance output when VDDIN is unready and VDDOUT is ready as shown in the table below.

**Table 12. Output Status vs. Power Status**

| Input | VDD1 Status | VDD2 Status | Output | Comment |
|---|---|---|---|---|
| H | Ready | Ready | Z | Normal operation. |
| L | Ready | Ready | L | |
| X | Unready | Ready | Z | The output follows the same status with the input within 60 us after input side VDD1 is powered on. |
| X | Ready | Unready | X | The output follows the same status with the input within 60 us after output side VDD2 is powered on. |

# 7 Packaging Information

The packaging information of the CMT810X is shown in the figures below.

## 7.1 CMT8100N/CMT8101N Narrow Body SOIC-8 Package

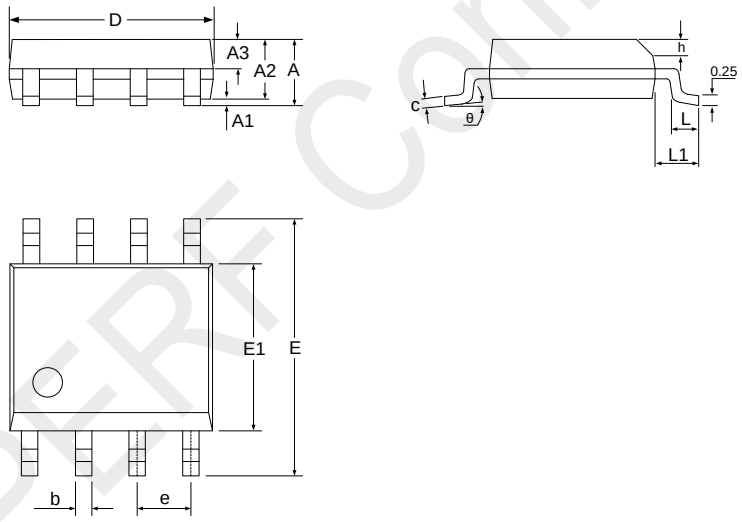



**Figure 10. Narrow Body SOIC-8 Packaging**

**Table 13. Narrow Body SOIC-8 Packaging Scale**

| Symbol | Size (mm) | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.75 |
| A1 | 0.10 | 0.18 | 0.25 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.33 | 0.42 | 0.51 |
| c | 0.17 | 0.21 | 0.25 |
| D | 4.80 | 5.00 | 5.20 |
| E | 5.80 | 6.00 | 6.20 |

| Symbol | Size (mm) | | |
|---|---|---|---|
| | Min | Typ | Max |
| E1 | 3.90 | 4.00 | 4.10 |
| e | 1.27 BSC | | |
| h | 0.25 | - | 0.50 |
| L | 0.40 | 0.60 | 0.80 |
| L1 | 1.05 BSC | | |
| θ | 0 | - | 8° |

## 7.2 CMT8100W/CMT8101W Wide Body SOIC-16 Package

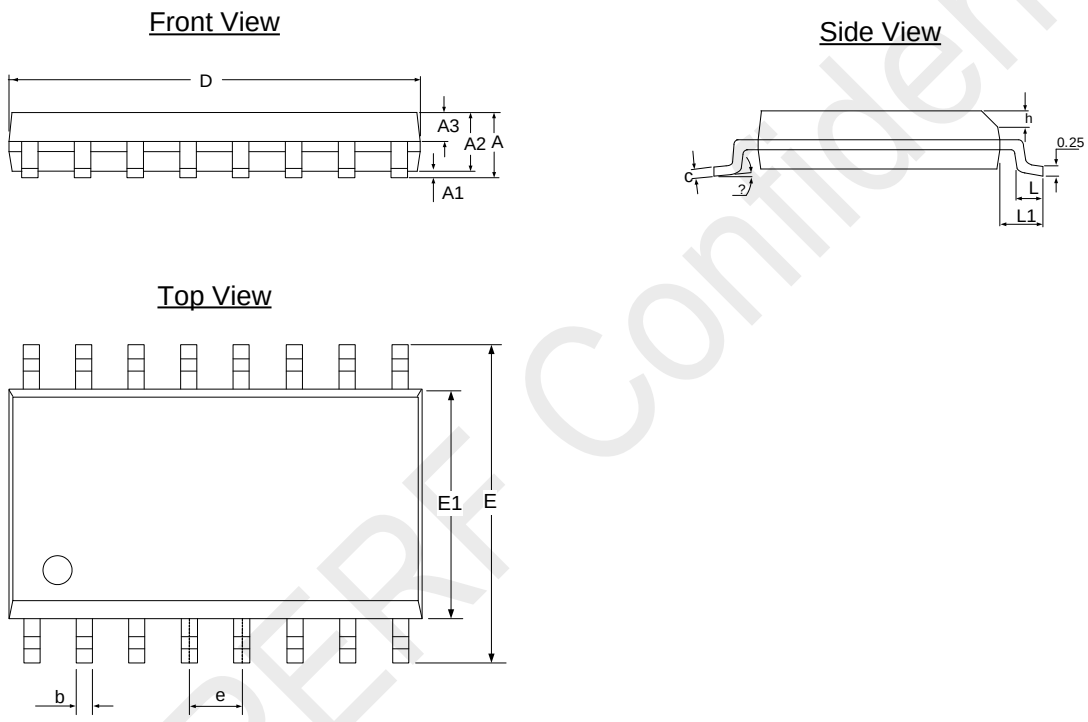



**Figure 11. Wide Body SOIC-16 Packaging**

**Table 14. Wide Body SOIC-16 Packaging Scale**

| Symbol | Scale (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 2.65 |
| A1 | 0.10 | 0.20 | 0.30 |
| A2 | 2.25 | 2.30 | 2.35 |
| A3 | 1.00 | 1.05 | 1.10 |
| b | 0.35 | 0.37 | 0.43 |
| c | 0.15 | 0.20 | 0.30 |
| D | 10.30 | 10.40 | 10.50 |
| E | 10.10 | 10.30 | 10.50 |

| Symbol | Scale (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.14 | 1.27 | 1.40 |
| L | 0.65 | 0.70 | 0.85 |
| L1 | | 1.40 | |
| θ | 0 | - | 8° |

## 7.3 CMT8100WH/CMT8101WH SOW-8 Package

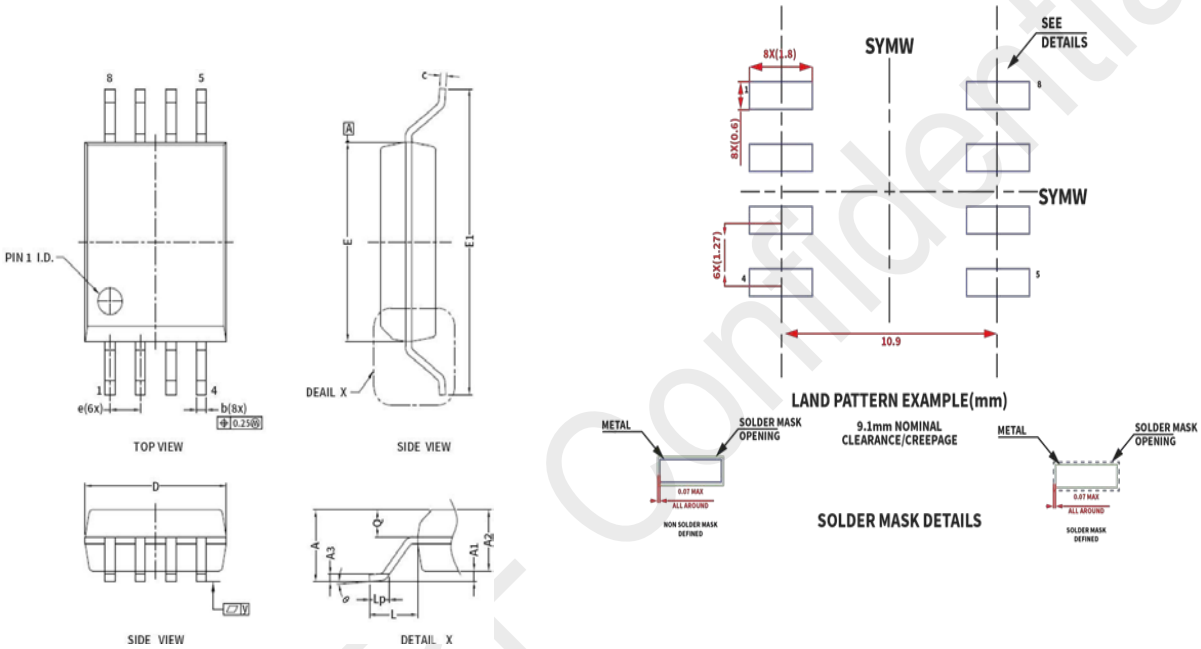



**Figure 12. CMT810X SOW-8 WB Packaging**

**Table 15. CMT810X SOW-8 WB Packaging Scale**

| Symbol | Scale (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 2.80 |
| A1 | 0.36 | - | 0.46 |
| A2 | 2.20 | 2.30 | 2.40 |
| A3 | - | 0.25 | - |
| Q | 0.97 | 1.02 | 1.07 |
| b | 0.31 | 0.41 | 0.51 |
| c | 0.13 | - | 0.33 |
| D | 5.75 | 5.85 | 5.95 |
| E | 7.40 | 7.50 | 7.60 |
| E1 | 11.25 | 11.50 | 11.75 |
| e | | 1.27 bsc | |

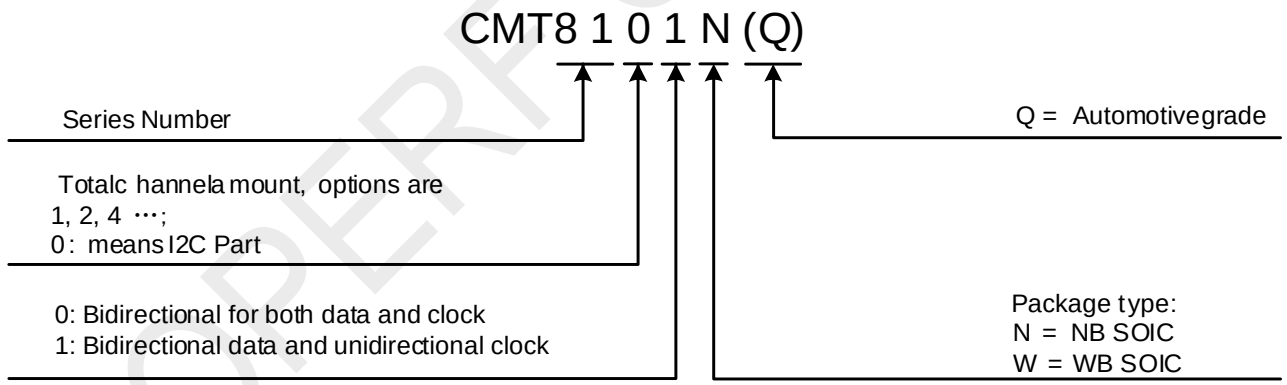
| Symbol | Scale (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| L | 2.00 bsc | | |
| Lp | 0.50 | - | 1.00 |
| Y | - | 0.10 | - |
| θ | 0 | - | 8° |

# 8 Ordering Information

**Table 16. Part Number Information List**

| Part No. | Isolation Rating(kV) | MOQ | Numbers of input channel | Max Clock Rate (MHz) | Temperature | Automotive | Package |
|---|---|---|---|---|---|---|---|
| CMT8100N | 3.75 | 3000 | 2 | 2 | -40 to 125℃ | NO | NB SOIC8 |
| CMT8101N | 3.75 | 3000 | 2 | 2 | -40 to 125℃ | NO | NB SOIC8 |
| CMT8100WH | 5 | 1000 | 2 | 2 | -40 to 125℃ | NO | WB SOW8 |
| CMT8101WH | 5 | 1000 | 2 | 2 | -40 to 125℃ | NO | WB SOW8 |
| CMT8100W | 5 | 1000 | 2 | 2 | -40 to 125℃ | NO | WB SOIC16 |
| CMT8101W | 5 | 1000 | 2 | 2 | -40 to 125℃ | NO | WB SOIC16 |

**Part Number Naming Rule:**

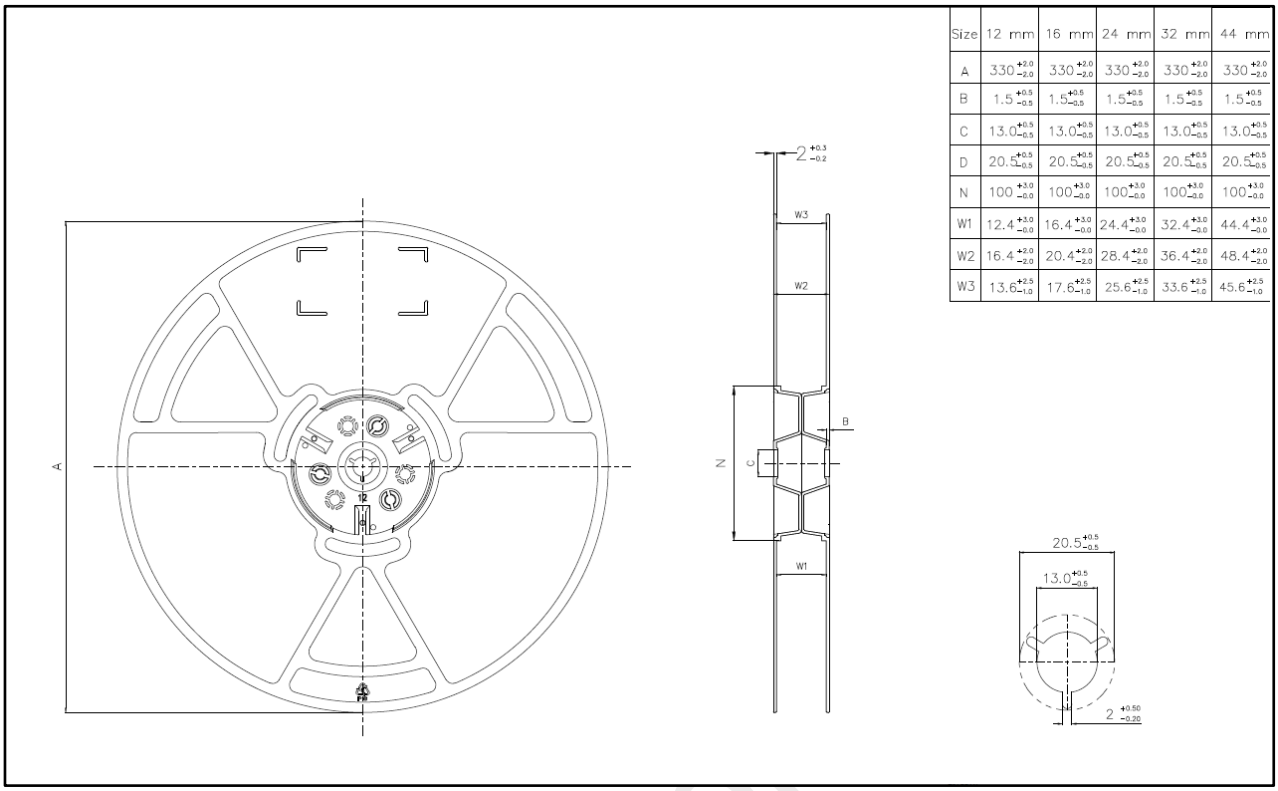





Please visit www.hoperf.com for more product/product line information.

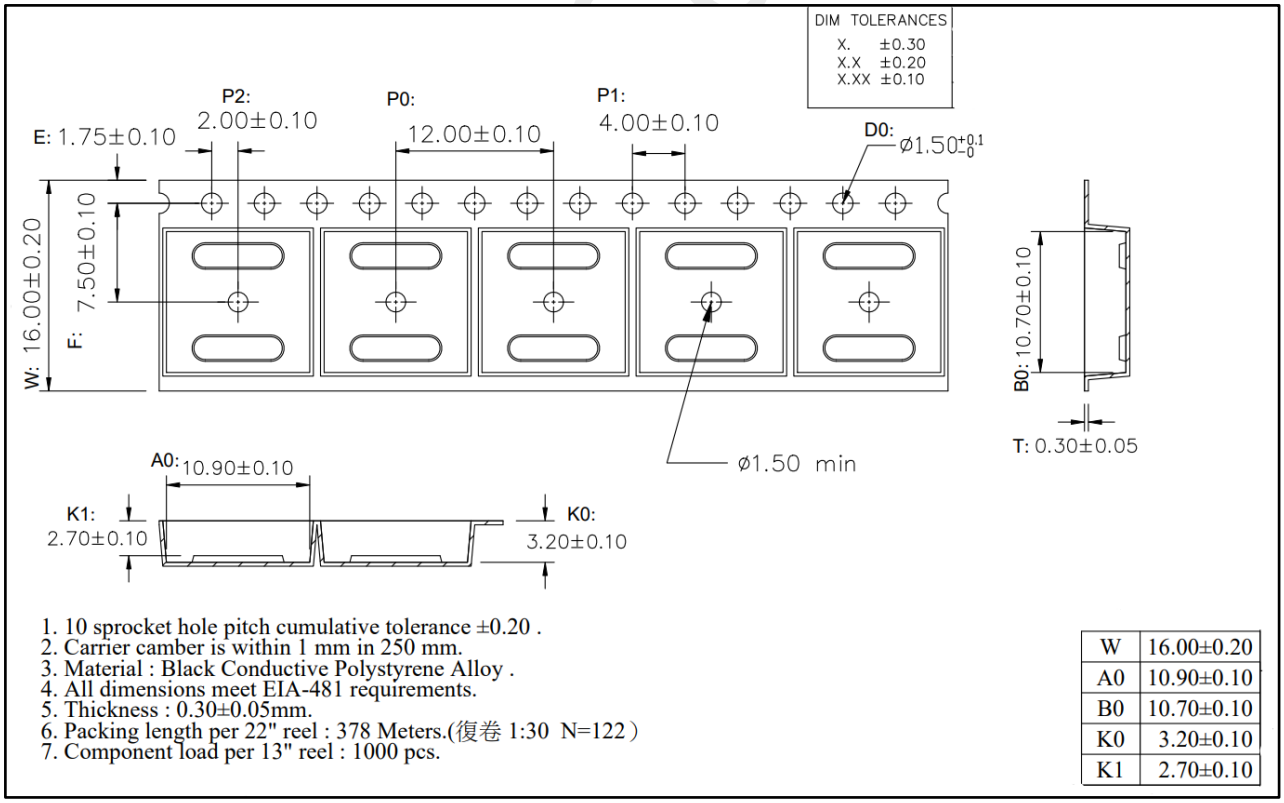
Please contact sales@hoperf.comor your local sales representative for sales or pricing requirements.

# 9 Tape and Reel Information




| Size | 12 mm | 16 mm | 24 mm | 32 mm | 44 mm |
|---|---|---|---|---|---|
| A | 330 +2.0 -2.0 | 330 +2.0 -2.0 | 330 +2.0 -2.0 | 330 +2.0 -2.0 | 330 +2.0 -2.0 |
| B | 1.5 +0.5 -0.5 | 1.5 +0.5 -0.5 | 1.5 +0.5 -0.5 | 1.5 +0.5 -0.5 | 1.5 +0.5 -0.5 |
| C | 13.0 +0.5 -0.5 | 13.0 +0.5 -0.5 | 13.0 +0.5 -0.5 | 13.0 +0.5 -0.5 | 13.0 +0.5 -0.5 |
| D | 20.5 +0.5 -0.5 | 20.5 +0.5 -0.5 | 20.5 +0.5 -0.5 | 20.5 +0.5 -0.5 | 20.5 +0.5 -0.5 |
| N | 100 +3.0 -0.0 | 100 +3.0 -0.0 | 100 +3.0 -0.0 | 100 +3.0 -0.0 | 100 +3.0 -0.0 |
| W1 | 12.4 +3.0 -0.0 | 16.4 +3.0 -0.0 | 24.4 +3.0 -0.0 | 32.4 +3.0 -0.0 | 44.4 +3.0 -0.0 |
| W2 | 16.4 +2.0 -2.0 | 20.4 +2.0 -2.0 | 28.4 +2.0 -2.0 | 36.4 +2.0 -2.0 | 48.4 +2.0 -2.0 |
| W3 | 13.6 +2.5 -1.0 | 17.6 +2.5 -1.0 | 25.6 +2.5 -1.0 | 33.6 +2.5 -1.0 | 45.6 +2.5 -1.0 |

**Figure 13. CMT810X WB SOIC-16 Tape and Reel Information**




| | |
|---|---|
| W | 16.00±0.20 |
| A0 | 10.90±0.10 |
| B0 | 10.70±0.10 |
| K0 | 3.20±0.10 |
| K1 | 2.70±0.10 |

**Figure 14. CMT810X WB SOIC-16 Tape and Reel Information**

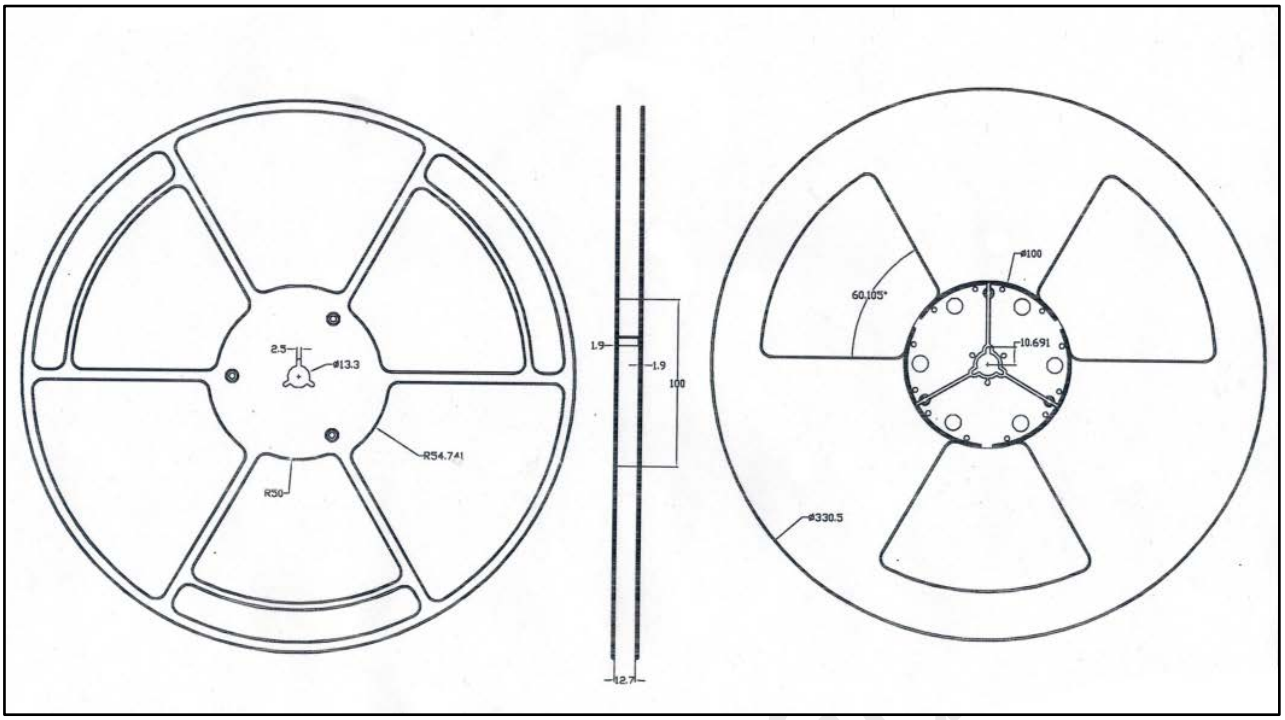
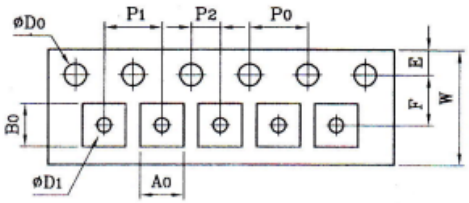



**Figure 15. CMT810X NB SOIC-8 Tape and Reel Information**

產品尺寸規格 (UNIT:mm)

| 規格 | W | P1 | E | F | D0 | D1 | P0 | P2 | 10P0 |
|---|---|---|---|---|---|---|---|---|---|
| 尺寸 | 12.0 $^{+0.30}_{-0.10}$ | 8.0±0.1 | 1.75±0.1 | 5.5±0.05 | 1.5 $^{+0.10}_{-0}$ | 1.5 $^{+0.25}_{-0}$ | 4±0.1 | 2±0.05 | 40±0.2 |
| 規格 | A0 | A1 | B0 | B1 | K0 | K1 | T | | |
| 尺寸 | 6.40±0.10 | | 5.40±0.10 | | 2.10±0.10 | | 0.25±0.03 | | |



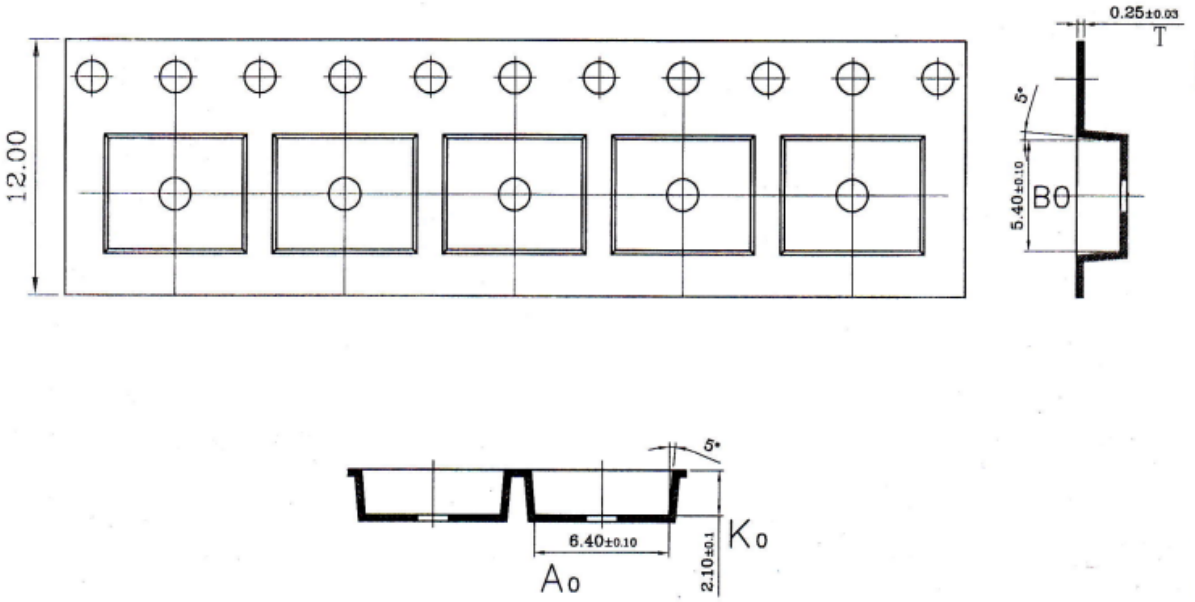




**Figure 16. CMT810X NB SOIC-8 Tape and Reel Information**

# 10 Revise History

**Table 17. Revise History Records**

| Version No. | Chapter | Description | Date |
|---|---|---|---|
| 0.1 | All | Initial version | 2021/11/02 |
| 0.2 | 4 | Update the supply current characteristic data | 2022/08/31 |
| 0.3 | All | Revise the NB SOIC-8 package size | 2022/10/24 |
| 0.4 | 8 | Update silver print information | 2023/03/29 |
| | 10 | Added tape information | |
| 0.5 | All | Delete the silver printing section | 2023/04/20 |
| | | Added the CQC cercificate number | |
| 0.6 | All | Revise the 8th pin of NC to NC/GND in package SOIC16. | 2023/09/11 |
| 0.7 | All | Added package of SOW8 WB | 2024/5/21 |

# 11 Contacts

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