SPECIFICATIONS FOR OLED MODULE

MODEL NO.
BL2004AM-WRNJU20C$
VER.01

FOR MESSRS:

_____

ON DATE OF:

_____

APPROVED BY:

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BOLYMIN, INC.
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History of Version

Version	Contents	Date	Note
01	NEW VERSION	2019/12/9	SPEC.

C O N T E N T S

1. Numbering System

B	L	2004	AM	-	W	R	N	J	U	20C	$	
0	1	2	3		4	5	6	7	8	9	10	11

0	Bolymin	B			
1	Module Type	L	OLED		
2	Format	2004	20 character type,4lines		
3	Version No.	AM			
	-				
4	LCD Color	L	OLED/Green	E	OLED/Yellow
		W	OLED/White	R	OLED/RED
		K	OLED/BLUE		
5	LCD Type	R	Positive/reflective		
6	Backlight type/color	N	No backlight		
7	CGRAM Font	J	English/Japanese Font	E	English/European Font
		B	English/Japanese/European	C	English/Cyrillic Font
8	View Angle /Operation Temperature	U	6:00/Ultra wide Temperature	H	6:00 /Wide Temperature
9	Special Code	3	3 voltage logic power supply	N	Positive voltage for LCD
		20K	RS 232 I/F	20C	I2C I/F
		20I	SPI I/F	68J	6800 mode,8-bits
		68K	6800 mode,4-bits	80J	8080 mode,8-bits
		80K	8080 mode,4-bits		
10	RoHS	$			
11	Customer Code	00 0 ~ 99 0 、AA 0 ~ ZZ 0			

2.General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of Characters	20 characters× 4 Lines	dots
Module dimension (L*W*H)	98.0 x 60.0 x 13.1	mm
View area	76.0 x 24.2	mm
Active area	70.42 x 20.82	mm
Dot size	0.57 x 0.57	mm
Dot pitch	0.60 x 0.60	mm
Character size (L x W)	2.97 x 4.77	mm
Character pitch (L x W)	3.55 x 5.35	mm

(2) Controller IC: Compatible with PT0066
IC Equivalent (compatible) HD44780, KS0066 , SPLC780 , ST7066 , AIP31066

3.Absolute Maximum Ratings

Item	Symbol	Condition	Min	Typ.	Max	Unit
Operating Temperature	TOP		-40	---	+80	℃
Storage Temperature	TST		-40	---	+90	℃
Supply Voltage(Logic)	VDD		-0.3	---	5.5	V
Input Voltage	VI		-0.3	---	5.5	V
Operating life time		80cd/m²	---	70000	---	Hrs

Note 1: All the above voltages are on the basis of “VSS = 0V”.
Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur.
Note 3:Ta = 25℃, 25% Checkerboard.
Software configuration follows section actual application example Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions..

4.Electrical Characteristics

(Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (VDD)	VDD	—	2.8	5.0	5.3	V
Input High Vol	V_{IH}	—	$0.7V_{DD}$	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	$0.3V_{DD}$	V
Output High Vol	V_{OH}	—	$0.7V_{DD}$	—	V_{DD}	V
Output Low Vol.	V_{OL}	—	—	—	0.3VDD	V
Supply Current (*)	IDD	—	—	40	—	mA

Note : VDD=5.0V, 25% Display Area Turn on 100 cd/m2.
When random texts pattern is running, averagely, about 1/4 of pixels will be on.

5.Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	—	Free	—	deg
Dark Room contrast	>10000:1			—
CIE x,y (Color: White)	(0.25,0.27)	(0.29,0.31)	(0.33,0.35)	
Brightness	—	100	—	cd/m2

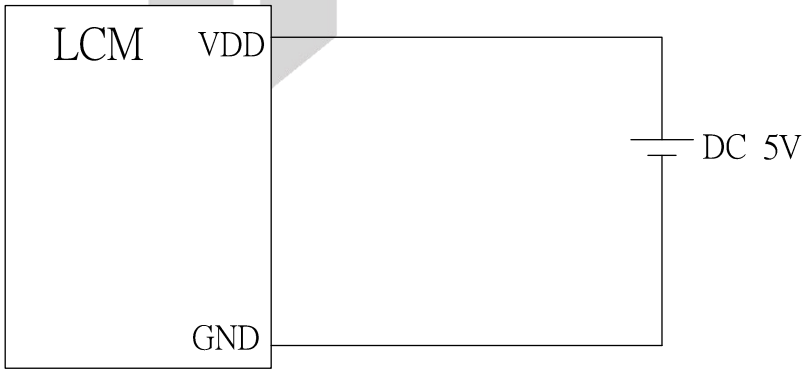
6.Interface Pin Function

1	GND	0V	Ground
2	VDD	5.0V	Supply Voltage for logic**.**
3	NC	-	No connection
4	SA0	H/L	Serves as SA0 to distinguish the different address of LCM driver.
5	R/W	H/L	Tie LOW
6	E	H→L	Tie LOW
7	SCL	H/L	Serial clock input
8	SDA	H/L	Serial data input
9	NC	-	No connection.
10	NC	-	No connection.
11	NC	-	No connection.
12	NC	-	No connection.
13	NC	-	No connection.
14	NC	-	No connection.
15	NC	-	No connection
16	NC	-	No connection

※I2C Series Interface is Default

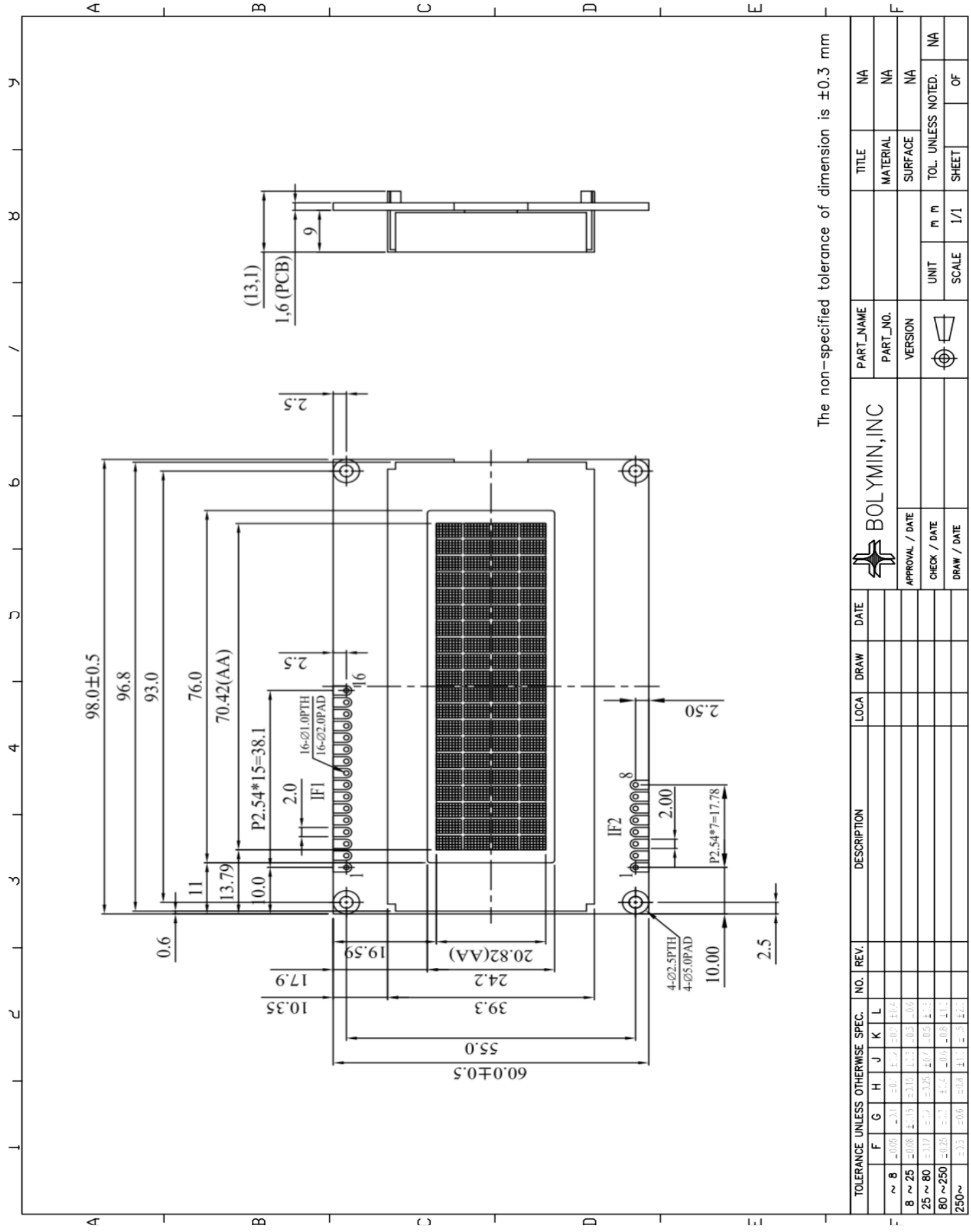
7.Power supply for LCD Module

＊LCM operating on "DC 5.0V " input with built-in positive voltage



8.Drawing& Block Diagram

8.1 Drawing

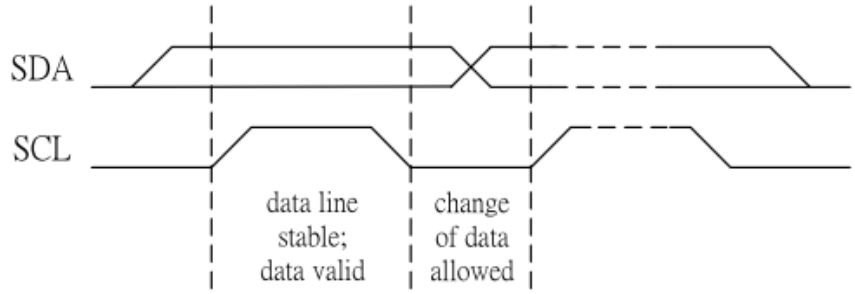


9. Controller Data

9.1 I2C-bus Interface

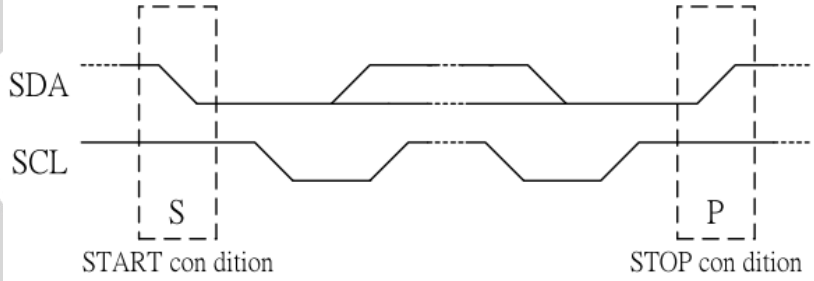
BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated below.



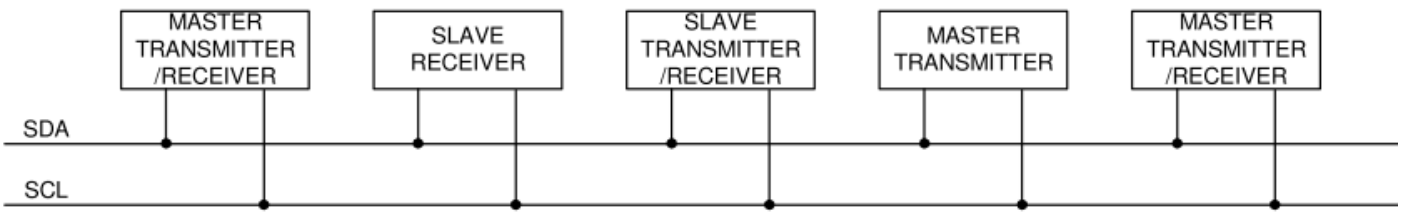
START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated below.

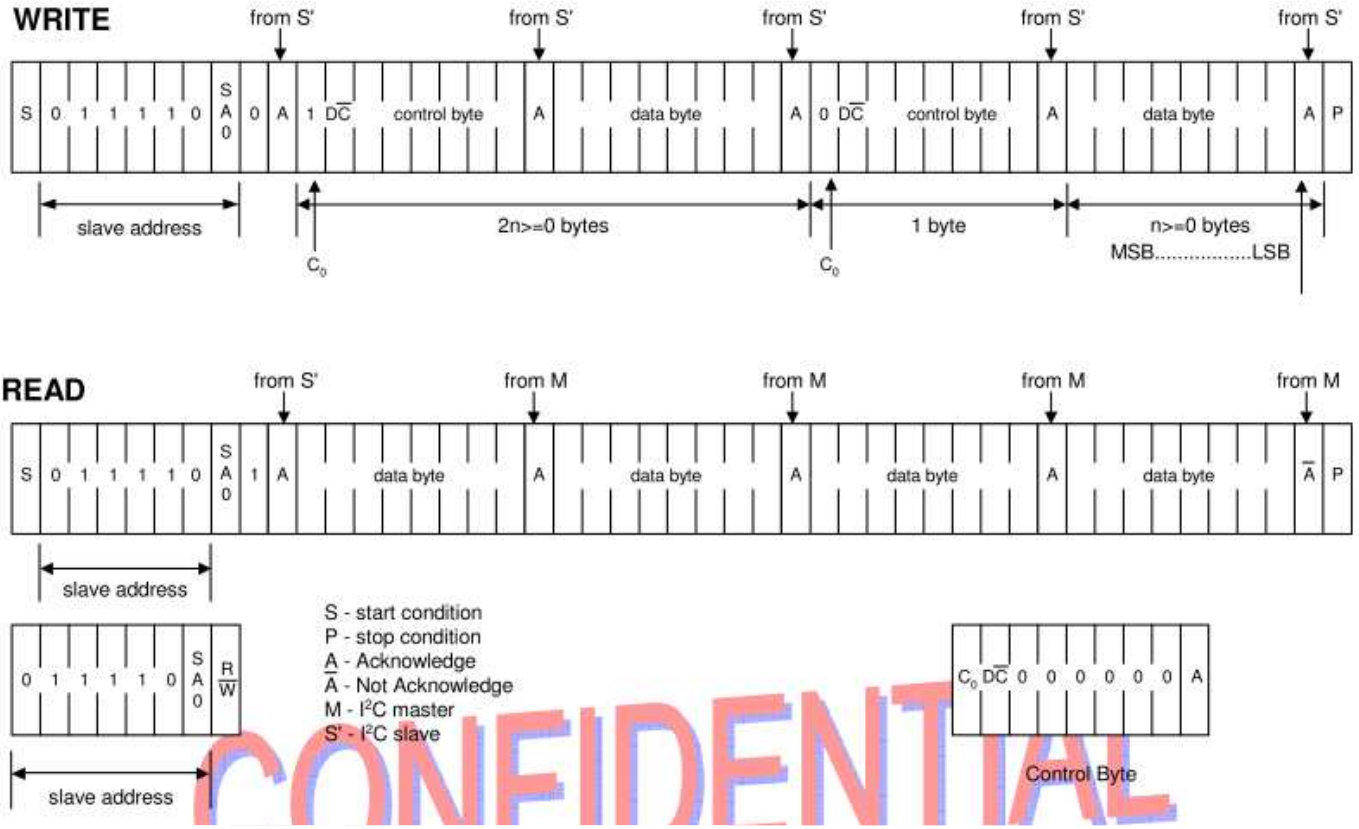


System configuration

1. Transmitter: The device that sends the data to the bus.
2. Receiver: The device that receives the data from the bus.
3. Master: The device that initiates a transfer, generates clock signals and terminates a transfer.
4. Slave: The device addressed by a master.
5. Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
6. Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowedto do so and the message is not corrupted.
7. Synchronization: Procedure to synchronize the clock signals of two or more devices.



Protocol

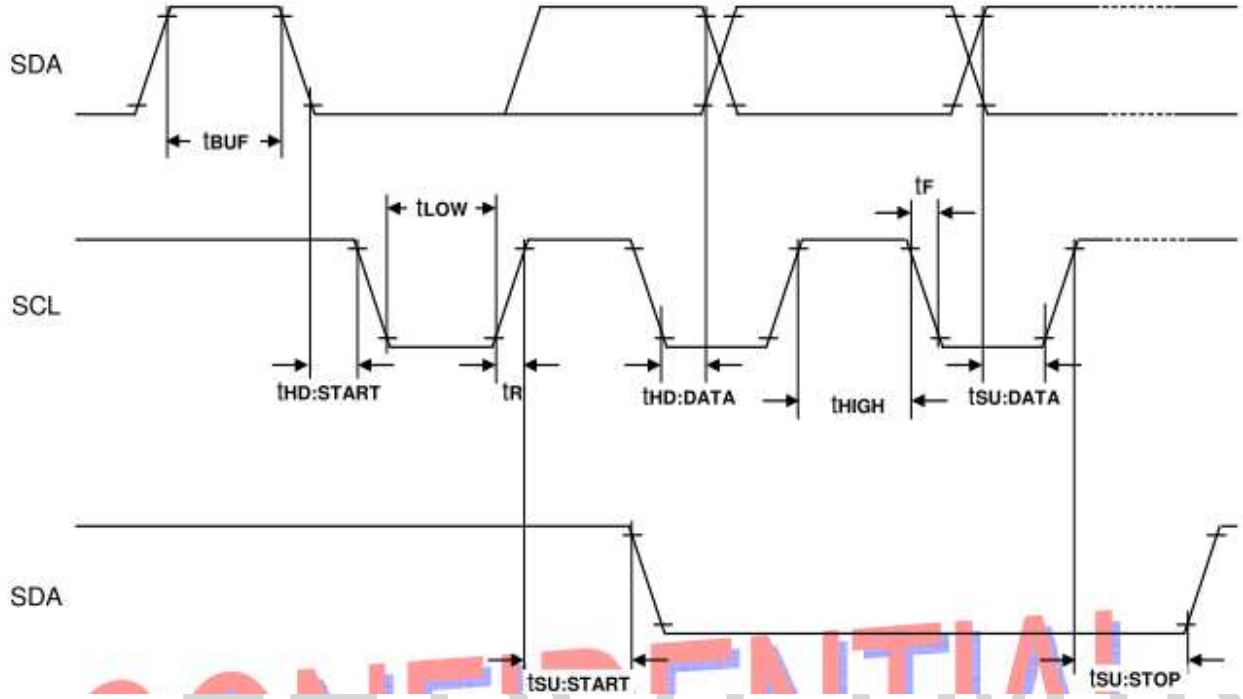


Note1:

1. Co = "0" : The last control byte , only data bytes to follow,
   Co = "1" : Next two bytes are a data byte and another control byte;
2. D/C̄ = "0" : The data byte is for command operation,
   D/C̄ = "1" : The data byte is for RAM operation.

9.2 System buses Read/Write Characteristics

I2C interface characteristics



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fSCL	SCL clock frequency	DC	-	400	kHz	
TLOW	SCL clock Low pulse width	1.3	-	-	uS	
THIGH	SCL clock H pulse width	0.6	-	-	uS	
TSU:DATA	data setup time	100	-	-	nS	
THD:DATA	data hold time	0	-	0.9	uS	
TR	SCL、SDA rise time	20+0.1Cb	-	300	nS	
TF	SCL、SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
TSU:START	Setup timefor re-START	0.6	-	-	uS	
THD:START	START Hold time	0.6	-	-	uS	
TSU:STOP	Setup time for STOP	0.6	-	-	uS	
TBUF	Bus free times between STOP and START condition	1.3	-	-	uS	

9.3 Display Control Instruction

Instruction	Instruction Code										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear entire display area.(POR = 01H)
Return Home	0	0	0	0	0	0	0	0	1	—	Counter with DDRAM address 00H. (POR = 10H)
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.(POR = 08H)
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Shift display or move cursor..
Function Set	0	0	0	0	1	DL	N	F	—	—	Set number of display line (N), and character font (F). (POR = 30H)
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read Busy Flag (BF) and Address Counter (POR = 00H)
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to CG RAM or DD RAM. (POR= 00H)
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from CG RAM or DD RAM. (POR = 00H)

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

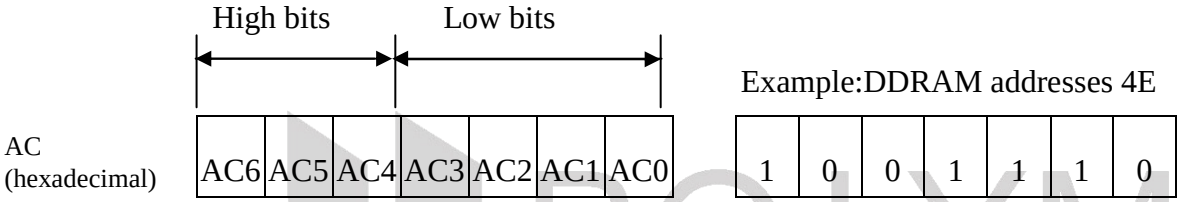
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationship between DDRAM addresses and positions on the liquid crystal display.



DDRAM Address

Display position DDRAM address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	14	16
00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

Example: 1-Line by 16-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

10. Built-in CGROM (Character Generator ROM)

ENGLISH_JAPANESE