Future Technology Devices International Ltd

TN_161 FT4222H Errata Technical Note

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Version 1.1

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The intention of this errata technical note is to give a detailed description of known functional or electrical issues with the FTDI FT4222H series device.
The current revision of the FT4222H series is **Revision B, released Sep 2015.**

Future Technology Devices International Limited (FTDI)
Unit 1, 2 Seaward Place, Glasgow G41 1HH, United Kingdom
Tel.: +44 (0) 141 429 2777 Fax: + 44 (0) 141 429 2758
Web Site: http://ftdichip.com

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1 FT4222H Revision

FT4222H part numbers are listed in **Table 1.** The letter at the end of the date code identifies the device revision.

The current revision of the FT4222H series is **revision B, released Sep 2015.** At the time of releasing this Technical Note there is a known issue with this silicon revision.

Part Number	Package
FT4222HQ	32 pin VQFN

Table 1 FT4222H Part Numbers

This errata technical note covers the revisions of FT4222H listed in Table 2.

Revision	Notes
A	First device revision. Launched Sep 2014
B	Second device revision. Launched Sep 2015

Table 2 FT4222H Series Revisions

2 Errata History Table – Functional Errata

Functional Errata	Short description	Errata occurs in device revision
FT4222H	Android issues	A
FT4222H	CPU usage too high	A
FT4222H	I²C combined message support	A
FT4222H	Default pin status change	A
FT4222H	More suspend setting support	A
FT4222H	Custom PID settings are ignored	B

Table 3 Functional Errata

2.1 Errata History Table – Electrical and Timing Specification Deviations

Deviations	Short description	Errata occurs in device revision
-	No known issues	-

Table 4 Electrical and Timing Errata

3 Functional Errata of FT4222H

3.1 Revision A

3.1.1 Android issues

Introduction:

FT4222H supports Android devices. With J2XX, it is possible to develop an app utilizing the FT4222H.

Issue:

The following issues may happen when the FT4222H connects to an Android device.

1. The FT4222H works as an SPI master, it may reset during transferring data.
2. The FT4222H works as I^2C slave, the last byte may be lost when the receiving buffer is full.

Workaround:

There are no known workarounds available. This issue is corrected at revision B.

Package specific:

The effected packages are listed in Table 5.

Package	Applicable (Yes/No)
FT4222HQ	Yes

Table 5 Effected Packages

3.1.2 CPU usage and latency timer issue

Introduction:

In USB, data is received from the device to the PC by a polling method. The driver will request a certain amount of data from the USB scheduler. The latency timer is provided to allow efficient polling and flushing short data packets.

Issue:

The FT4222H doesn't support the latency timer feature and causes the USB scheduler to be busy and uses too much CPU resource.

Workaround:

There are no known workarounds available. This issue is corrected at revision B.

Package specific:

The effected packages are listed in Table 6.

Package	Applicable (Yes/No)
FT4222HQ	Yes

Table 6 Effected Packages

3.1.3 I²C combined message issue

Introduction:

A master issue at least two reads and/or writes to one or more slaves. In a combined message, each read or write begins with a START and the slave address. After the first START, the subsequent starts are referred to as repeated START bits; repeated START bits are not preceded by STOP bits, which indicate to the slave the next transfer is part of the same message.

Start	7 bit slave address	write	ACK	8 bit data	ACK	**SR**	7 bit slave address	read	ACK	8 bit data	ACK	8 bit data	ACK	STOP

Issue:

Some I²C devices need to communicate with a combined message format. However, the FT4222H doesn't support this feature.

Workaround:

There are no known workarounds available. The feature of I²C combined messages will be supported at revision B.

Package specific:

The effected packages are listed in Table 7.

Package	Applicable (Yes/No)
FT4222HQ	Yes

Table 7 Effected Packages

3.1.4 Default pin status

Introduction:

By default, the FT4222H will be initialized as an SPI master after power on. When the FT4222H is ready, i.e. finishes USB enumeration, the status of the pins of the Rev.A device is as shown below:

pin num	pin name	mode 0	mode 1	mode 2	mode 3
8	SCK	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)
9	MISO	MISO (IN)	MISO (IN)	MISO (IN)	MISO (IN)
10	MOSI	MOSI (OUT, high)	MOSI (OUT, high)	MOSI (OUT, high)	MOSI (OUT, high)
11	IO2	IO2 (IN)	IO2 (IN)	IO2 (IN)	IO2 (IN)
12	IO3	IO3 (IN)	IO3 (IN)	IO3 (IN)	IO3 (IN)
13	GPIO0	GPIO0 (OUT, low)	SS1O (OUT, low)	SS1O (OUT, low)	GPIO0 (OUT, low)
14	GPIO1	GPIO1 (OUT, low)	SS2O (OUT, low)	SS2O (OUT, low)	GPIO1 (OUT, low)
15	GPIO2	suspend out (OUT, low)	suspend out (OUT, low)	SS3O (OUT, low)	suspend out (OUT, low)
16	GPIO3	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)
17	SS0O	SS0O (OUT, low)	SS0O (OUT, low)	SS0O (OUT, low)	SS0O (OUT, low)
32	SS	SS (IN)	SS (IN)	SS (IN)	SS (IN)

Table 8 Rev.A FT4222H ready

In the Rev.B, the pin status will be changed as per the table below:

pin num	pin name	mode 0	mode 1	mode 2	mode 3
8	SCK	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)
9	MISO	MISO (IN)	MISO (IN)	MISO (IN)	MISO (IN)
10	MOSI	MOSI (OUT, high)	MOSI (OUT, high)	MOSI (OUT, high)	MOSI (OUT, high)
11	IO2	IO2 (IN)	IO2 (IN)	IO2 (IN)	IO2 (IN)
12	IO3	IO3 (IN)	IO3 (IN)	IO3 (IN)	IO3 (IN)
13	GPIO0	GPIO0 (IN)	SS1O (OUT, high)	SS1O (OUT, high)	GPIO0 (IN)
14	GPIO1	GPIO1 (IN)	SS2O (OUT, high)	SS2O (OUT, high)	GPIO1 (IN)
15	GPIO2	suspend out (OUT, low)	suspend out (OUT, low)	SS3O (OUT, high)	suspend out (OUT, low)
16	GPIO3	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)
17	SS0O	SS0O (OUT, high)	SS0O (OUT, high)	SS0O (OUT, high)	SS0O (OUT, high)
32	SS	SS (IN)	SS (IN)	SS (IN)	SS (IN)

Table 9 Rev.B FT4222H ready

Package specific:

The effected packages are listed in Table 10.

Package	Applicable (Yes/No)
FT4222HQ	Yes

Table 10 Effected Packages

3.1.5 More suspend setting support

Introduction:

The FT4222H provides flexible settings for suspend behavior via FT_Prog. The rev.B of the FT4222H device provides more options for customers to configure the pin status during suspend.

- SUSPEND_OUT_POL
  - **Suspend output is High active. (default)**
  - Suspend output is Low active.
- SPI_SUSPEND_MODE
  - **Disable SPI IP and make SPI pins input (tri-state). (default)**
  - Keep SPI pin status when the FT4222H suspends.
  - Enable SPI pin control. Refer to SPI_SUSPEND for detail settings.
- SPI_SUSPEND (enable by SPI_SUSPEND_MODE)
  - miso_suspend
    - push low when suspend
    - push high when suspend
  - mosi_suspend
    - push low when suspend
    - push high when suspend
  - io2_io3_suspend
    - push low when suspend
    - push high when suspend
  - ss0O_suspend
    - No change (default)
    - push low when suspend
    - push high when suspend
- GPIO_SUSPEND
  - gpio0_suspend
    - No change (default)
    - input (tri-state)
    - push low when suspend
    - push high when suspend
  - gpio1_suspend
    - No change (default)
    - input (tri-state)
    - push low when suspend
    - push high when suspend
  - gpio2_suspend
    - No change (default)
    - input (tri-state)
    - push low when suspend
    - push high when suspend
  - gpio3_suspend
    - No change (default)
    - input (tri-state)
    - push low when suspend
    - push high when suspend

The default pin status of the Rev.A device during suspend is shown below:

pin num	pin name	mode 0	mode 1	mode 2	mode 3
8	SCK	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)
9	MISO	MISO (OUT, low)	MISO (OUT, low)	MISO (OUT, low)	MISO (OUT, low)
10	MOSI	MOSI (OUT, low)	MOSI (OUT, low)	MOSI (OUT, low)	MOSI (OUT, low)
11	IO2	IO2 (OUT, low)	IO2 (OUT, low)	IO2 (OUT, low)	IO2 (OUT, low)
12	IO3	IO3 (OUT, low)	IO3 (OUT, low)	IO3 (OUT, low)	IO3 (OUT, low)
13	GPIO0	GPIO0 (OUT, low)	SS1O (OUT, no change)	SS1O (OUT, no change)	GPIO0 (OUT, low)
14	GPIO1	GPIO1 (OUT, low)	SS2O (OUT, no change)	SS2O (OUT, no change)	GPIO1 (OUT, low)
15	GPIO2	suspend out (OUT, high)	suspend out (OUT, high)	SS3O (OUT, no change)	suspend out (OUT, high)
16	GPIO3	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)
17	SS0O	SS0O (OUT, no change)	SS0O (OUT, no change)	SS0O (OUT, no change)	SS0O (OUT, no change)
32	SS	SS (IN)	SS (IN)	SS (IN)	SS (IN)

Table 11 Rev.A FT4222H suspend

In the Rev.B device, the default suspend setting is changed as per the table below:

pin num	pin name	mode 0	mode 1	mode 2	mode 3
8	SCK	SCK (tri-state)	SCK (tri-state)	SCK (tri-state)	SCK (tri-state)
9	MISO	MISO (IN)	MISO (IN)	MISO (IN)	MISO (IN)
10	MOSI	MOSI (IN)	MOSI (IN)	MOSI (IN)	MOSI (IN)
11	IO2	IO2 (IN)	IO2 (IN)	IO2 (IN)	IO2 (IN)
12	IO3	IO3 (IN)	IO3 (IN)	IO3 (IN)	IO3 (IN)
13	GPIO0	GPIO0 (no change)	SS1O (OUT, no change)	SS1O (OUT, no change)	GPIO0 (no change)
14	GPIO1	GPIO1 (no change)	SS2O (OUT, no change)	SS2O (OUT, no change)	GPIO1 (no change)
15	GPIO2	suspend out (OUT, high)	suspend out (OUT, high)	SS3O (OUT, no change)	suspend out (OUT, high)
16	GPIO3	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)
17	SS0O	SS0O (OUT, no change)	SS0O (OUT, no change)	SS0O (OUT, no change)	SS0O (OUT, no change)
32	SS	SS (IN)	SS (IN)	SS (IN)	SS (IN)

Table 12 Rev.B FT4222H suspend

Package specific:

The effected packages are listed in Table 13.

Package	Applicable (Yes/No)
FT4222HQ	Yes

Table 13 Effected Packages

3.2 Revision B

3.2.1 Custom PID settings are ignored

Introduction

It is not possible to change the PID on the FT4222H from our default value of 601C to a custom value. Note, there are no problems changing the VID.

Issue

Any changes made to the PID using the OTP are ignored and the value returns to its default state.

Workaround

There are no workarounds available.

4 FT4222H Series Package Markings

The FT4222H is supplied in a RoHS compliant leadless VQFN-32 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC. An example of the markings on the package is shown in the figures below.

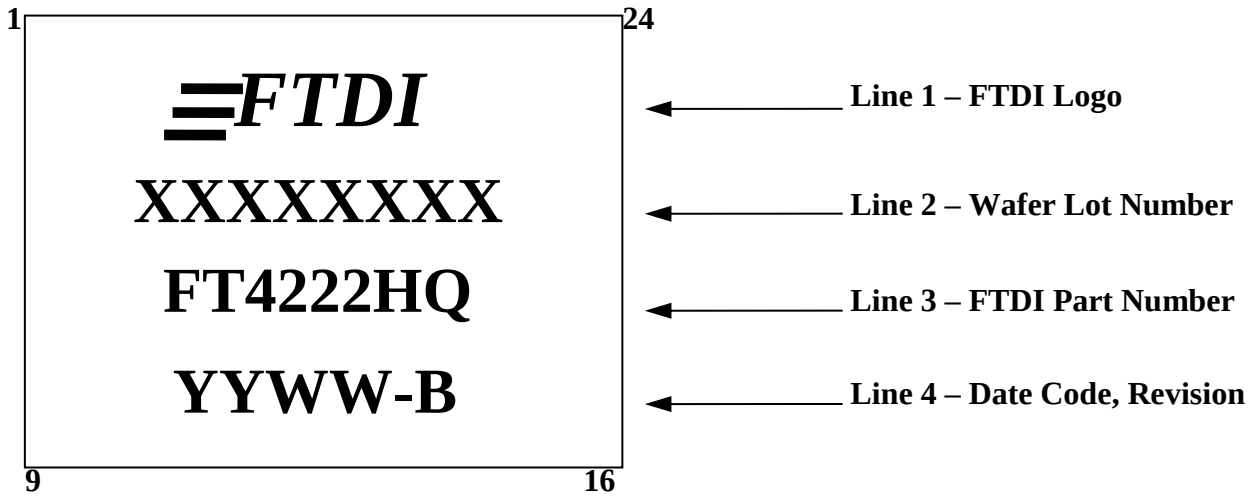

Figure 4.1 VQFN-32 Package Markings

The date code format is **YYWW** where WW = 2 digit week number, YY = 2 digit year number. This is followed by the revision number.
The code **XXXXXXXX** is the manufacturing LOT code

5 Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Tigard, Oregon, USA

Future Technology Devices International Limited
(USA)
7130 SW Fir Loop
Tigard, OR 97223
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited
(Taiwan)
2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan , R.O.C.
Tel: +886-2-8797 1330
Fax: +886-2-8751-9737

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Shanghai, China

Future Technology Devices International Limited
(China)
Room 1103, No.666 West Huaihai Road,
Shanghai, 200052
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

http://ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Acronyms and Abbreviations

Terms	Description
CPU	Central Processing Unit
GPIO	General Purpose Input/output
I2C	Inter-Integrated Circuit
MISO	Master In Slave Out
MOSI	Master Out Slave In
PC	Personal Computer
SS	Slave Select
SCK	Serial Clock
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
VQFN	Very Thin Quad Flat Non-Leaded Package

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Appendix C – Revision History

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Revision	Changes	Date
1.0	Initial Release	2015-08-31
1.1	Updated with custom PID issue.	2016-05-17