# PIC18(L)F1XK50
# Silicon Errata and Data Sheet Clarification

The PIC18(L)F1XK50 family devices that you have received conform functionally to the current Device Data Sheet (DS41350**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F1XK50 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B0**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F1XK50 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) | Silicon Revision ID(2) | | | |
|---|---|---|---|---|---|
| | | A6 | A7 | A8 | B0 |
| PIC18LF13K50 | 4700h | 06h | 07h | 08h | 00h |
| PIC18LF14K50 | 4720h | 06h | 07h | 08h | 00h |
| PIC18F13K50 | 4740h | 06h | 07h | 08h | 00h |
| PIC18F14K50 | 4760h | 06h | 07h | 08h | 00h |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

**2:** Refer to the *"PIC18(L)F1XK50 Flash Memory Programming Specification"* (DS41342) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions(1) | | | |
|---|---|---|---|---|---|---|---|
| | | | | A6 | A7 | A8 | B0 |
| ADC (Analog-to-Digital Converter) | Conversions | 1.1 | INL error and acquisition time. | X | X | | |
| ADC (Analog-to-Digital Converter) | Conversions | 1.2 | May fail in RUN mode. | X | | | |
| ADC (Analog-to-Digital Converter) | Conversions | 1.3 | High pin leakage. | X | X | X | |
| ADC (Analog-to-Digital Converter) | Conversions | 1.4 | Offset error. | X | X | | |
| ADC (Analog-to-Digital Converter) | Conversions | 1.5 | ADC conversion does not complete. | X | X | | |
| MSSP (Master Synchronous Serial Port) | Transmit Setup | 2.1 | SPI and $I^2C$™ clock and bit issues. | X | X | X | X |
| MSSP (Master Synchronous Serial Port) | Receive mode | 2.2 | SSPIF flag set early. | X | X | X | X |
| System Clocks | HFINTOSC | 3.1 | Frequency instability. | X | X | | |
| System Clocks | HFINTOSC | 3.2 | Frequency shift on Reset. | X | | | |
| EUSART | Receive mode | 4.1 | RCIDL bit issue. | X | | | |
| EUSART | OERR flag | 4.2 | Cannot clear the OERR flag. | X | X | | |
| EUSART | Asynchronous mode | 4.3 | TX/CK improperly driven. | X | X | X | X |
| CPU | Sleep | 5.1 | Reset on Wake-up. | X | X | | |
| Timer1 Oscillator | Operations | 6.1 | Fails to operate above 90°C. | X | X | X | |
| IOC (Interrupt-on-Change) | Multiple Sources | 7.1 | Invalid interrupts. | X | X | X | X |
| Boot Block Memory | Code Protection | 8.1 | BBSIZ selection is invalid for code-protect. | X | X | X | X |
| Enhanced/Capture/ Compare PWM (ECCP) | Special Event Trigger | 9.1 | Will not start A/D conversion. | X | X | | |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B0**).

### 1. Module: ADC (Analog-to-Digital Converter)

**1.1** Offset error is 3 LSb typical, 7 LSb maximum, including an acquisition time dependent component (~2 LSb).

**Work around**

The time dependent error is insignificant when the time between conversions is less than 100 ms. When the time since the previous conversion is greater than 100 ms, take two ADC conversions and discard the first.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

**1.2** When the ADC is configured to operate with the internal FRC oscillator (ADCON2<2:0> = X11) and the device is not in Sleep, then the ADC may fail to complete the conversion which is indicated by the GO/DONE bit of the ADCON0 register remaining in the GO state indefinitely. This condition can be cleared by a device Reset or by clearing the ADON bit of the ADCON0 register.

**Work around**

1. Select a clock source that is not FRC.
2. Set the ADIE bit of the PIE1 register and clear the ADIF bit of the PIR1 register, then put the part to Sleep immediately after setting the GO/DONE bit of the ADCON0 register. The device will perform the conversion during Sleep and Wake at the completion.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

**1.3** ADC conversion on AN3/OSC2 will have large INL error up to approximately 8 LSb.

**Work around**

None for the AN3 pin. For better accuracy, use another analog pin.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

**1.4** The offset error incorrectly exceeds the data sheet specifications if time between conversions is longer than 10 ms. If the time between conversions is greater than 10 ms, the offset error is 1 LSB typical and 3.3 LSB maximum.

**Work around**

The time dependent error is insignificant when the time between conversions is less than 10 ms. When the time between conversions is greater than 10 ms, take two back-to-back ADC conversions and discard the results of the first conversion.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

**1.5** Under certain device operating conditions, the ADC conversion may not complete properly. When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the ADGO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

**Work around**

Select the dedicated RC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 2. Module: MSSP (Master Synchronous Serial Port)

### 2.1 Short First Clock Pulse During SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011), the first SPI high time may be short.

**Work around**

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 2.2 SSPIF is Set Prematurely During SPI

The MSSP interrupt flag bit is set at one-half clock cycle before it should be, if modes 1 or 3 are used. This affect can be seen in the following situations:

1. Mode 1: CKP = 0, CKE = 0
2. Mode 3: CKP = 1, CKE = 0

It is most notable if the SPI clock is used at low-clock speeds. If the user responds to the interrupt and writes to SSPBUF before the intended interrupt time, then the WCOL (Write Collision) bit will be set and the transmission will not occur. Future transmissions will not occur until the WCOL bit is cleared.

**Work around**

Delay at least one-half period length of time before writing to SSPBUF after the SSPIF is set, if using modes 1 or 3.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## 3. Module: System Clocks

### 3.1 Frequency Instability

HFINTOSC output frequency may have up to 1% short term frequency instability.

**Work around**

Use the HS, XT or EC clock modes.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 3.2 Frequency Shift on Reset

The internal oscillator module may experience a ±1% frequency shift after a Reset. The frequency shift is not consistent and could cause the oscillator to operate outside of the 2% specification.

**Work around**

To minimize the chances of experiencing the frequency shift, the following steps should be taken:

1. Operate the internal oscillator at 8 MHz or 2 MHz.
2. Use an external pull-up on $\overline{\text{MCLR}}$ or use internal $\overline{\text{MCLR}}$ mode.
3. Disable the Power Reset Timer (PWRT).
4. The bypass capacitor and Voltage Regulator Capacitor ($V_{CAP}$) should be used appropriately to minimize noise in the device.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 4. Module: EUSART

### 4.1 RCIDL Bit

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when the RX input goes low at the leading edge of a Start bit. If the RX input stays low for less than 1/8$^{th}$ of a bit time, then the Start bit is invalid and the RCIDL should go high. However, the RCIDL bit will stay low improperly until a valid Start bit is received.

**Work around**

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 4.2 OERR Bit

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

**Work around**

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 4.3 Asynchronous Mode

In Asynchronous mode when TXEN = 0, the TX/CK output is improperly driven. All mid-range parts tri-state the TX/CK pin when TXEN = 0 in Asynchronous mode.

**Work around**

None.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## 5. Module: CPU

### 5.1 Reset on Wake-up

If a wake from Sleep event occurs during the execution of a Sleep command, the device may reset. This Reset will be seen as a Power-on Reset to the device.

**Work around**

1. Disable all asynchronous interrupt before going to Sleep.
2. Make sure the timing of an asynchronous interrupt will not happen during the execution of the SLEEP instruction.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 6. Module: Timer1 Oscillator

### 6.1 Operation above 90°C

The Timer1 oscillator does not operate above 90°C.

**Work around**

None.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 7. Module: IOC (Interrupt-on-Change)

### 7.1 IOC (Interrupt-on-Change) False Wake-up

When IOC is enabled for multiple pins to wake-up the processor from Sleep, invalid interrupts or wake-ups may occur.

**Work around**

Use only one pin as IOC with Sleep.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## 8. Module: Boot Block Memory

### 8.1 BBSIZ Selection is Invalid for Code-Protect

When code-protecting the Boot Block with the CPB bit in CONFIG5H, the smaller Boot Block size is used, regardless of the BBSIZ bit selection in CONFIG4L. If Block 0 is also code-protected, the full range of memory from the Boot Block through Block 0 is protected; no intermediate program memory is left unprotected.

**Work around**

None.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## 9. Module: Enhanced/Capture/Compare PWM (ECCP)

### 9.1 Will not Start A/D Conversion

When the ECCP is configured to work in Compare mode as a Special Event Trigger (CCP1M<3:0> = 1011), the special event trigger will not set the GO/DONE bit of the ADCON0 register and A/D conversion will not take place.

**Work around**

In the interrupt set ADCON0bits.GO = 1 with software after the CCPIF is set.

**Affected Silicon Revisions**

| A6 | A7 | A8 | B0 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41350**E**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

None.

## APPENDIX A: DOCUMENT REVISION HISTORY

### Rev A Document (10/2008)

Initial release of this document

### Rev B Document (8/2009)

Updated Errata to new format; minor edits.

Data Sheet Clarifications:

Added Modules 1-8 to add QFN package information to data sheet.

### Rev C Document (05/2010)

Removed ‘Rev. A6’ from the title; Added A7 and A8 silicon revisions to Table 1 and Table 2; Removed Note 2 from Table 1; Updated Module 1.4; Added Module 1.5; Removed Table 3; Removed Modules 2.2, 2.3, 2.4, 2.5, 2.6; Added Modules 3.1 and 3.2; Updated Module 4; Added Modules 5.1, 5.2, 5.3, 6 and 7; Updated the Affected Silicon Revision section adding A7 and A8.

Data Sheet Clarifications:

Removed Modules 1 to 8. Data Sheet updated.

### Rev D Document (07/2011)

Added Silicon revision B0; Deleted Module 4, Timer1 and renumbered Modules.

### Rev E Document (11/2011)

Updated Errata to new format; Added Module 2.2.

### Rev F Document (02/2012)

Added Module 7, Interrupt-on-Change.

### Rev G Document (07/2012)

Added MPLAB X IDE; Added Module 8, Boot Block Memory.

### Rev H Document (11/2012)

Added Module 9, Enhanced Capture/Compare/PWM (ECCP).

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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