TFT Module Specification

MODEL: 13-080ZIMA0GA0-S

< ◇ > PRELIMINARY SPECIFICATION

< ◆ > APPROVAL SPECIFICATION

CUSTOMER
APPROVED BY
DATE:

DESIGNED	CHECKED	APPROVED
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RECORD OF REVISION

Version	Revised Date	Page	Content
V1.0	2020/12/23	--	PRELIMINARY SPECIFICATION

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

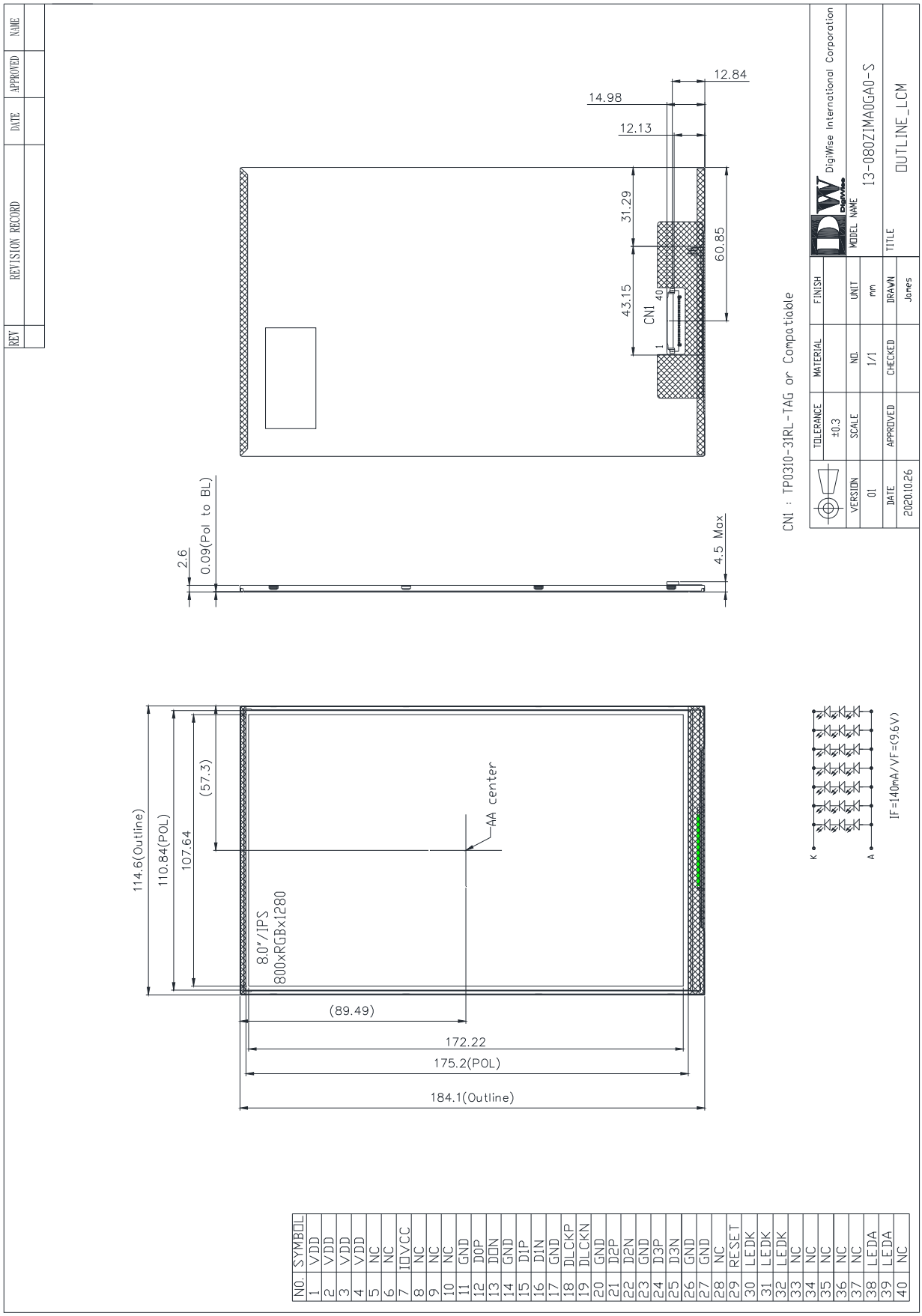
1.1 Description

The specification is model 13-080ZIMA0GA0-S is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit, a backlight system. This TFT LCD has a 8 inch diagonally measured active display area with HD (800 horizontal by 1280 vertical pixels) resolution.

1.2 Features:

No.	Item	Specification	Unit
1	Panel Size	8”	Inch
2	Number of Pixels	800 (W) x RGB x 1280 (H)	Pixels
3	Active Area	107.64 (W) × 172.22 (H)	mm
4	Pixel Pitch	0.13455 (W) x 0.13455 (H)	mm
5	Outline Dimension	114.6 (W) × 184.1 (H) × 2.6 (T)	mm
6	Number of Colors	16.7M	- -
7	Display Mode	IPS / Normally Black / Transmissive	- -
8	View Direction	Free direction	
9	Display Format	RGB vertical stripe	- -
10	Surface Treatment	Anti-Glare	- -
11	Contrast Ratio	800 (Typ.)	- -
12	Luminance (cd/m^2)	450 (Typ.)	cd/m2
13	Interface	MIPI DSI 4 lane	- -
14	Backlight	White LED	- -
15	Driver IC	ILI9881C	- -
16	Operation Temperature	-10 ~ 60	°C
17	Storage Temperature	-20 ~ 70	°C
18	Weight	(110)	g

2. MECHANICAL SPECIFICATION



NO.	SYMBOL
1	VDD
2	VDD
3	VDD
4	VDD
5	NC
6	NC
7	IOVCC
8	NC
9	NC
10	NC
11	GND
12	D0P
13	D0N
14	GND
15	D1P
16	D1N
17	GND
18	DLCKP
19	DLCKN
20	GND
21	D2P
22	D2N
23	GND
24	D3P
25	D3N
26	GND
27	GND
28	NC
29	RESET
30	LEDK
31	LEDK
32	LEDK
33	NC
34	NC
35	NC
36	NC
37	NC
38	LEDA
39	LEDA
40	NC

3. PIN DESCRIPTION

Pin No.	Symbol	I/O	Function	Note
1	VDD	P	Power Supply voltage +3.3V	(1)
2	VDD	P	Power Supply voltage +3.3V	
3	VDD	P	Power Supply voltage +3.3V	
4	VDD	P	Power Supply voltage +3.3V	
5	NC	-	No connection	
6	NC	-	No connection	
7	IOVCC	P	Power Supply Logic voltage +1.8V	
8	NC	-	No connection	
9	NC	-	No connection	
10	NC	-	No connection	
11	GND	P	Ground	
12	D0P	I	Positive MIPI differential data input	
13	D0N	I	Negative MIPI differential data input	
14	GND	P	Ground	
15	D1P	I	Positive MIPI differential data input	
16	D1N	I	Negative MIPI differential data input	
17	GND	P	Ground	
18	DCLKP	I	Positive MIPI differential clock input	
19	DCLKN	I	Negative MIPI differential clock input	
20	GND	P	Ground	
21	D2P	I	Positive MIPI differential data input	
22	D2N	I	Negative MIPI differential data input	
23	GND	P	Ground	
24	D3P	I	Positive MIPI differential data input	
25	D3N	I	Negative MIPI differential data input	
26	GND	P	Ground	
27	GND	P	Ground	
28	NC	-	No connection	
29	RST	I	Global reset pin	
30	LEDK	P	LED Cathode	
31	LEDK	P	LED Cathode	
32	LEDK	P	LED Cathode	
33	NC	-	No connection	
34	NC	-	No connection	
35	NC	-	No connection	
36	NC	-	No connection	
37	NC	-	No connection	
38	LEDA	P	LED Anode	
39	LEDA	P	LED Anode	

40	NC	-	No connection	

4. ABSOLUTE MAXIMUM RATINGS

4.1 Electrical Absolute Rating

4.1.1 TFT LCD Module

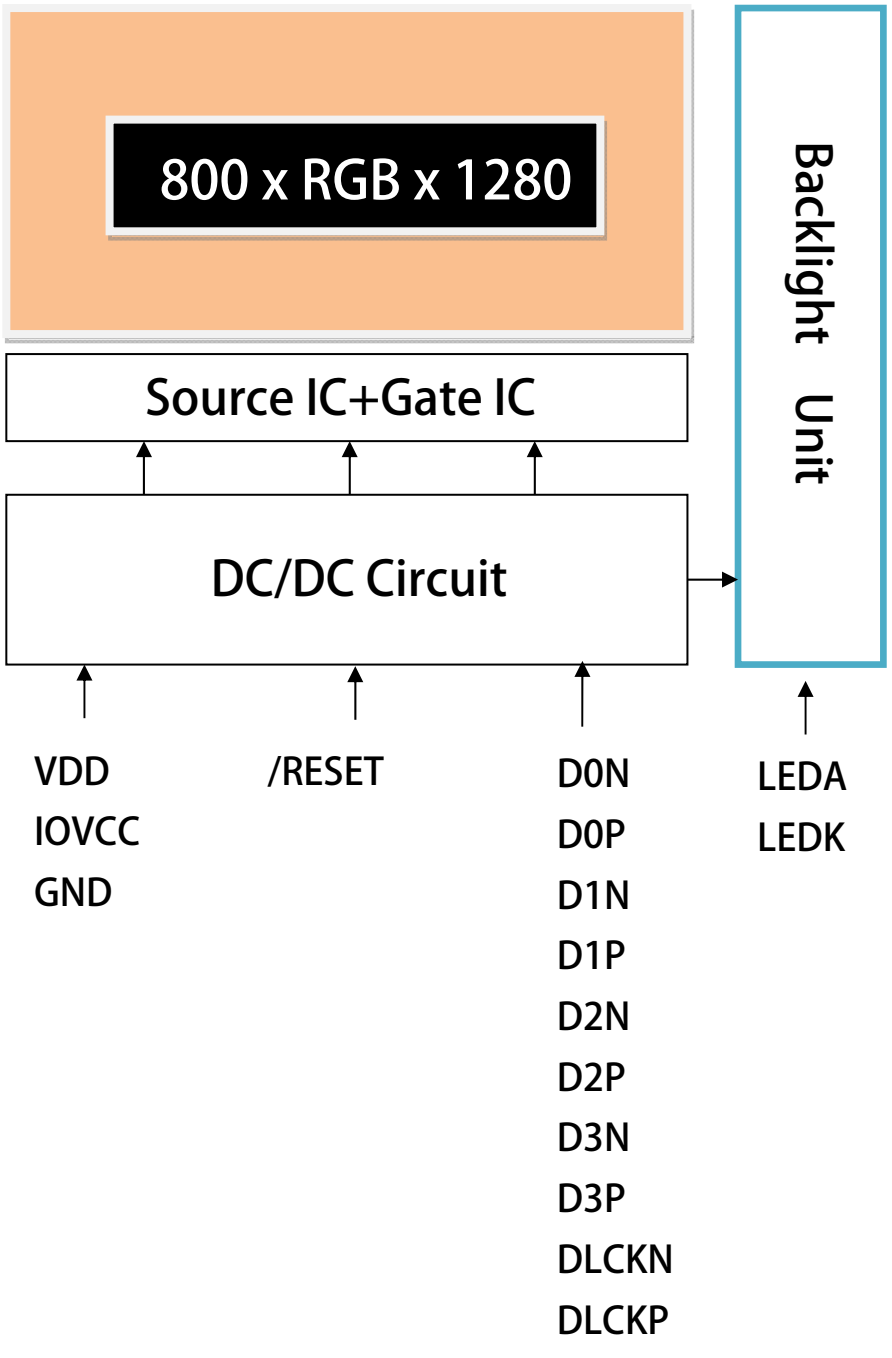
Item	Symbol	Values		Unit	Note
		Min.	Max.		
Power supply voltage	VDD	-0.3	+3.8	V	
	IOVCC	-0.3	+3.8	V	

4.1.2 Environment Absolute Rating

Item	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Operating Temperature	Topa	-10		60	°C	Ambient temperature
Storage Temperature	Tstg	-20		70	°C	

5. BLOCK DIAGRAM

5.1 TFT LCD Module



6. ELECTRICAL CHARACTERISTICS

6.1 DC Characteristics for Panel Driving

Item		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power supply voltage		VDD	2.6	3.3	3.6	V	
		IOVCC	1.65	1.8	3.6	V	
Input Voltage for logic	H Level	VIH	0.7xIOVCC	-	IOVCC	V	
	L Level	VIL	-0.3	-	0.3xIOVCC	V	
Digital Current		IDD	-	TBD	-	mA	

6.2 DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table

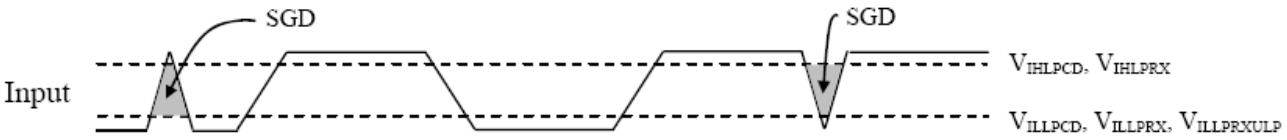
State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

6.2.1 DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

6.2.2 Spike/Glitch Rejection



Notes:

1. A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and Interference Frequency is 450MHz (at the very least).
2. n = 0 and 1.

Spike/Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N, DnP/N	SGD	Input pulse rejection for DSI	-	300	Vps

6.2.3 DC Characteristics for DSI HS mode

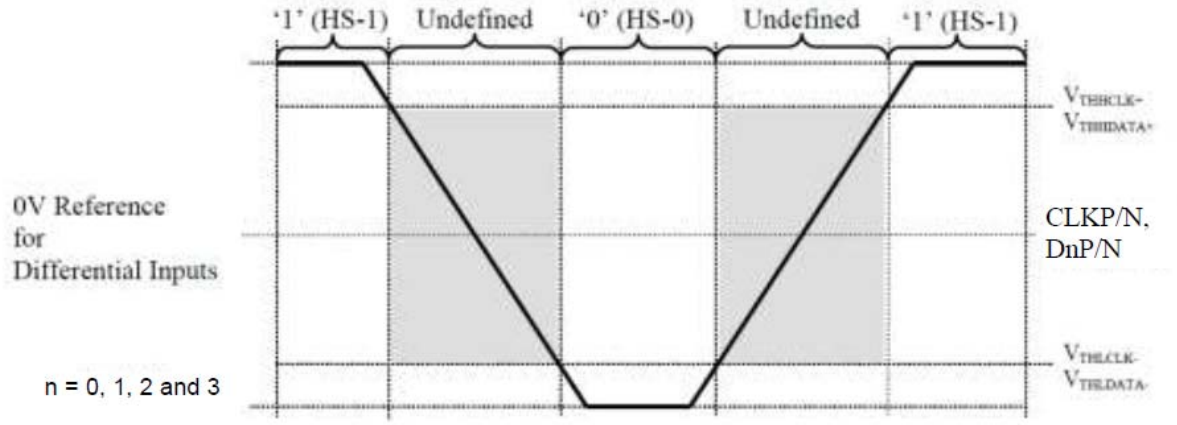
Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF

Notes:

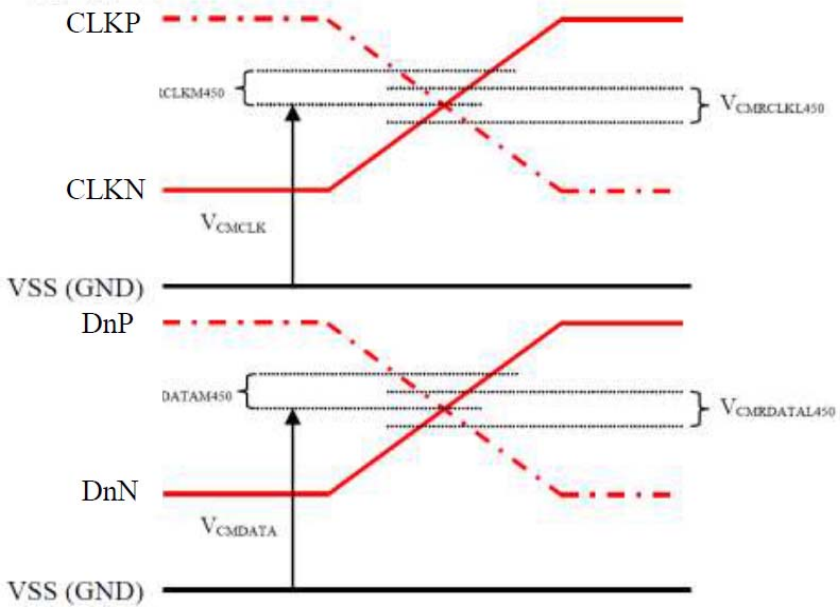
1. Ta = -30℃ to 70℃ (to +85℃ no damage) , VDD = 2.5V to 6.6V, IOVCC = 1.65V to 3.6V

2. Includes 50mV (-50mV to 50mV) ground difference
3. Without VCMRCLKM450/VCMRDATAM450
4. Without 50mV (-50mV to 50mV) ground difference
5. n = 0 and 1
6. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) understands that there is logical 1 (= HS-1) when a differential voltage is more than VTHH (CLKP/DnP). The DSI receiver (HS mode) understands that there is logical 0 (= HS-0) when a differential voltage is more than VTHL (CLKN/DnN). There is undefined state if the differential voltage is less than VTHH (CLKP/DnP) and less than VTHL (CLKN/DnN). A reference figure is below.



Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range



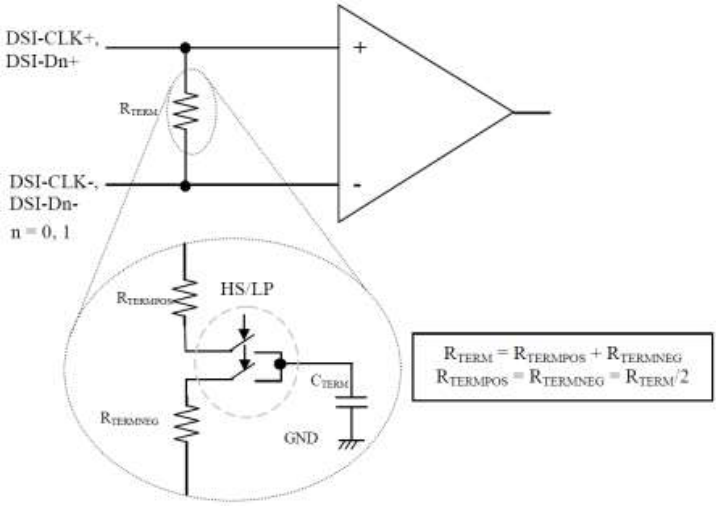
Common Mode Voltage on Clock and Data Channels

The termination resistor (RTERM) of the differential DSI receiver can be driven to two different states by the receiver:

※Low Power (LP) mode when the termination resistor is not connected between differential inputs (CLKP<=> CLKN or D0P <=> D0N or D1P <=> D2N or D2P <=> D3N or D1P <=> D3N)

※High Speed (HS) mode when the termination resistor is connected between differential inputs (CLKP<=> CLKN or D0P <=> D0N or D1P <=> D2N or D2P <=> D3N or D1P <=> D3N)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

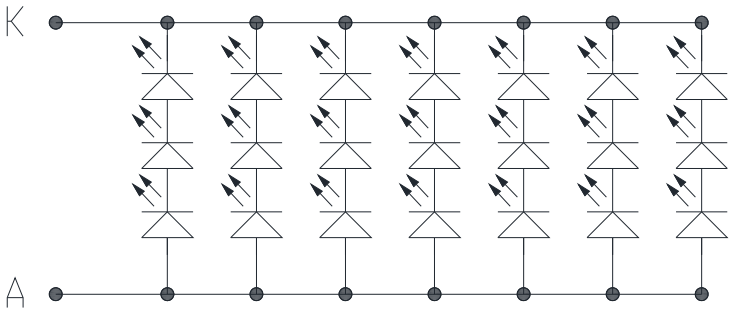


Differential Pair Termination Resistor on the Receiver Side

6.3 Backlight Unit

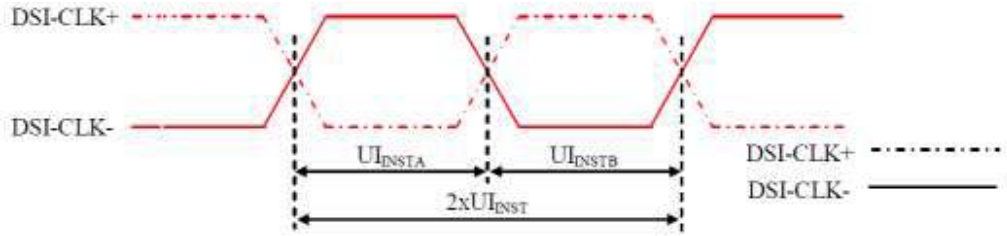
Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
LED Voltage	VL	-	(9.6)	-	V	
LED Current	IL	-	140	-	mA	3S7P
Power Consumption	PBL	-	1.344	-	W	
LED Life Time (25℃)	-	50000	-	-	hr	(1)

Note (1): The “LED life time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ 60% RH.



7. AC CHARACTERISTICS

7.1 High Speed Mode – Clock Channel Timing



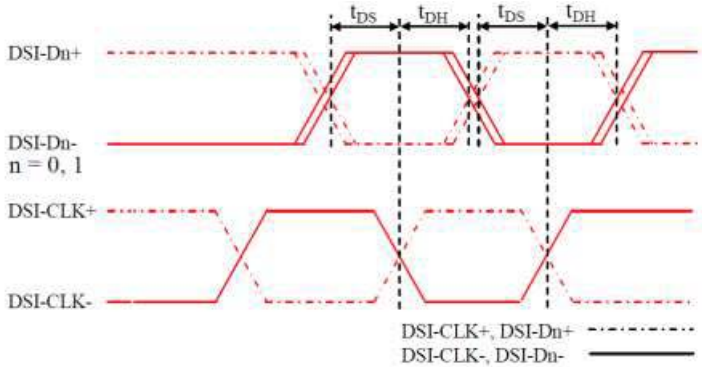
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB
2. Define the minimum value, see below.

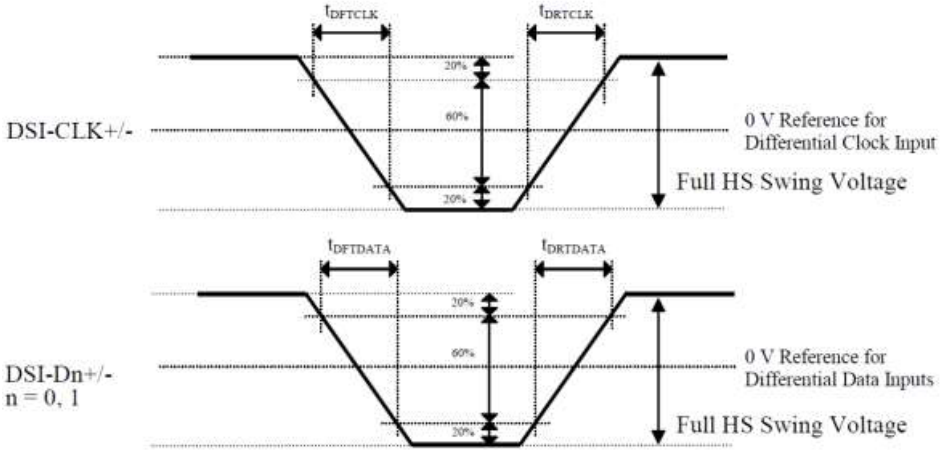
Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

7.2 High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

7.3 High Speed Mode – Rising and Falling Timings

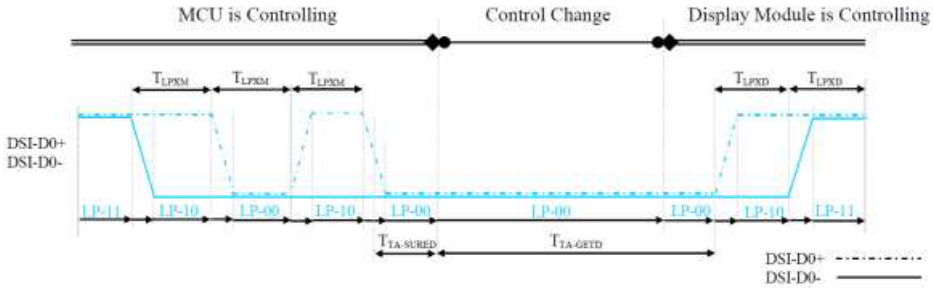


Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

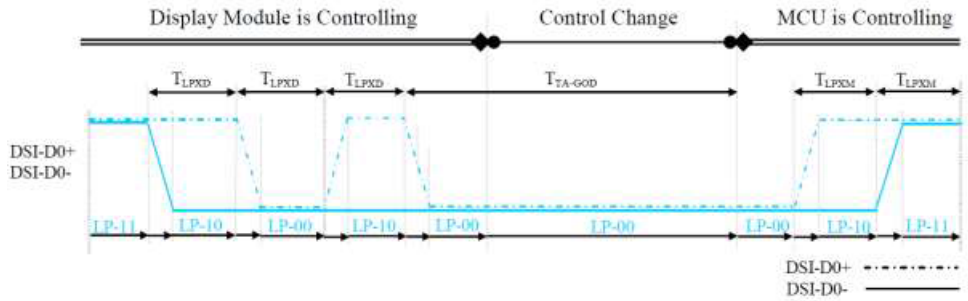
7.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.



BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.



BTA from the Display Module to the MCU

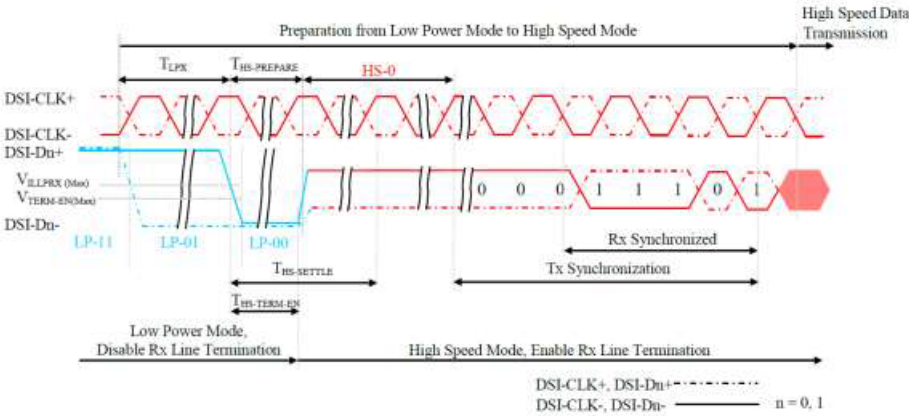
Low Power State Period Timings-A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Low Power State Period Timings-B

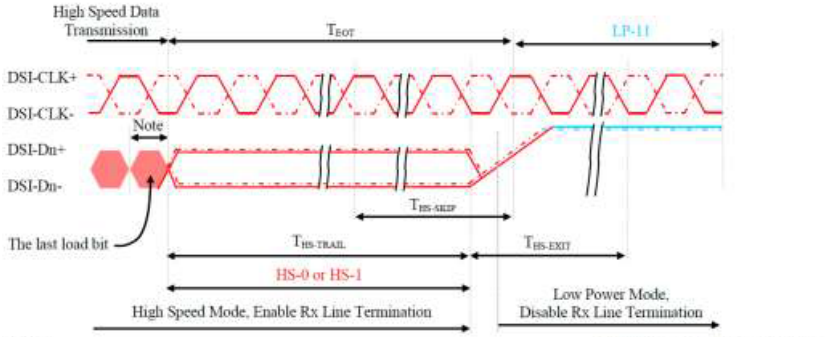
Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

7.5 Data Lanes from Low Power Mode to High Speed Mode



Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

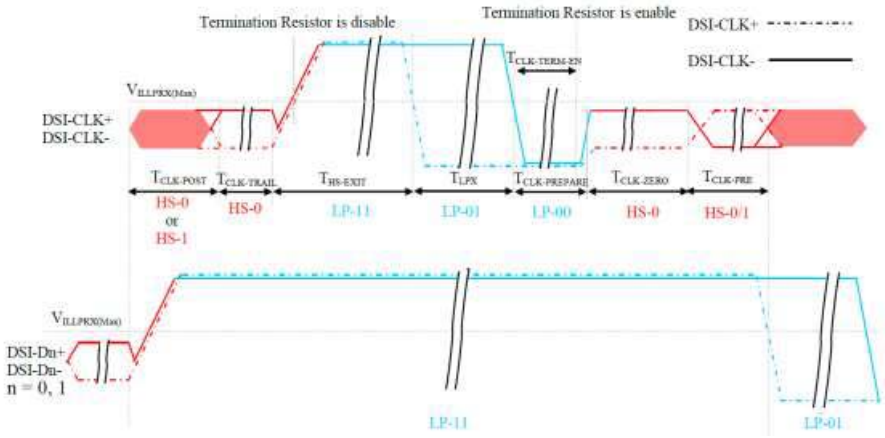
7.6 Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

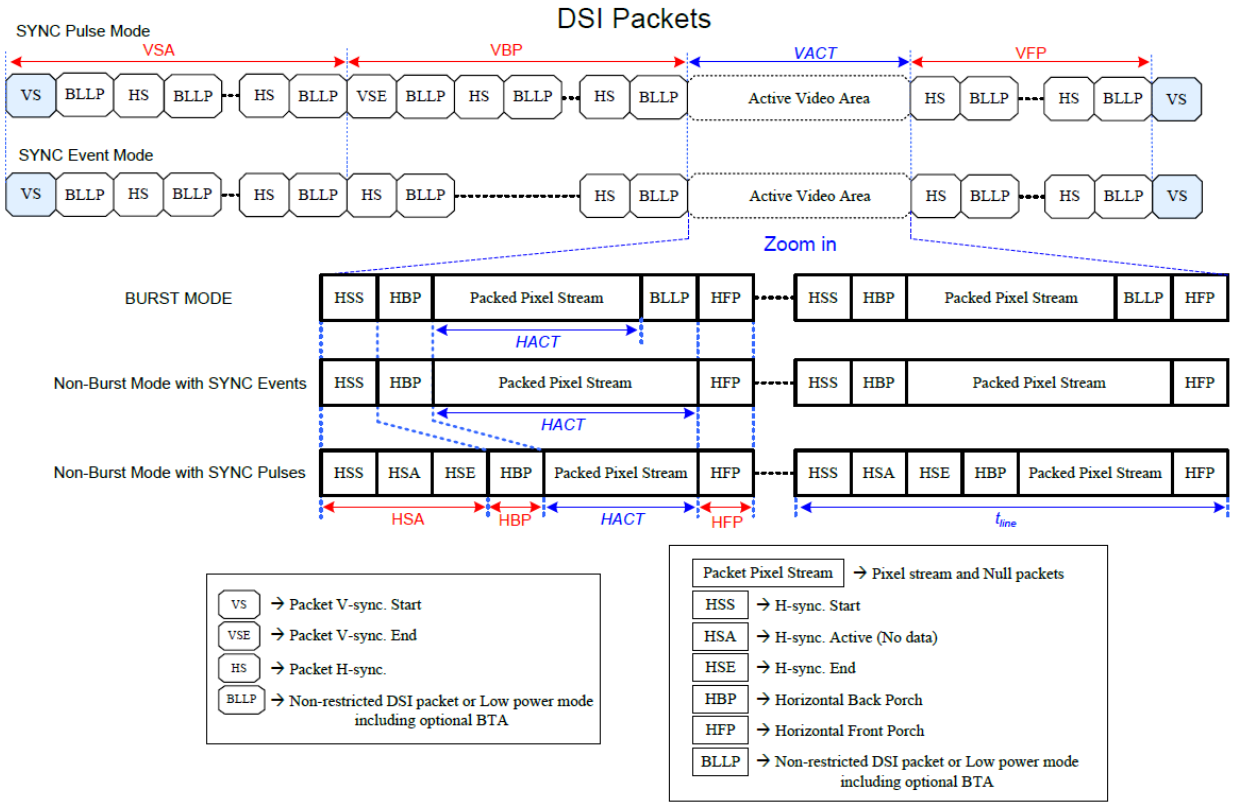
Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

7.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode



Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

7.8 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

7.8.1 TFT Timing

Signal	Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK	CLK frequency	Fclk	50	66.77	80	MHz	
HSYNC	Horizontal Line	Th	825	880	1056	CLK	
	HS Display Area	Thd	-	800	-	CLK	
	HS Pulse Width	Thpw	4	16	20	CLK	
	HS Back Porch	Thb	8	48	88	CLK	
	HS Front Porch	Thfp	2	16	28	CLK	
VSYNC	VS Period Time	Tv	1288	1296	1330	th	
	VS Display Area	Tvd	-	1280	-	th	
	VS Pulse Width	Tvpw	2	4	6	th	
	VS Back Porch	Tvb	2	4	10	th	
	VS Front Porch	Tvfp	2	8	10	th	

7.9 Reset Timing

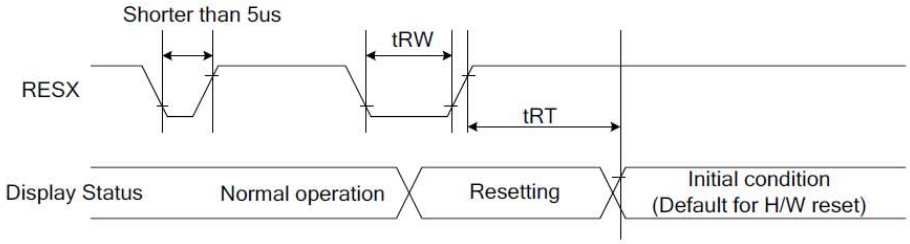


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

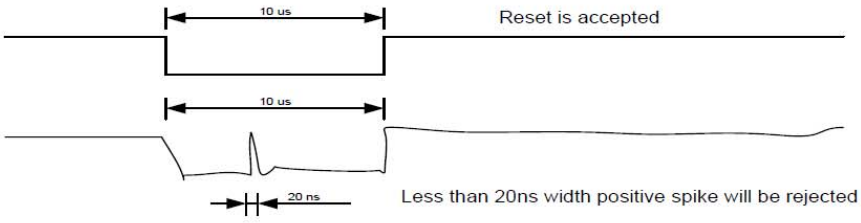


Figure 125: Positive Noise Pulse during Reset Low

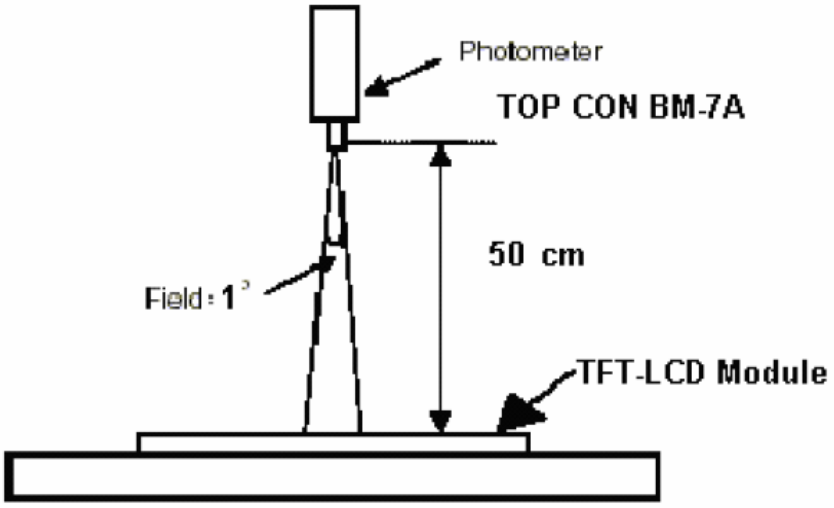
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Brightness		--	Note1, Note 3, ($\theta = 0^\circ$, Normal Viewing	360	450	--	cd/m^2
Uniformity		B-uni		--	80	--	%
Contrast Ratio		CR		1200	1500	--	
Response Time		Tr+Tf		--	30	35	ms
Color Chromaticity	White	Wx		0.260	0.310	0.360	
		Wy		0.275	0.325	0.375	
View angle	Horizontal	θ x+	Center CR≥10	75	80	--	
		θ x-		75	80	--	
	Vertical	θ Y+		75	80	--	
		θ Y-		75	80	--	

Note：The following optical specifications shall be measured in a darkroom or equivalent state(ambient luminance ≤1 lux, and at room temperature). The operation temperature is 25°C±2°C. The measurement method is shown in Note1.

Note1: The method of optical measurement:

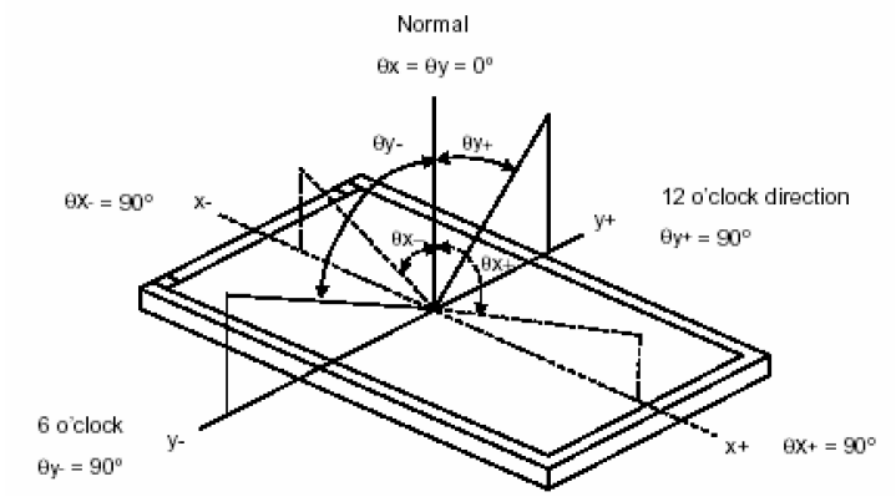


Note2: Measured at the center area of the panel and at the viewing angle of the θ x= θ y =0°

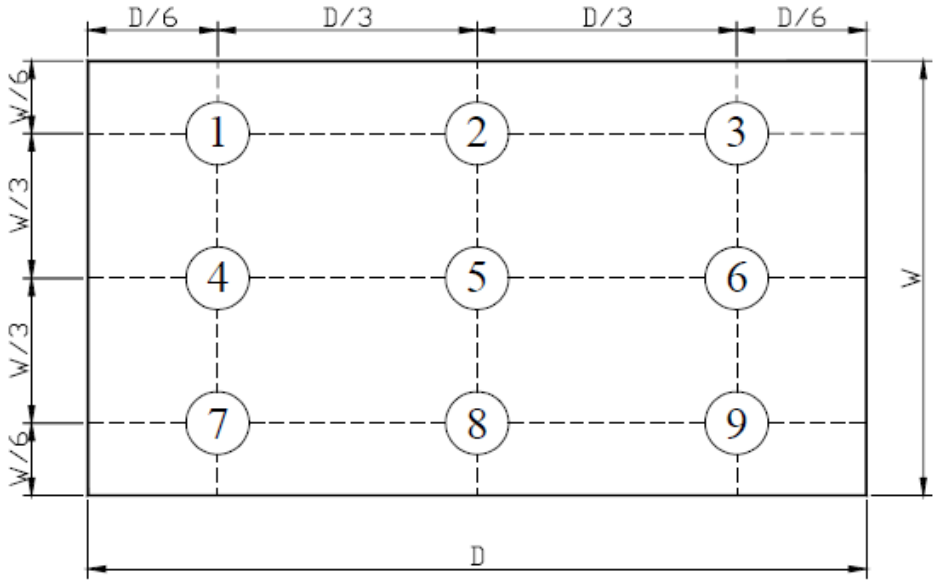
Note3: Definition of Contrast Ratio (CR):

CR = Luminance with all pixels in white state ÷ Luminance with all pixels in Black state

Note 4: Definition of Viewing Angle:



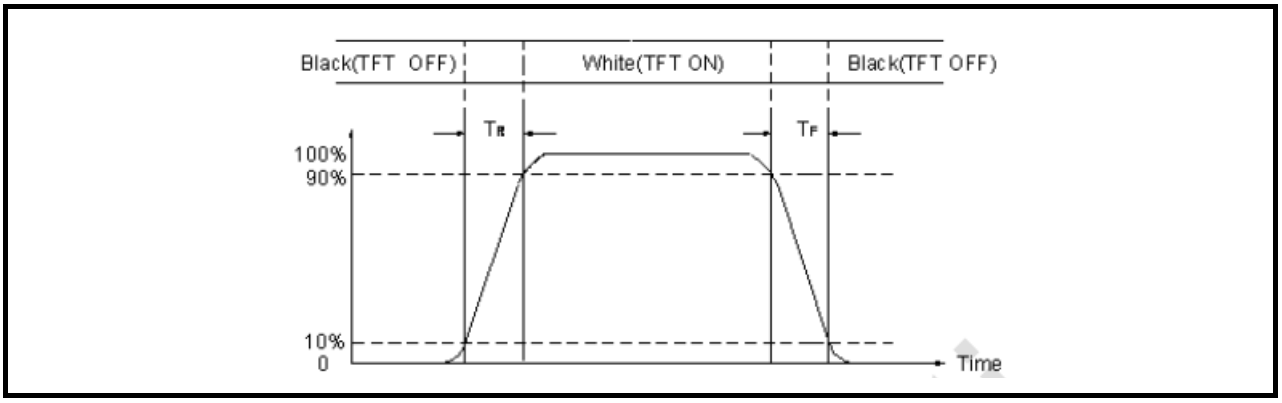
Note 5: Definition of Brightness Uniformity (B-uni):



B-uni ＝(Minimum luminance of 9 points÷Maximum luminance of 9points)X100%

Note 6: Definition of Response Time:

The Response Time is set initially by defining the “Rising Time (Tr)” and the “Falling Time (Tf)” respectively. Tr and Tf are defined as following figure



Note 7: Definition of Chromaticity:

The color coordinates (Wx,Wy),(Rx,Ry),(Gx,Gy),and (Bx,By) are obtained with all pixels in the viewing field at white, red, green, and blue states, respectively.

9. RELIABILITY

9.1 Test Condition

9.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 25 ± 5°C

Humidity : 65 ± 5%

9.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

9.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

9.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

9.2 TESTS

No.	ITEM	CONDITION CRITERION
1	High Temperature Storage	70°C, 120 hrs
2	Low Temperature Storage	-20°C, 120 hrs
3	High Temperature Operating	60°C, 120 hrs
4	Low Temperature Operating	-10°C, 120 hrs
5	High Temperature/Humidity Non-Operating	40°C, 90%RH, 120 hrs
6	Temperature Shock Non-Operating	-20°C ←→ 70°C (0.5hr each), 25 cycles
7	Vibration Test Non-Operating	Frequency:0 ~ 55 Hz Amplitude:1.5 mm Sweep Time:11min Test Period:6 Cycles for each Direction of X,Y,Z

Note1: The test sample have recovery time for 24 hours at room temperature before the function check. In the standard conditions, there is no any touch panel function NG issue occurred.

9.3 JUDGMENT STANDARD

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect. Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.

9.4 INCOMING INSPECTION STANDARDS

<table>
<tr><th>No.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td rowspan="2">1</td><td rowspan="2">Operating</td><td>
Display function: No Display malfunction (Major)
Contrast ratio (Black, White):
Does not meet specified range in the spec. (Major) (Note:3)
Line Defect: No obvious Vertical and Horizontal line defect in bright, dark and colored. (Major) (Note:1)
Point Defect : Active area ≤ 5 dots (Minor) (Note:1)
<table>
<tr><th rowspan="2">Item</th><th>Acceptable number</th><th rowspan="2">Total</th></tr>
<tr><th>Active Area</th></tr>
<tr><td>Bright</td><td>2</td><td rowspan="2">5</td></tr>
<tr><td>Dark</td><td>4</td></tr>
</table>
</td></tr>
<tr><td>
Non-uniformity: Visible through 5%ND filter. (Minor)
Foreign material in Black or White spots shape (W>1/4L)
<table>
<tr><th>Zone / Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>D> 0.5</td><td>0</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>0.3 < D ≤ 0.5</td><td>5</td></tr>
<tr><td>D ≤ 0.3</td><td>*</td></tr>
</table>
D = (Long + Short) / 2 ＊ : Disregard
Foreign Material in Line or spiral shape (W≤1/4L) (Note: 4)
<table>
<tr><th>L (mm) / Zone W(mm)</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>L >5</td><td>W>0.1</td><td>0</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>0.5 < L ≤ 5</td><td>0.03 < W≤0.1</td><td>5</td></tr>
<tr><td>L ≤0.5</td><td>W≤0.03</td><td>*</td></tr>
</table>
L : Length W : Width ＊ : Disregard
</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">External Inspection (non-operating)</td><td>
Dimension: Outline (Major)
Bezel appearance: uneven (Minor)
Scratch on the polarize: (Note:2)
<table>
<tr><th>L (mm) / Zone W(mm)</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>--</td><td>W>0.1</td><td>0</td><td rowspan="2">Minor</td><td rowspan="2">1.5</td></tr>
<tr><td>L ≤ 3</td><td>W≤0.1</td><td>3</td></tr>
</table>
L : Length W : Width ＊ : Disregard
</td></tr>
<tr><td>
Dent or bubble on the polarize (Note:2)
<table>
<tr><th>Zone / Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>D≤0.3</td><td>*</td><td rowspan="2">Minor</td><td rowspan="2">1.5</td></tr>
<tr><td>D≤0.5</td><td>3</td></tr>
</table>
D = (Long + Short) / 2 ＊ : Disregard
</td></tr>
</table>

Class of defects	**Major**	AQL 0.65%	**Definition** It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.
	Minor	AQL 1.5%	It is a defect that will not result in functioning problem with deviation classified.

Note1:

(a)Bright point defect is defined as point defect of R,G,B with area >1/2 pixel respectively

(b)Dark point defect is defined as visible in full white pattern.

(c)Definition of distribution of point defect is as follows:

-minimum separation between dark point defects should be larger than 5mm.

-minimum separation between bright point defects should be larger than 5mm.

(d)Definition of joined bright point defect and joined dark point defect are as follows:

-Two or more joined bright point defects must be nil.

-Three joined dark point defects must be nil.

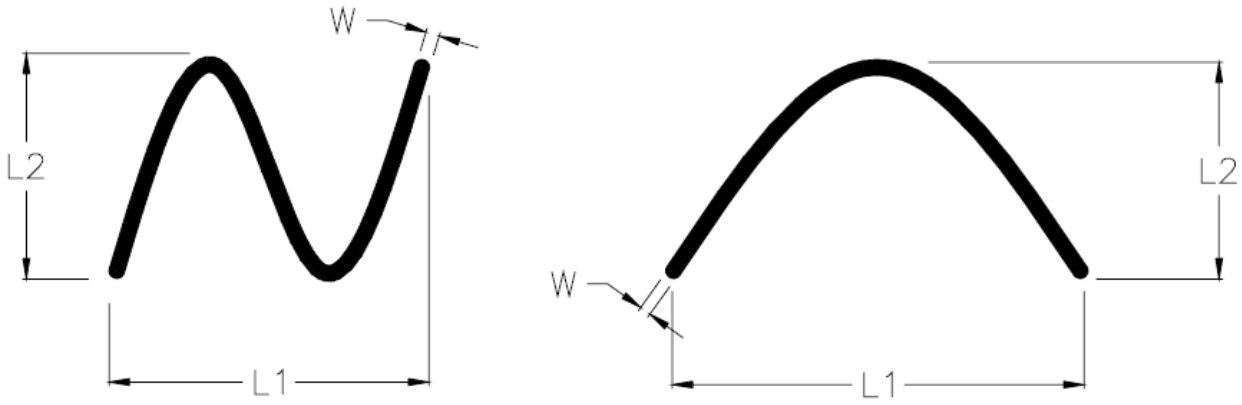
-Coupling of one dark and one bright point in junction is counted as one dark and bright spot with 1 pair maximum.

-Two Joined dark point is counted as two dark points with 2 pair maximum.

Note2: The external inspection should be conducted at the distance 30± 5cm between the eyes of inspector and the panel.

Note3: Luminance measurement for contrast ratio is at the distance 50± 5cm between the detective head and the panel with ambient luminance less than 1 lux. Contrast ratio is obtained at optimum view angle.

Note4: W-Width in mm , L-length of Max.(L1,L2) in mm.



9.5 Sampling Condition

Unless otherwise agree in written, the sampling inspection shall be applied to the incoming inspection of customer.

Lot size: Quantity of shipment lot per model.

Sampling type: normal inspection, single sampling

Sampling table: MIL-STD-105E

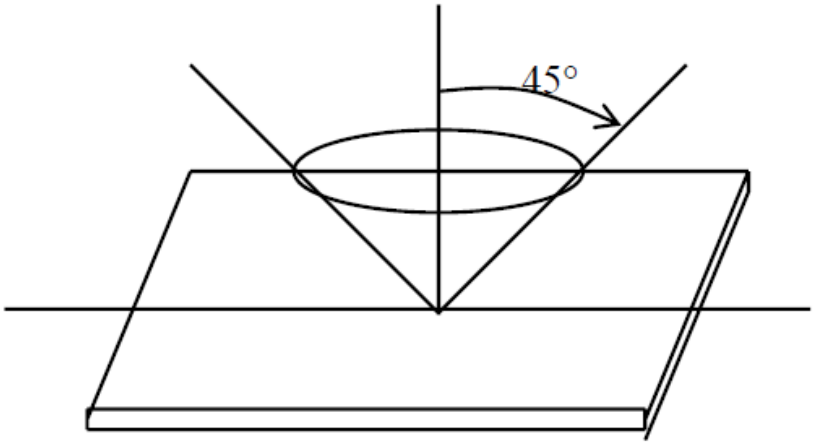
Inspection level: Level II

9.6 Inspection conditions

The LCD shall be inspected under 40W white fluorescent light.

$\theta \leq 45^{\circ}$ inspection under non-operating condition.

$\theta \leq 5^{\circ}$ inspection under operating condition



10. PRECAUTION RELATING PRODUCT HANDLING

10.1 SAFETY

10.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.

10.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

10.2 HANDLING

10.2.1 Avoid any strong mechanical shock which can break the glass.

10.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module, be sure to ground your body and any electrical equipment you may be using.

10.2.3 Do not remove the panel or frame from the module.

10.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully, Do not touch, push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)

10.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

10.2.6 Do not touch the display area with bare hands , this will stain the display area.

10.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

10.2.8 To control temperature and time of soldering is 280 ± 10°C and 3-5 sec.

10.2.9 To avoid liquid (include organic solvent) stained on LCM.

10.3 STORAGE

10.3.1 Store the panel or module in a dark place where the temperature is 25°C ± 5°C and the humidity is below 65% RH.

10.3.2 Do not place the module near organics solvents or corrosive gases.

10.3.3 Do not crush, shake, or jolt the module.