

RoHS Compliant

8GB DDR4 SDRAM SO-DIMM Industrial

Halogen free

Product Specifications

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Version 0.2



Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan

Tel: +886-2-2267-8000

Fax: +886-2-2267-2261

www.apacer.com

General Description

Apacer **75.CA4GR.G000B** is a 1024M x 64 DDR4 SDRAM (Synchronous DRAM) SO-DIMM. This high-density memory module consists of 8 pieces 1024M x 8 bits with 4 banks DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 260-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
75.CA4GR.G000B	17 GB/sec	2133 Mbps	1066 MHz	CL15

Density	Organization	Component	Rank
8GB	1024M x 64	1024M x8*8	1

Key Parameters

MT/s	DDR4-1866	DDR4-2133	DDR4-2400	Unit
Grade	-CL13	-CL15	-CL17	
tCK (min)	1.07	0.93	0.83	ns
CAS latency	13	15	17	tCK
tRCD (min)	13.92	14.06	14.16	ns
tRP (min)	13.92	14.06	14.16	ns
tRAS (min)	34	33	32	ns
tRC (min)	47.92	47.05	46.16	ns
CL-tRCD-tRP	13-13-13	15-15-15	17-17-17	tCK

Specifications:

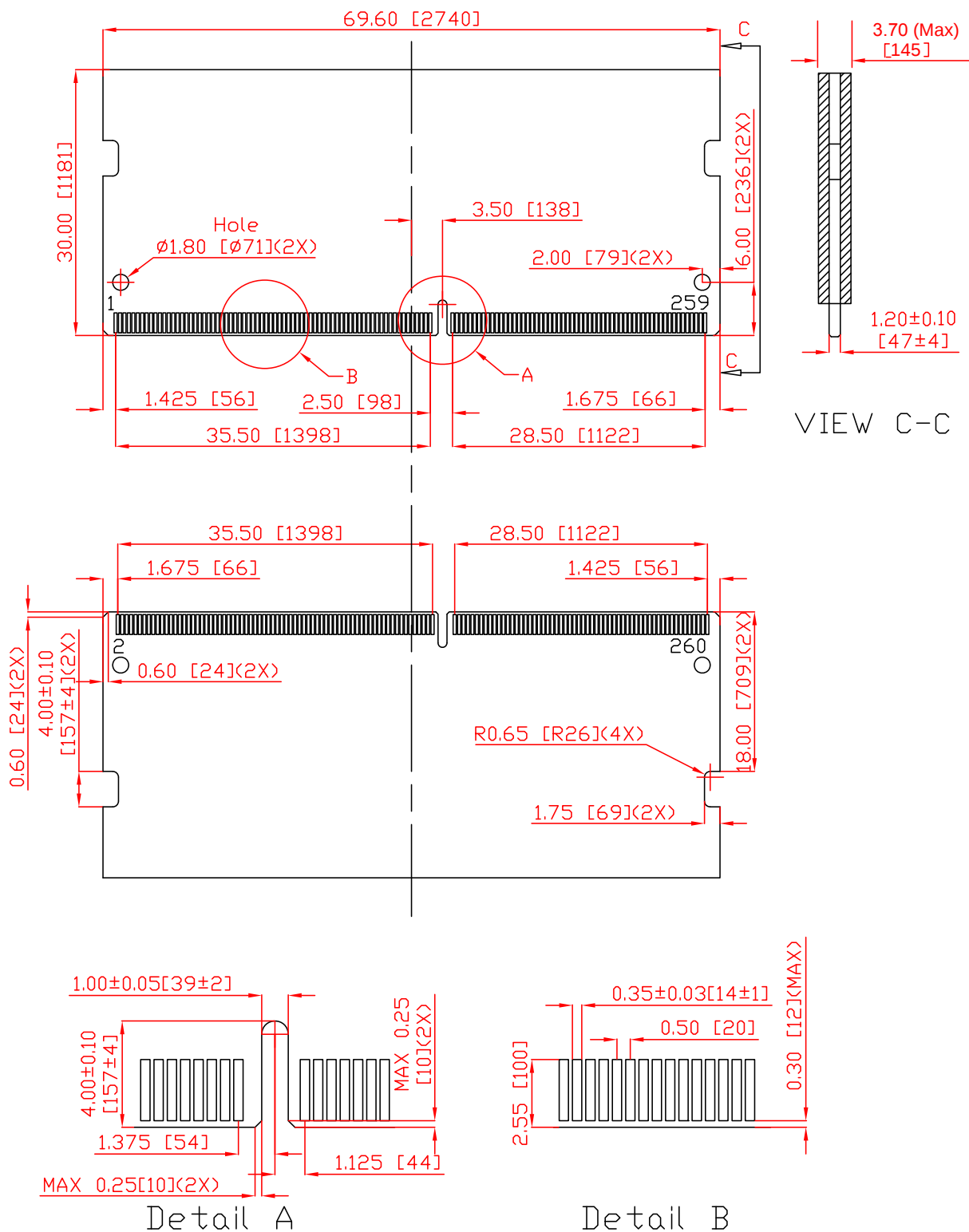
- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 1024 words x 64 bits, 1 rank
- ◆ Integrating 8 pieces of 8G bits DDR4 SDRAM sealed FBGA
- ◆ Package: 260-pin socket type small outline dual in-line memory module (SO-DIMM)
- ◆ PCB: height 30.00 mm, lead pitch 0.50 mm (pin),
- ◆ Serial Presence Detect (SPD)
- ◆ Power Supply: VDD=1.2V (1.14V to 1.26V)
- ◆ VDDQ = 1.2V (1.14V to 1.26V)
- ◆ VPP = 2.5V (2.375V to 2.75V)
- ◆ VDDSPD = 2.2V to 3.6V
- ◆ 16 internal banks (4 Bank Groups)
- ◆ CAS Latency (CL): 10, 11, 12, 13, 14, 15
- ◆ CAS Write Latency (CWL): 9, 10, 11, 12, 14
- ◆ Support Industrial Temp (-40°C~95°C)
 - tREFI 7.8us at -40 °C ≤ TCASE ≤ 85°C
 - tREFI 3.9us at 85 °C < TCASE ≤ 95°C
- ◆ Lead-free (RoHS compliant)
- ◆ Halogen free
- ◆ PCB: 30μ gold finger

Features:

- ◆ Functionality and operations comply with the DDR4 SDRAM datasheet
- ◆ Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- ◆ Bi-Directional Differential Data Strobe
- ◆ 8 bit pre-fetch
- ◆ Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- ◆ Per DRAM Addressability is supported
- ◆ Internal Vref DQ level generation is available
- ◆ Write CRC is supported at all speed grades
- ◆ DBI (Data Bus Inversion) is supported(x8)
- ◆ CA parity (Command/Address Parity) mode is supported

Mechanical Drawing

Unit: mm



30 μ gold finger

(All dimensions are in millimeters with ± 0.15 mm tolerance unless specified otherwise.)

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist.,

New Taipei City 236, Taiwan R.O.C.

Tel: +886-2-2267-8000

Fax: +886-2-2267-2261

amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.

46732 Lakeview Blvd., Fremont, CA 94538

Tel: 1-408-518-8699

Fax: 1-510-249-9568

sa@apacerus.com

Japan

Apacer Technology Corp.

5F, Matsura Bldg., Shiba, Minato-Ku

Tokyo, 105-0014, Japan

Tel: 81-3-5419-2668

Fax: 81-3-5419-0018

jpservices@apacer.com

Europe

Apacer Technology B.V.

Science Park Eindhoven 5051 5692 EB Son,

The Netherlands

Tel: 31-40-267-0000

Fax: 31-40-290-0686

sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd.

Room D, 22/FL, No.2, Lane 600, Jieyun Plaza,

Tianshan RD, Shanghai, 200051, China

Tel: 86-21-6228-9939

Fax: 86-21-6228-9936

sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd.

Unit No.201, "Brigade Corner", 7th Block Jayanagar,

Yediyur Circle, Bangalore – 560082, India

Tel: 91-80-4152-9061

Fax: 91-80-4170-0215

sales_india@apacer.com