Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 54 Powerful Instructions – Most Single Clock Cycle Execution
  - 16 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 12 MIPS Throughput at 12 MHz
- Non-volatile Program and Data Memories
  - 4K Bytes of In-System Programmable Flash Program Memory
  - 256 Bytes Internal SRAM
  - Flash Write/Erase Cycles: 10,000
  - Data Retention: 20 Years at 85°C / 100 Years at 25°C
- Peripheral Features
  - One 8-bit Timer/Counter with Two PWM Channels
  - One 8/16-bit Timer/Counter
  - 10-bit Analog to Digital Converter
    - 12 Single-Ended Channels
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Master/Slave SPI Serial Interface
  - Slave TWI Serial Interface
- Special Microcontroller Features
  - In-System Programmable
  - External and Internal Interrupt Sources
  - Low Power Idle, ADC Noise Reduction, Stand-by and Power-down Modes
  - Enhanced Power-on Reset Circuit
  - Internal Calibrated Oscillator
- I/O and Packages
  - 20-pin SOIC/TSSOP: 18 Programmable I/O Lines
  - 20-pad VQFN/MLF: 18 Programmable I/O Lines
- Operating Voltage:
  - 1.8 – 5.5V
- Programming Voltage:
  - 5V
- Speed Grade
  - 0 – 4 MHz @ 1.8 – 5.5V
  - 0 – 8 MHz @ 2.7 – 5.5V
  - 0 – 12 MHz @ 4.5 – 5.5V
- Industrial Temperature Range
- Low Power Consumption
  - Active Mode:
    - 200 µA at 1 MHz and 1.8V
  - Idle Mode:
    - 25 µA at 1 MHz and 1.8V
  - Power-down Mode:
    - < 0.1 µA at 1.8V

8-bit AVR® Microcontroller with 4K Bytes In-System Programmable Flash

ATtiny40

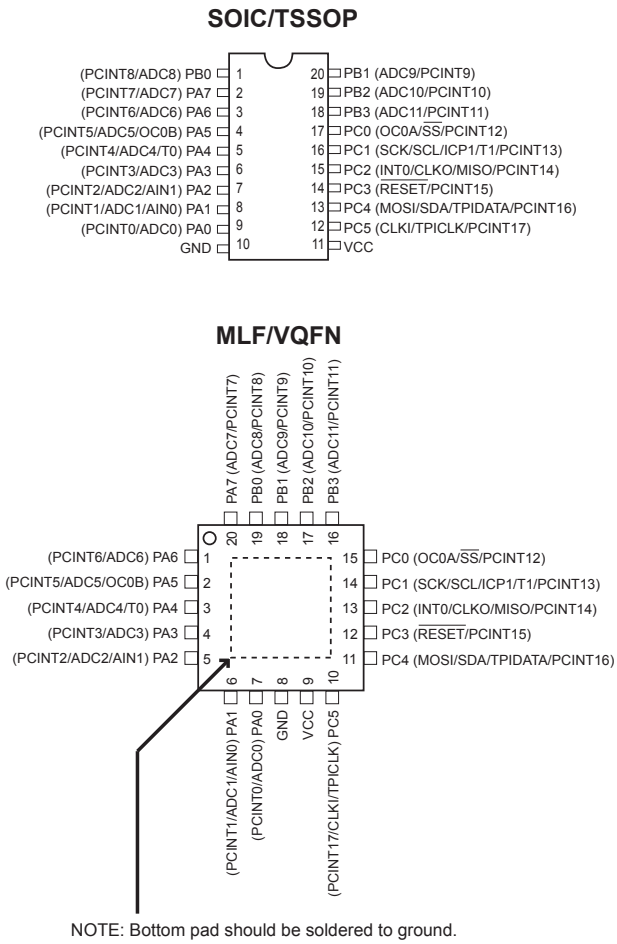
Preliminary

Summary

Rev. 8263AS–AVR–08/10

1. Pin Configurations

Figure 1-1. Pinout of ATtiny40



NOTE: Bottom pad should be soldered to ground.

1.1 Pin Description

1.1.1 VCC

Supply voltage.

1.1.2 GND

Ground.

1.1.3 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in Table 21-4 on page 168. Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

1.1.4 Port A (PA7:PA0)

Port A is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A has alternate functions as analog inputs for the ADC, analog comparator and pin change interrupt as described in “Alternate Port Functions” on page 52.

1.1.5 Port B (PB3:PB0)

Port B is a 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

The port also serves the functions of various special features of the ATtiny40, as listed on page 41.

1.1.6 Port C (PC5:PC0)

Port C is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability except PC3 which has the $\overline{\text{RESET}}$ capability. To use pin PC3 as an I/O pin, instead of RESET pin, program (‘0’) RSTDISBL fuse. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

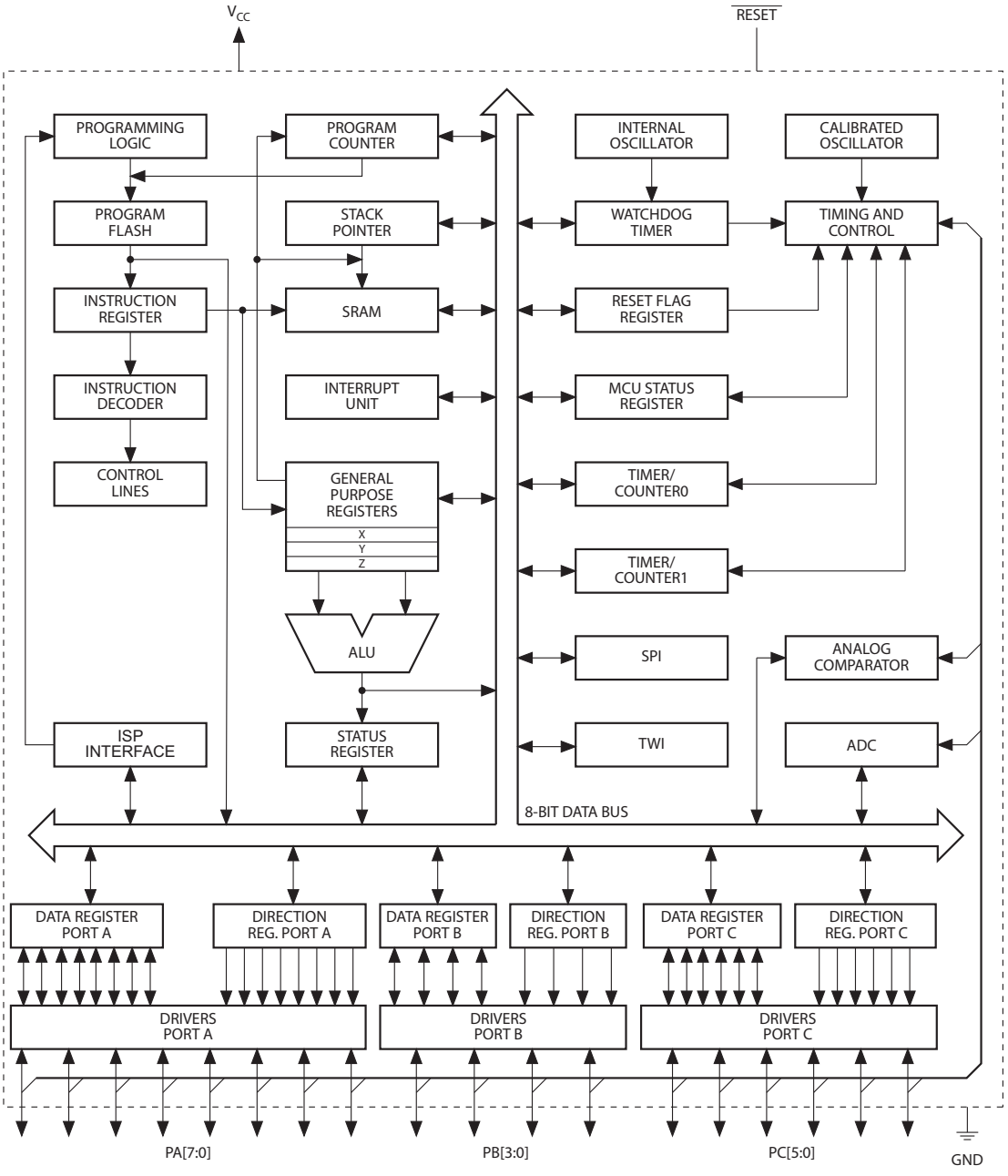
Port C has alternate functions as analog inputs for the ADC, analog comparator and pin change interrupt as described in “Alternate Port Functions” on page 52.

The port also serves the functions of various special features of the ATtiny40, as listed on page 41.

2. Overview

ATtiny40 is a low-power CMOS 8-bit microcontroller based on the compact AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny40 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 16 general purpose working registers and system registers. All registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The resulting architecture is compact and code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny40 provides the following features: 4K bytes of In-System Programmable Flash, 256 bytes of SRAM, twelve general purpose I/O lines, 16 general purpose working registers, an 8-bit Timer/Counter with two PWM channels, a 8/16-bit Timer/Counter, Internal and External Interrupts, an eight-channel, 10-bit ADC, a programmable Watchdog Timer with internal oscillator, a slave two-wire interface, a master/slave serial peripheral interface, an internal calibrated oscillator, and four software selectable power saving modes.

Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and interrupt system to continue functioning. ADC Noise Reduction mode minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC. In Power-down mode registers keep their contents and all chip functions are disabled until the next interrupt or hardware reset. In Standby mode, the oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip, in-system programmable Flash allows program memory to be re-programmed in-system by a conventional, non-volatile memory programmer.

The ATtiny40 AVR is supported by a suite of program and system development tools, including macro assemblers and evaluation kits.

3. General Information

3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at http://www.atmel.com/avr.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

3.4 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device has been characterized.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F	SREG	I	T	H	S	V	N	Z	C	Page 14
0x3E	SPH	Stack Pointer High Byte								Page 13
0x3D	SPL	Stack Pointer Low Byte								Page 13
0x3C	CCP	CPU Change Protection Register								Page 13
0x3B	RSTFLR	–	–	–	–	WDRF	BORF	EXTRF	PORF	Page 39
0x3A	MCUCR	ISC01	ISC00	–	BODS	SM2	SM1	SM0	SE	Pages 30, 43
0x39	OSCCAL	Oscillator Calibration Register								Page 25
0x38	Reserved	–								
0x37	CLKMSR	–	–	–	–	–	–	CLKMS1	CLKMS0	Page 24
0x36	CLKPSR	–	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	Page 24
0x35	PRR	–	–	–	PRTWI	PRSPI	PRTIM1	PRTIM0	PRADC	Page 31
0x34	QTCSR	QTouch Control and Status Register								Page 144
0x33	NVMCMD	–	–	NVM Command Register						Page 164
0x32	NVMCSR	NVMBSY	–	–	–	–	–	–	–	Page 164
0x31	WDTCSR	WDIF	WDIE	WDP3	–	WDE	WDP2	WDP1	WDP0	Page 37
0x30	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	Page 128
0x2F	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	Page 130
0x2E	SPDR	SPI Data Register								Page 130
0x2D	TWSCRA	TWSHE	–	TWDIE	TWASIE	TWEN	TWSIE	TWPME	TWSME	Page 139
0x2C	TWSCRB	–	–	–	–	–	TWAA	TWCMD[1.0]		Page 140
0x2B	TWSSRA	TWDIF	TWASIF	TWCH	TWRA	TWC	TWBE	TWDIR	TWAS	Page 141
0x2A	TWSA	TWI Slave Address Register								Page 142
0x29	TWSAM	TWI Slave Address Mask Register								Page 143
0x28	TWSD	TWI Slave Data Register								Page 143
0x27	TCNT1H	Timer/Counter1 – Counter Register High Byte								Page 95
0x26	TIMSK	ICIE1	–	OCIE1B	OCIE1A	TOIE1	OCIE0B	OCIE0A	TOIE0	Pages 81, 96
0x25	TIFR	ICF1	–	OCF1B	OCF1A	TOV1	OCF0B	OCF0A	TOV0	Pages 81, 97
0x24	TCCR1A	TCW1	ICEN1	ICNC1	ICES1	CTC1	CS12	CS11	CS10	Page 94
0x23	TCNT1L	Timer/Counter1 – Counter Register Low Byte								Page 95
0x22	OCR1A	Timer/Counter1 – Compare Register A								Page 95
0x21	OCR1B	Timer/Counter1 – Compare Register B								Page 96
0x20	RAMAR	RAM Address Register								Page 19
0x1F	RAMDR	RAM Data Register								Page 19
0x1E	PUEC	–	–	PUEC5	PUEC4	PUEC3	PUEC2	PUEC1	PUEC0	Page 64
0x1D	PORTC	–	–	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	Page 64
0x1C	DDRC	–	–	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0	Page 64
0x1B	PINC	–	–	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	Page 64
0x1A	PCMSK2	–	–	PCINT17	PCINT16	PCINT15	PCINT14	PCINT13	PCINT12	Page 45
0x19	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	Page 76
0x18	TCCR0B	FOC0A	FOC0B	TSM	PSR	WGM02	CS02	CS01	CS00	Pages 79, 100
0x17	TCNT0	Timer/Counter0 – Counter Register								Page 80
0x16	OCR0A	Timer/Counter0 – Compare Register A								Page 80
0x15	OCR0B	Timer/Counter0 – Compare Register B								Page 81
0x14	ACSRA	ACD	ACBG/ACIRE	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	Page 102
0x13	ACSRB	HSEL	HLEV	ACLP	–	ACCE	ACME	ACIRS1	ACIRS0	Page 103
0x12	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	Page 119
0x11	ADCSRB	VDEN	VDPD	–	–	ADLAR	ADTS2	ADTS1	ADTS0	Page 120
0x10	ADMUX	–	REFS	REFEN	ADC0EN	MUX3	MUX2	MUX1	MUX0	Page 117
0x0F	ADCH	ADC Conversion Result – High Byte								Page 118
0x0E	ADCL	ADC Conversion Result – Low Byte								Page 118
0x0D	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	Pages 104, 121
0x0C	GIMSK	–	PCIE2	PCIE1	PCIE0	–	–	–	INT0	Page 43
0x0B	GIFR	–	PCIF2	PCIF1	PCIF0	–	–	–	INTF0	Page 44
0x0A	PCMSK1	–	–	–	–	PCINT11	PCINT10	PCINT9	PCINT8	Page 45
0x09	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	Page 45
0x08	PORTCR	ADC11D	ADC10D	ADC9D	ADC8D	–	BBMC	BBMB	BBMA	Pages 62, 121
0x07	PUEB	–	–	–	–	PUEB3	PUEB2	PUEB1	PUEB0	Page 63
0x06	PORTB	–	–	–	–	PORTB3	PORTB2	PORTB1	PORTB0	Page 63
0x05	DDRB	–	–	–	–	DDRB3	DDRB2	DDRB1	DDRB0	Page 63
0x04	PINB	–	–	–	–	PINB3	PINB2	PINB1	PINB0	Page 64
0x03	PUEA	PUEA7	PUEA6	PUEA5	PUEA4	PUEA3	PUEA2	PUEA1	PUEA0	Page 63
0x02	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	Page 63
0x01	DDRA	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0	Page 63
0x00	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	Page 63

Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One's Complement	Rd ← $FF – Rd	Z,C,N,V,S	1
NEG	Rd	Two's Complement	Rd ← $00 – Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3/4
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	3/4
RET		Subroutine Return	PC ← STACK	None	4/5
RETI		Interrupt Return	PC ← STACK	I	4/5
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd – K	Z, C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	A, b	Skip if Bit in I/O Register is Set	if (I/O(A,b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow.	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	1/2
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Decrement	X ← X - 1, Rd ← (X)	None	2/3
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	1/2
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Decrement	Y ← Y - 1, Rd ← (Y)	None	2/3
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1/2
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2/3
LDS	Rd, k	Store Direct from SRAM	Rd ← (k)	None	1
ST	X, Rr	Store Indirect	(X) ← Rr	None	1
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1
ST	- X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1
ST	- Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1
ST	Z+, Rr	Store Indirect and Post-Increment.	(Z) ← Rr, Z ← Z + 1	None	1
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1, (Z) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	1
IN	Rd, A	In from I/O Location	Rd ← I/O (A)	None	1
OUT	A, Rr	Out to I/O Location	I/O (A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
BREAK		Break	(see specific descr. for Break)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

6. Ordering Information

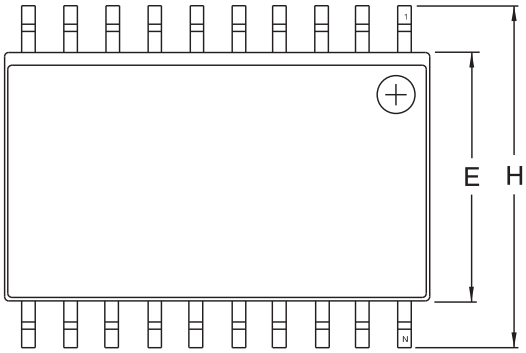
Speed (MHz)	Power Supply (V)	Ordering Code[1]	Package[2]	Operational Range
12	1.8 - 5.5	ATtiny40-SU ATtiny40-SUR ATtiny40-XU ATtiny40-XUR ATtiny40-MMH[3] ATtiny40-MMHR[3]	20S2 20S2 20X 20X 20M2[3] 20M2[3]	Industrial (-40°C to +85°C)[4]

Notes:
1. Code indicators:
   - H: NiPdAu lead finish
   - U: matte tin
   - R: tape & reel
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. Topside marking for ATtiny40:
   - 1st Line: T40
   - 2nd Line: xx
   - 3rd Line: xxx
4. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

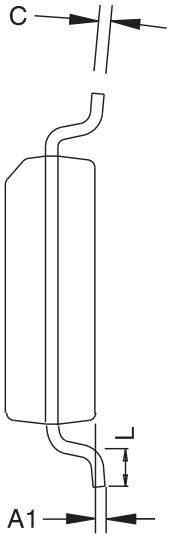
Package Type	
20S2	20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
20X	20-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
20M2	20-pad, 3 x 3 x 0.85 mm Body, Very Thin Quad Flat No Lead Package (VQFN)

7. Packaging Information

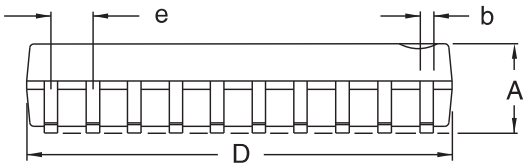
7.1 20S2



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

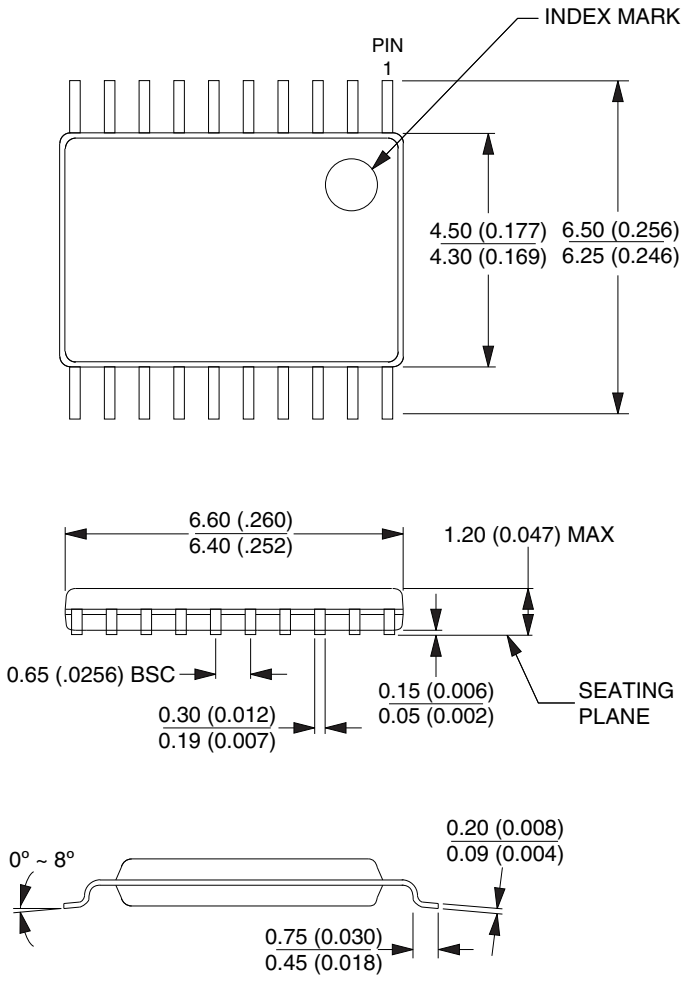
Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

11/6/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	B

7.2 20X

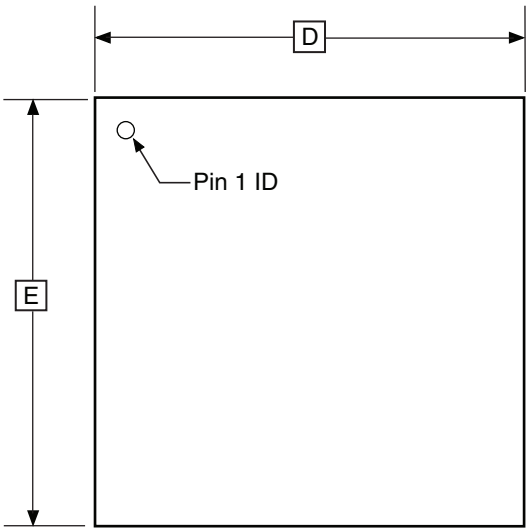
Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC



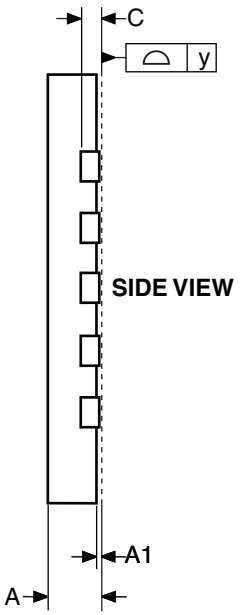
10/23/03

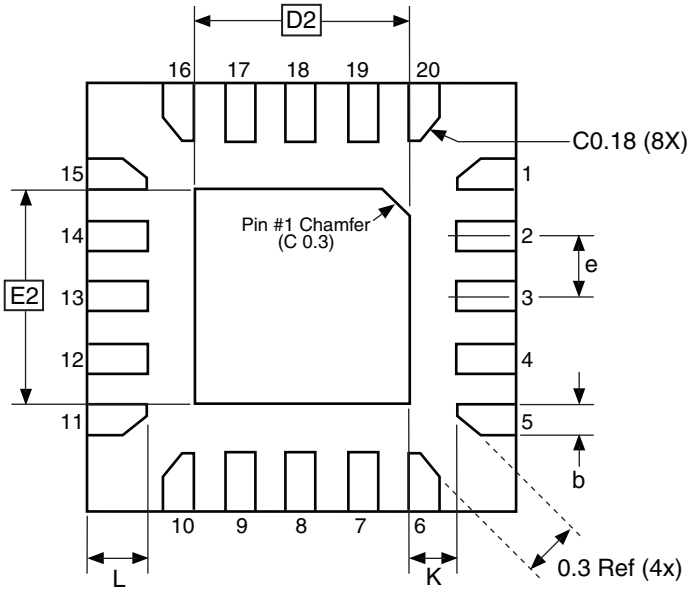
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	20X	C

7.3 20M2



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.75	0.80	0.85	
A1	0.00	0.02	0.05	
b	0.17	0.22	0.27	
C		0.152		
D	2.90	3.00	3.10	
D2	1.40	1.55	1.70	
E	2.90	3.00	3.10	
E2	1.40	1.55	1.70	
e	–	0.45	–	
L	0.35	0.40	0.45	
K	0.20	–	–	
y	0.00	–	0.08	

10/24/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**20M2,** 20-pad, 3 x 3 x 0.85 mm Body, Lead Pitch 0.45 mm, 1.55 x 1.55 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	ZFC	20M2	B

8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny40 device.

8.1 Rev. B

No known errata.

8.2 Rev. A

Not sampled.

9. Datasheet Revision History

9.1 Rev. 8263A – 08/10

1. Initial revision. Copied and modified from 8235_t20.

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