

**DISPLAY Elektronik GmbH**

**DATA SHEET**

**LCD MODULE**

**DEM 240128A1 ADX-PW-N**

*Product Specification*

*Version : 2*

**30.11.2021**

# GENERAL SPECIFICATION

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MODULE NO. :

**DEM 240128A1 ADX-PW-N**

CUSTOMER P/N:

| Version NO. | Change Description                                   | Date       |
|-------------|--|------------|
| 0           | Original Version                                     | 22.11.2021 |
| 1           | Correct the op. and st. temp. on page 7 and page 14. | 25.11.2021 |
| 2           | Correct the LCD No. on page 2.                       | 30.11.2021 |
|             |  |            |
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PREPARED BY: PS

DATE: 30.11.2021

APPROVED BY: WH

DATE: 30.11.2021

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**1. FUNCTIONS & FEATURES**

┆ DEM 240128A1 Series LCD Type :

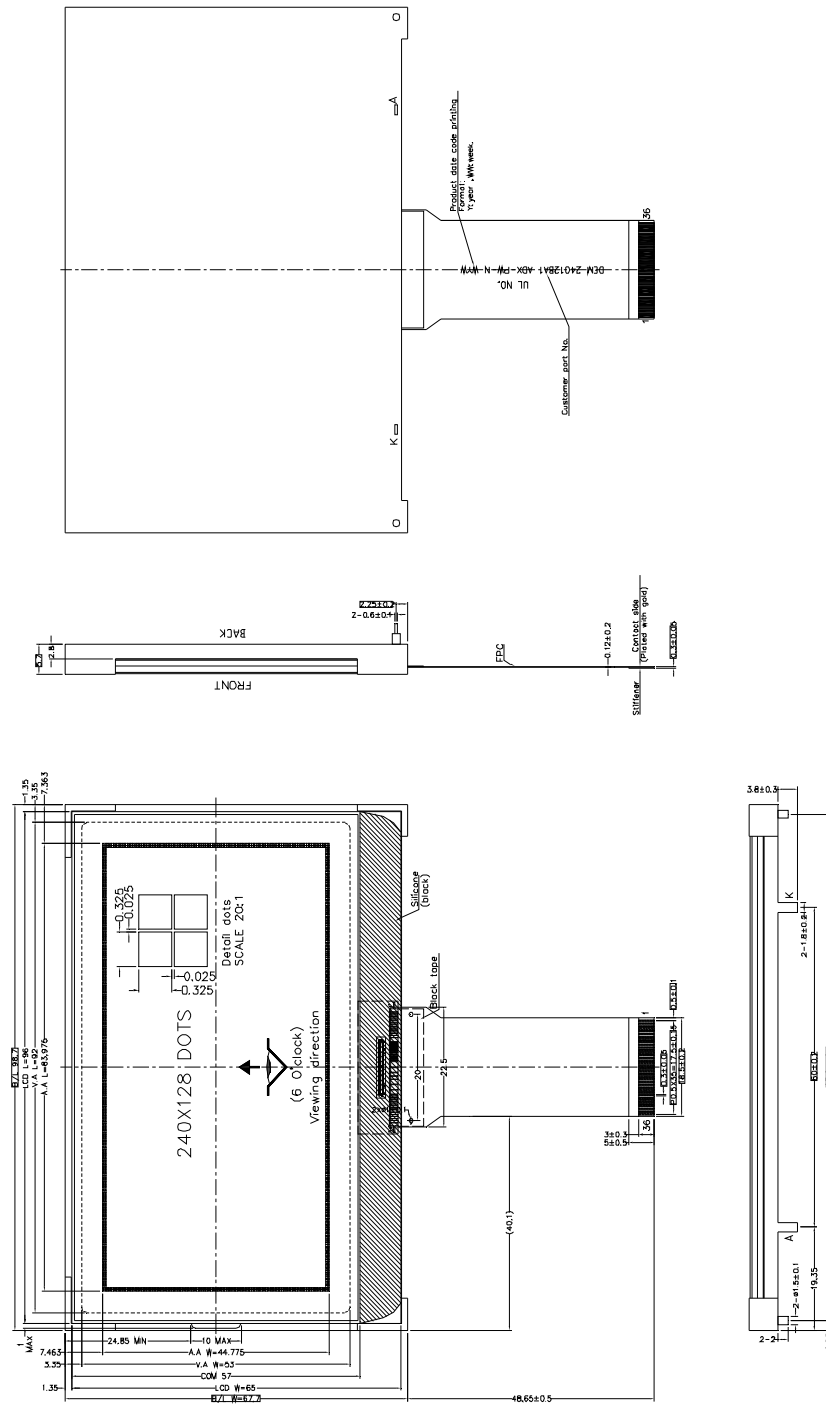
| <b>Module</b>            | <b>LCD Type</b>                 | <b>Remark</b> |
|--------------------------|---------------------------------|---------------|
| DEM 240128A1<br>ADX-PW-N | ASTN Transmissive Negative Mode |               |

- ┆ Viewing Direction : 6 O'clock
- ┆ Driving Scheme : 1/128Duty Cycle, 1/12 Bias
- ┆ Power Supply Voltage : 3.0 V
- ┆ LCD Operation Voltage : 14.5V
- ┆ Driver IC : ST7529A
- ┆ Display Contents : 240 x 128 Dots
- ┆ RoHS Compliant

**2. MECHANICAL SPECIFICATIONS**

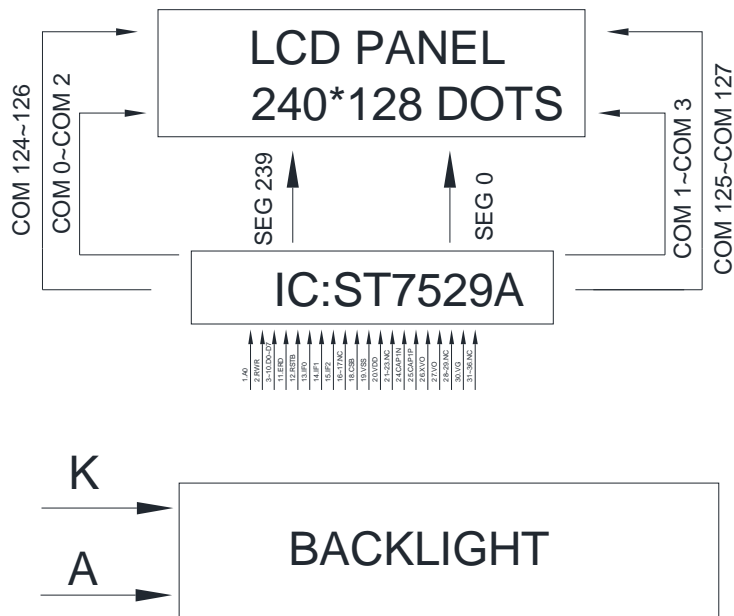
- ┆ Module Size(Without FPC) : 98.70 x 67.70 x 5.70 mm
- ┆ View Area : 92.00 x 53.00 mm
- ┆ Active Area : 83.975 x 44.775 mm
- ┆ Dot Size : 0.325 x 0.325 mm
- ┆ Dot Pitch : 0.35 x 0.35 mm

3. EXTERNAL DIMENSIONS



Remarks:  
 1. Unmarked tolerance is  $\pm 0.3$   
 2. All materials comply with RoHS  
 3. [ ]: critical dimension.

4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

| Pin No.   | Name           | Description   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
|---|----------------|---|--------------------------|---|--------------------------|--------------------|----|---|-------------|--------------------------|--|---|---|--------------------------|---|---|---|-----------------------|
| 1   | A <sub>0</sub> | Register select input pin<br>A0 = "H": DB0 to DB7 or SI are display data<br>A0 = "L": DB0 to DB7 or SI are control data<br>There is no A0 pin in 3-Line SPI interface. A0 should be fixed to "H" by VDD1.   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 2   | RWR            | Read / Write execution control pin  |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
|   |                | <table border="1"> <thead> <tr> <th>MPU type</th> <th>RWR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>6800-series</td> <td>RW</td> <td>Read / Write control input pin<br/>RW = "H" : read<br/>RW = "L" : write</td> </tr> <tr> <td>8080-series</td> <td>/WR</td> <td>Write enable clock input pin<br/>The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td> </tr> </tbody> </table>   | MPU type                 | RWR   | Description              | 6800-series        | RW | Read / Write control input pin<br>RW = "H" : read<br>RW = "L" : write   | 8080-series | /WR                      | Write enable clock input pin<br>The data on DB0 to DB7 are latched at the rising edge of the /WR signal. |   |   |                          |   |   |   |                       |
|   |                | MPU type  | RWR                      | Description   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
|   |                | 6800-series   | RW                       | Read / Write control input pin<br>RW = "H" : read<br>RW = "L" : write |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 8080-series   | /WR            | Write enable clock input pin<br>The data on DB0 to DB7 are latched at the rising edge of the /WR signal.  |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| This pin is not used in serial interfaces and should be connected to VDD. |                |   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 3   | D0             |   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 4   | D1             | When using 8-bit parallel interface: 8080 or 6800 mode<br>8 bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 5   | D2             |   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 6   | D3             | When using serial interface : 4-line SPI or 3-line SPI mode<br>D[0:3] : fix to "H" by VDD1.   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 7   | D4             | D[4:6] : serial input/output data (SDA).  |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 8   | D5             | D[7] : serial input clock (SCL).  |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 9   | D6             | D4to D6must be connected together (SDA)   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 10  | D7             | When CSBis "H", D[7:0] are high impedance.  |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 11  | ERD            | Read / Write execution control pin  |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
|   |                | <table border="1"> <thead> <tr> <th>MPU Type</th> <th>ERD</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>6800-series</td> <td>E</td> <td>Read / Write control input pin<br/>RW = "H": When E is "H", DB0 to DB7 are in an output status.<br/>RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal.</td> </tr> <tr> <td>8080-series</td> <td>/RD</td> <td>Read enable clock input pin<br/>When /RD is "L", DB0 to DB7 are in an output status.</td> </tr> </tbody> </table> | MPU Type                 | ERD   | Description              | 6800-series        | E  | Read / Write control input pin<br>RW = "H": When E is "H", DB0 to DB7 are in an output status.<br>RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal. | 8080-series | /RD                      | Read enable clock input pin<br>When /RD is "L", DB0 to DB7 are in an output status.                      |   |   |                          |   |   |   |                       |
|   |                | MPU Type  | ERD                      | Description   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 6800-series   | E              | Read / Write control input pin<br>RW = "H": When E is "H", DB0 to DB7 are in an output status.<br>RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal.   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 8080-series   | /RD            | Read enable clock input pin<br>When /RD is "L", DB0 to DB7 are in an output status.   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
|   |                |   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 12  | RSB            | Reset input pin<br>When RST is "L", initialization is executed.   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 13  | IF0            | Parallel / Serial data input select input   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 14  | IF1            | <table border="1"> <thead> <tr> <th>IF0</th> <th>IF1</th> <th>IF2</th> <th>MPU interface type</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>L</td> <td>80 series 8-bit parallel</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>68 series 8-bit parallel</td> </tr> <tr> <td>L</td> <td>L</td> <td>L</td> <td>8-bit serial (4 line)</td> </tr> </tbody> </table>  | IF0                      | IF1   | IF2                      | MPU interface type | H  | H   | L           | 80 series 8-bit parallel | L  | H | H | 68 series 8-bit parallel | L | L | L | 8-bit serial (4 line) |
|   |                | IF0   | IF1                      | IF2   | MPU interface type       |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
|   |                | H   | H                        | L   | 80 series 8-bit parallel |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| L   | H              | H   | 68 series 8-bit parallel |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| L   | L              | L   | 8-bit serial (4 line)    |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 15  | IF2            |   |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |
| 16  | NC             | No connect  |                          |   |                          |                    |    |   |             |                          |  |   |   |                          |   |   |   |                       |

|       |         |  |
|-------|---------|--|
| 17    | NC      |  |
| 18    | CS<br>B | Chip select input pins<br>Data/instruction I/O is enabled only when CSB is "L".<br>When chip select is non-active, DB0 to DB7 may be high impedance. |
| 19    | VS<br>S | Ground   |
| 20    | VDD     | Power supply   |
| 21    | NC      | No connect   |
| 22    | NC      |  |
| 23    | NC      |  |
| 24    | CAP1N   | DC/DC Voltage Converter  |
| 25    | CAP1P   |  |
| 26    | XVO     | Negative operating voltage of COM-drivers.   |
| 27    | VO      | Positive operating voltage of COM-drivers.   |
| 28    | NC      | No connect   |
| 29    | NC      |  |
| 30    | VG      | VG is the power of SEG-drivers.  |
| 31~36 | NC      | No connect   |

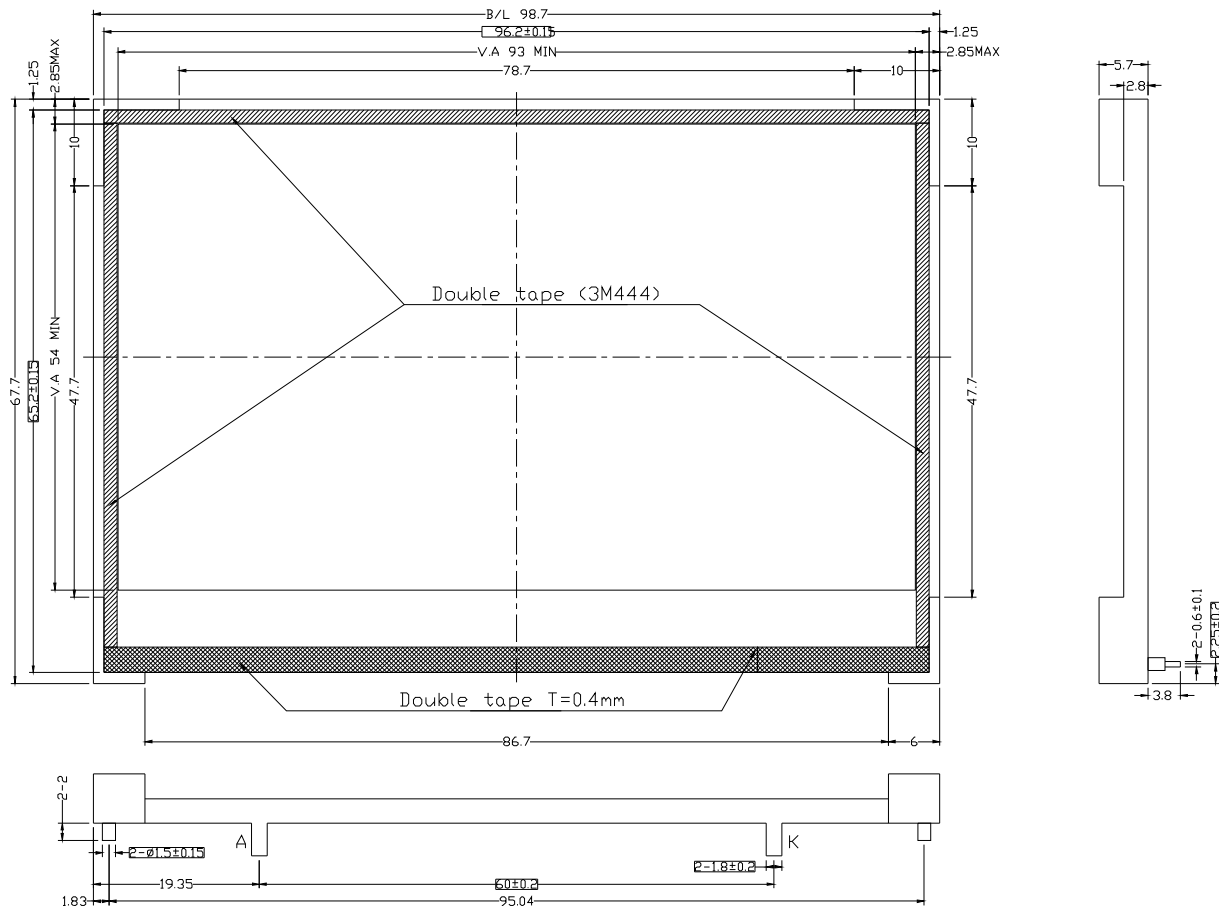
Please note: Only support 10x boosting!



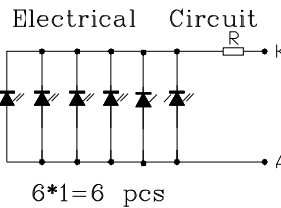
6. BACKLIGHT DRAWING

Electrical/Optical Specifications

| Item                | Symbol | Min. | Typ. | Max.  | Unit              | Condition          |
|---------------------|--------|------|------|-------|-------------------|--------------------|
| Forward Voltage     | Vf     | --   | 3.1  | --    | V                 | --                 |
| Forward Current     | If     | --   | 90   | 120   | mA                | Vf = 3.1 V         |
| Power Dissipation   | Pd     | --   | --   | 0.372 | W                 | Vf = 3.1 V         |
| Reverse Voltage     | Vr     | --   | --   | 5     | V                 | --                 |
| Reverse Current     | Ir     | --   | --   | 0.1   | mA                | Vr = 5 V Each chip |
| Luminous Intensity  | Lv     | 400  | --   | --    | cd/m <sup>2</sup> | Vf = 3.1 V         |
| Luminous Uniformity | Δ Lv   | 70   | --   | --    | %                 | Vf = 3.1 V         |
| Color Chromaticity  | X      | 0.26 | --   | 0.33  | --                | Vf = 3.1 V         |
|                     | Y      | 0.26 | --   | 0.33  | --                |                    |



Remarks:  
 1.Unmarked tolerance is ±0.3  
 2.All materials comply with RoHs  
 3. [ ]....critical dimension.  
 4.Backlight color: white  
 5.LED life time 50000H



**7. ABSOLUTE MAXIMUM RATINGS**

| Parameter                           | Symbol | Min  | Max     | Unit |
|-------------------------------------|--------|------|---------|------|
| Power Supply Voltage                | VDD    | -0.5 | +4.0    | V    |
| Power supply voltage (VDD standard) | V0-XV0 | -0.5 | +19     | V    |
| Power supply voltage (VDD standard) | VG     | -0.3 | VDD+0.3 | V    |
| Operating Temperature               | Topr   | -30  | +80     | °C   |
| Storage Temperature                 | Tstr   | -40  | +90     | °C   |

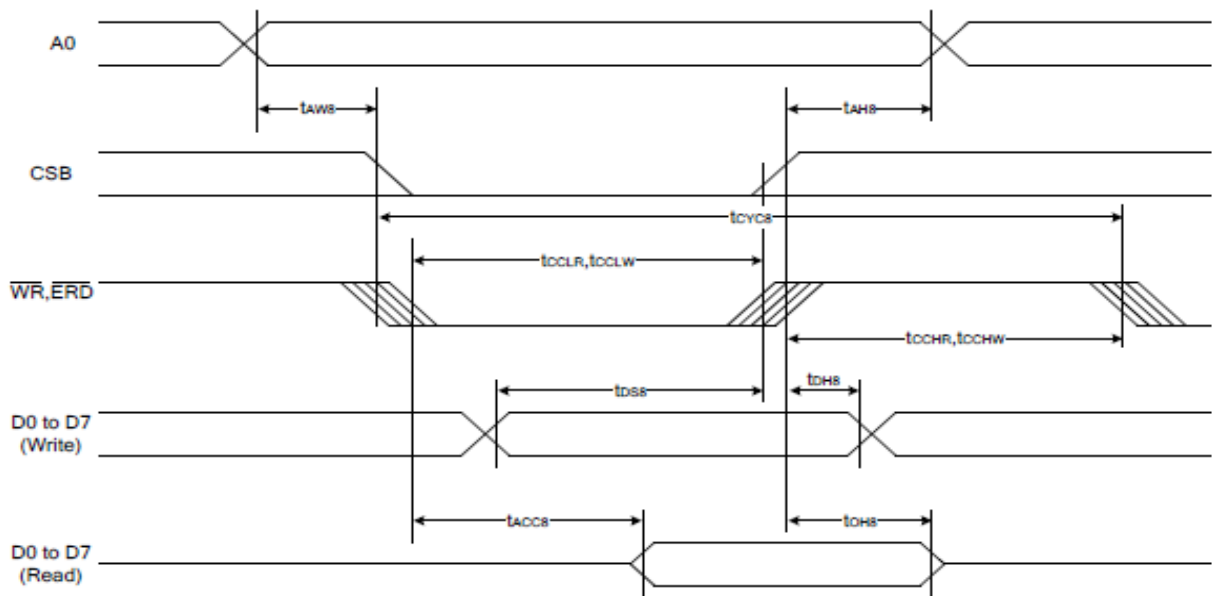
**8. DC CHARACTERISTICS**

| Item                 | Symbol | Standard Value |      |      | Test Condition | Unit |
|----------------------|--------|----------------|------|------|----------------|------|
|                      |        | Min.           | Typ. | Max. |                |      |
| Power supply Voltage | VDD    | 2.7            | 3.0  | 3.3  |                | V    |
| Operating Voltage    | Vop    | 14.2           | 14.5 | 14.8 |                |      |
| Current Consumption  | IDD    | ---            | TBD  | ---  |                | mA   |

9. AC ELECTRICAL CHARACTERISTICS

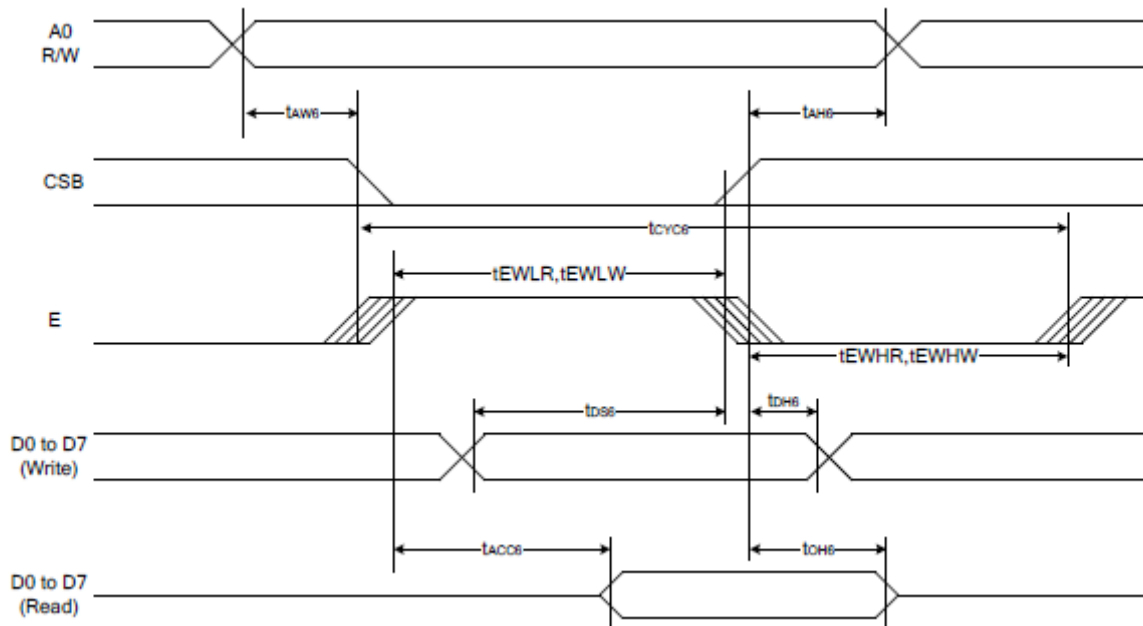
9.1 System bus READ/WRITE characteristics for the 8080 series MPU

| Item                         | Signal   | Symbol | Condition   | Rating |      | Units |
|------------------------------|----------|--------|-------------|--------|------|-------|
|                              |          |        |             | Min.   | Max. |       |
| Address hold time            | A0       | tAH8   | -           | 40     | -    | ns    |
| Address setup time           |          | tAW8   | -           | 20     | -    |       |
| System cycle time            | WR       | tCYC8  | -           | 380    | -    |       |
| Enable L pulse width (WRITE) |          | tCCLW  | -           | 80     | -    |       |
| Enable H pulse width (WRITE) |          | tCCHW  | -           | 300    | -    |       |
| Enable L pulse width (READ)  | RD       | tCCLR  | -           | 230    | -    |       |
| Enable H pulse width (READ)  |          | tCCHR  | -           | 500    | -    |       |
| WRITE Data setup time        | D0 to D7 | tDS8   | -           | 250    | -    |       |
| WRITE Address hold time      |          | tDH8   | -           | 20     | -    |       |
| READ access time             |          | tACC8  | CL = 100 pF | -      | 40   |       |
| READ Output disable time     |          | tOH8   | CL = 100 pF | -      | 30   |       |



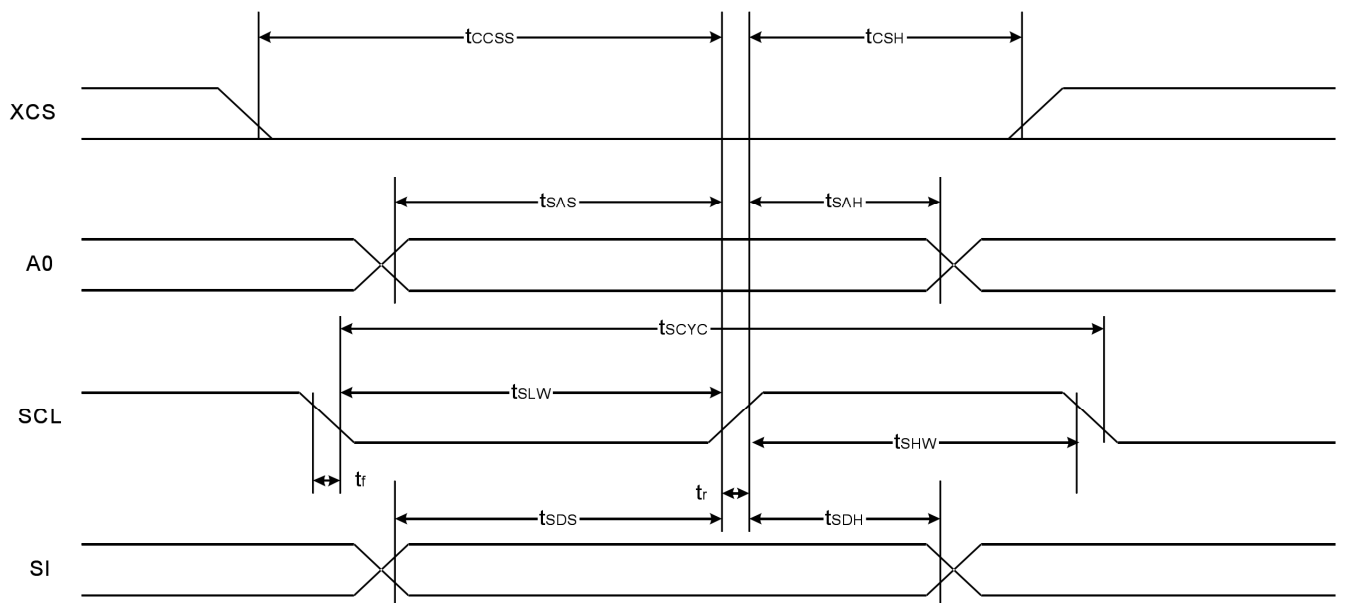
9.2 System bus READ/WRITE characteristics for the 6800 series MPU

| Item                         | Signal   | Symbol | Condition   | Rating |      | Units |
|------------------------------|----------|--------|-------------|--------|------|-------|
|                              |          |        |             | Min.   | Max. |       |
| Address hold time            | A0       | tAH6   | -           | 20     | -    | ns    |
| Address setup time           |          | tAW6   | -           | 20     | -    |       |
| System cycle time            | E        | tCYC6  | -           | 470    | -    |       |
| Enable L pulse width (WRITE) |          | tEWLW  | -           | 330    | -    |       |
| Enable H pulse width (WRITE) |          | tEWHW  | -           | 140    | -    |       |
| Enable L pulse width (READ)  | E        | tEWLR  | -           | 500    | -    |       |
| Enable H pulse width (READ)  |          | tEWHR  | -           | 230    | -    |       |
| WRITE Data setup time        | D0 to D7 | tDS6   | -           | 240    | -    |       |
| WRITE Address hold time      |          | tDH6   | -           | 230    | -    |       |
| READ access time             |          | tACC6  | CL = 100 pF | -      | 40   |       |
| READ Output disable time     |          | tOH6   | CL = 100 pF | -      | 30   |       |



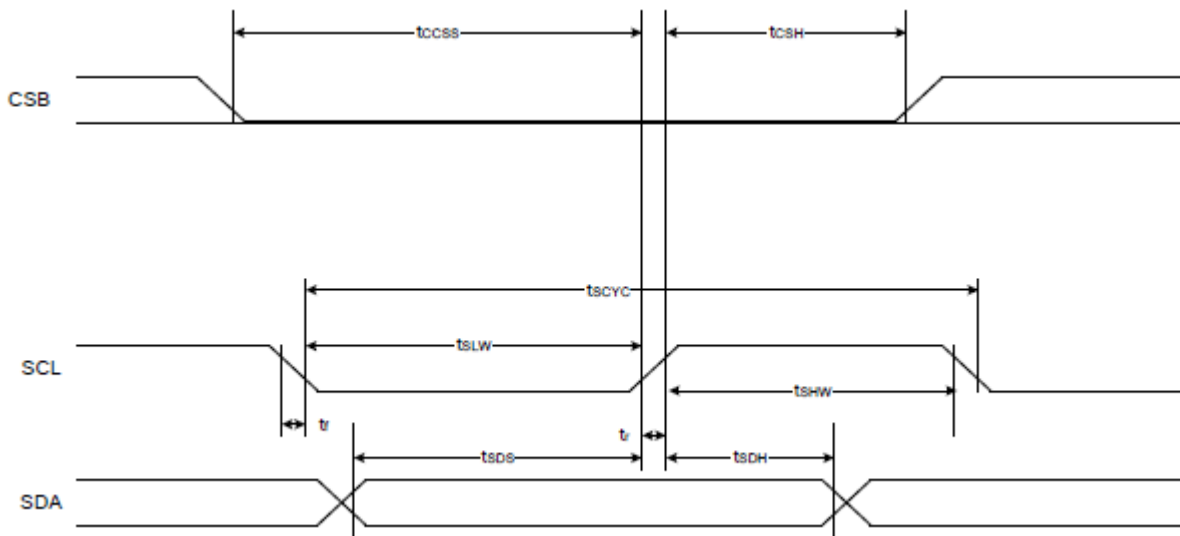
9.3 The Serial Interface (4-Line interface)

| Item                | Signal | Symbol | Condition | Rating |      | Units |
|---------------------|--------|--------|-----------|--------|------|-------|
|                     |        |        |           | Min.   | Max. |       |
| Serial Clock Period | SCL    | tSCYC  | -         | 130    | -    | ns    |
| SCL "H" pulse width |        | tSHW   | -         | 80     | -    |       |
| SCL "L" pulse width |        | tSLW   | -         | 50     | -    |       |
| Address setup time  | A0     | tSAS   | -         | 40     | -    |       |
| Address hold time   |        | tSAH   | -         | 30     | -    |       |
| Data setup time     | SDA    | tSDS   | -         | 40     | -    |       |
| Data hold time      |        | tSDH   | -         | 30     | -    |       |
| CS-SCL time         | CSB    | tCSS   | -         | 20     | -    |       |
| CS-SCL time         |        | tCSH   | -         | 60     | -    |       |



9.4 The Serial Interface (3-Line interface)

| Item                | Signal | Symbol | Condition | Rating |      | Units |
|---------------------|--------|--------|-----------|--------|------|-------|
|                     |        |        |           | Min.   | Max. |       |
| Serial Clock Period | SCL    | tSCYC  | -         | 130    | -    | ns    |
| SCL "H" pulse width |        | tSHW   | -         | 80     | -    |       |
| SCL "L" pulse width |        | tSLW   | -         | 50     | -    |       |
| Data setup time     | SI     | tSDS   | -         | 40     | -    |       |
| Data hold time      |        | tSDH   | -         | 30     | -    |       |
| CS-SCL time         | CSB    | tCSS   | -         | 20     | -    |       |
| CS-SCL time         |        | tCSH   | -         | 60     | -    |       |



## 10. COMMAND TABLE

Ext=0 or Ext=1

| Index | Command | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function  | Hex | Parameter |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|-----------|-----|-----------|
| 1     | Ext In  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | Ext=0 Set | 30  | None      |
| 2     | Ext Out | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 1  | Ext=1 Set | 31  | None      |

Ext=0

| Index | Command  | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function              | Hex | Parameter |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|-----------------------|-----|-----------|
| 1     | DISON    | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | Display On            | AF  | None      |
| 2     | DISOFF   | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 0  | Display Off           | AE  | None      |
| 3     | DISNOR   | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | Normal Display        | A6  | None      |
| 4     | DISINV   | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 1  | Inverse Display       | A7  | None      |
| 5     | COMSCN   | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | COM Scan Direction    | BB  | 1 byte    |
| 6     | DISCTRL  | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | Display Control       | CA  | 3 bytes   |
| 7     | SLPIN    | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | Sleep In              | 95  | None      |
| 8     | SLPOUT   | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | Sleep Out             | 94  | None      |
| 9     | LASET    | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | Line Address Set      | 75  | 2 bytes   |
| 10    | CASET    | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | Column Address Set    | 15  | 2 bytes   |
| 11    | DATSDR   | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 0  | Data Scan Direction   | BC  | 3 bytes   |
| 12    | RAMWR    | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 0  | Writing to Memory     | 5C  | Data      |
| 13    | RAMRD    | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | Reading from Memory   | 5D  | Data      |
| 14    | PTLIN    | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | Partial display in    | A8  | 2 bytes   |
| 15    | PTLOUT   | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | Partial display out   | A9  | None      |
| 16    | RMWIN    | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | Read and Modify Write | E0  | None      |
| 17    | RMWOUT   | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | RMW end               | EE  | None      |
| 18    | ASCSET   | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | Area Scroll Set       | AA  | 4 bytes   |
| 19    | SCSTART  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | Scroll Start Set      | AB  | 1 byte    |
| 20    | OSCON    | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | Internal OSC on       | D1  | None      |
| 21    | OSCOFF   | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | Internal OSC off      | D2  | None      |
| 22    | PWRCTRL  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | Power Control         | 20  | 1 byte    |
| 23    | VOLCTRL  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | EC control            | 81  | 2 bytes   |
| 24    | VOLUP    | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | EC increase 1         | D6  | None      |
| 25    | VOLDOWN  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 1  | 1  | EC decrease 1         | D7  | None      |
| 26    | RESERVED | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | Not Use               | 82  | 0         |
| 27    | EPSRRD1  | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | READ Register1        | 7C  | None      |

|    |         |   |   |   |           |   |   |   |   |   |   |             |                 |    |        |
|----|---------|---|---|---|-----------|---|---|---|---|---|---|-------------|-----------------|----|--------|
| 28 | EPSRRD2 | 0 | 1 | 0 | 0         | 1 | 1 | 1 | 1 | 1 | 0 | 1           | READ Register2  | 7D | None   |
| 29 | NOP     | 0 | 1 | 0 | 0         | 0 | 1 | 0 | 0 | 1 | 0 | 1           | NOP Instruction | 25 | None   |
| 30 | STREAD  | 0 | 0 | 1 | Read Data |   |   |   |   |   |   | Status Read |                 |    |        |
| 31 | EPINT   | 0 | 1 | 0 | 0         | 0 | 0 | 0 | 0 | 1 | 1 | 1           | Initial code(1) | 07 | 1 byte |

Ext=1

| Index | Command    | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function              | Hex | Parameter |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|-----------------------|-----|-----------|
| 1     | Gray 1 Set | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | FRAME 1 Gray PWM Set  | 20  | 16 bytes  |
| 2     | Gray 2 Set | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | FRAME 2 Gray PWM Set  | 21  | 16 bytes  |
| 3     | Wt. Set    | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | Weight Set            | 22  | 3 bytes   |
| 4     | ANASET     | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | Analog Circuit Set    | 32  | 3 bytes   |
| 5     | DITHOFF    | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | Dithering Circuit Off | 34  | None      |
| 6     | DITHON     | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | Dithering Circuit On  | 35  | None      |
| 7     | EPCTIN     | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 1  | Control EEPROM        | CD  | 1 byte    |
| 8     | EPCOUT     | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | Cancel EEPROM         | CC  | None      |
| 9     | EPMWR      | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | Write to EEPROM       | FC  | None      |
| 10    | EPMRD      | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | Read from EEPROM      | FD  | None      |



**11. ACCEPT QUALITY LEVEL (AQL)**

11.1 Inspection Plan: ANSI Z-1.4, Normal Inspection Level II, Single Sampling Plan.

**12. RELIABILITY TEST**

Operating life time: 50000 hours (at room temperature without direct irradiation of sunlight)

Reliability characteristics shall meet following requirements.

| <b>Test Item</b>                | <b>Test Condition</b>                                  |
|---------------------------------|--|
| High temperature storage        | +90°C x 96hrs  |
| Low temperature storage         | -40°C x 96hrs  |
| High temperature operation      | +80°C x 96hrs  |
| Low temperature operation       | -30°C x 96hrs  |
| High temperature, High humidity | +60°C x 95%RH x 96hrs                                  |
| Thermal shock                   | -30°C x 30min → +25°C x 10s → +80°C x 30min<br>5Cycles |
| Vibration test                  | Frequency x Swing x Time<br>40Hz x 4mm x 4hrs          |
| Drop test                       | Drop height x No. of drops<br>1.0m x 6drops            |

13. QUALITY DESCRIPTION

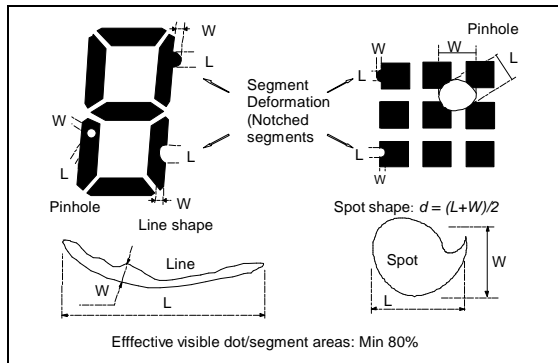
**DEFECT SPECIFICATION:**

a: Table for Cosmetic defects

(Note: nc = not counted).

Sizes and number of defects

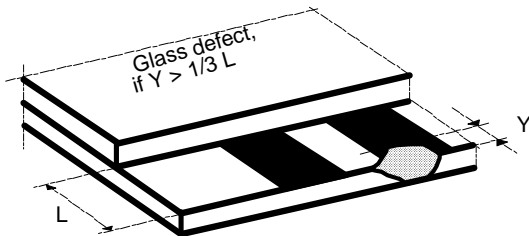
(Max. Qty)



Examples/ Shapes

b: Glass defects

b1: Glass defects at contact ledge



b2: Glass chipping in other areas shall not be in conflict with the product's function.

| Defect Type              | Max. defect size [mm] |        | Max. Quantity.  |
|--------------------------|-----------------------|--------|-----------------|
|                          | d or L                | W      |                 |
| Black or White Spots     | d ≤ 100               |        | nc              |
|                          | 100 < d ≤ 200         |        | 3               |
| Black or White Lines     | --                    | W ≤ 10 | nc              |
|                          | L ≤ 3000              | W ≤ 30 | 2               |
|                          | L ≤ 2000              | W ≤ 50 | 2               |
| Pinhole                  | d ≤ 100               |        | nc<br>1/segment |
|                          | 100 < d ≤ 200         |        |                 |
| (Total defects)          |                       |        | (5)             |
| Segment Deformation      | W ≤ 100               |        | nc              |
| Bubble (e.g. under pola) | d ≤ 150               |        | nc              |
|                          | 200 < d ≤ 400         |        | 2               |

**14. LCD MODULES HANDLING PRECAUTIONS**

- n** The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- n** If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- n** Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- n** The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- n** To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD module.

- Tools required for assembly, such as soldering irons, must be properly grounded.

- To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- n** Storage precautions

- When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

**15. OTHERS**

- n** Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- n** If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- n** To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections