Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 080160A VMH-PW-N

(C-TOUCH)

0,96“ TFT

Product Specification Ver.: 2

26.07.2022

Revision History

VERSION	DATE	REVISED PAGE NO.	Note
0 1	25.09.2020 15.07.2021		First Issue Correct Initial Code for Reference
2	26.07.2022		Modify Contour Drawing

Contents

1. Summary

DEM 080160A VMH-PW-N(C-TOUCH) is a color active matrix thin film transistor (TFT) liquid crystal empty cell. This model is composed of amorphous silicon TFT as a switching device. It is a transmissive type display operating in the normally black mode.

This TFT LCD has a 0.96-inch diagonally measured active display area with 80 x 160 dot (80 horizontal by 160 vertical pixel) resolution. Each pixel is divided into Red, Green, Blue dots which are arranged in vertical stripes.

2. General Specifications

n	Size:	0.96 Inch
n	Dot Matrix:	80 x RGB x 160(TFT) dots
n	Module Dimension:	18.70 x 31.90 x 2.64 mm
n	Active Area:	10.80 x 21.696 mm
n	Dot Pitch:	0.135 x 0.1356 mm
n	LCD Type:	TFT, Normally Black, Transmissive
n	Viewing Angle:	80/80/80/80
n	Aspect Ratio:	1:2
n	IC:	ST7735S or equivalent
n	TFT Interface:	SPI Interface
n	Backlight Type:	LED, Normally White
n	CTP Interface:	I2C
n	CTP IC:	FT3267 or equivalent
n	CTP FW Version:	V06
n	With /Without TP:	With CTP
n	Surface:	Glare

*Color tone slight changed by temperature and driving voltage.

3. Interface

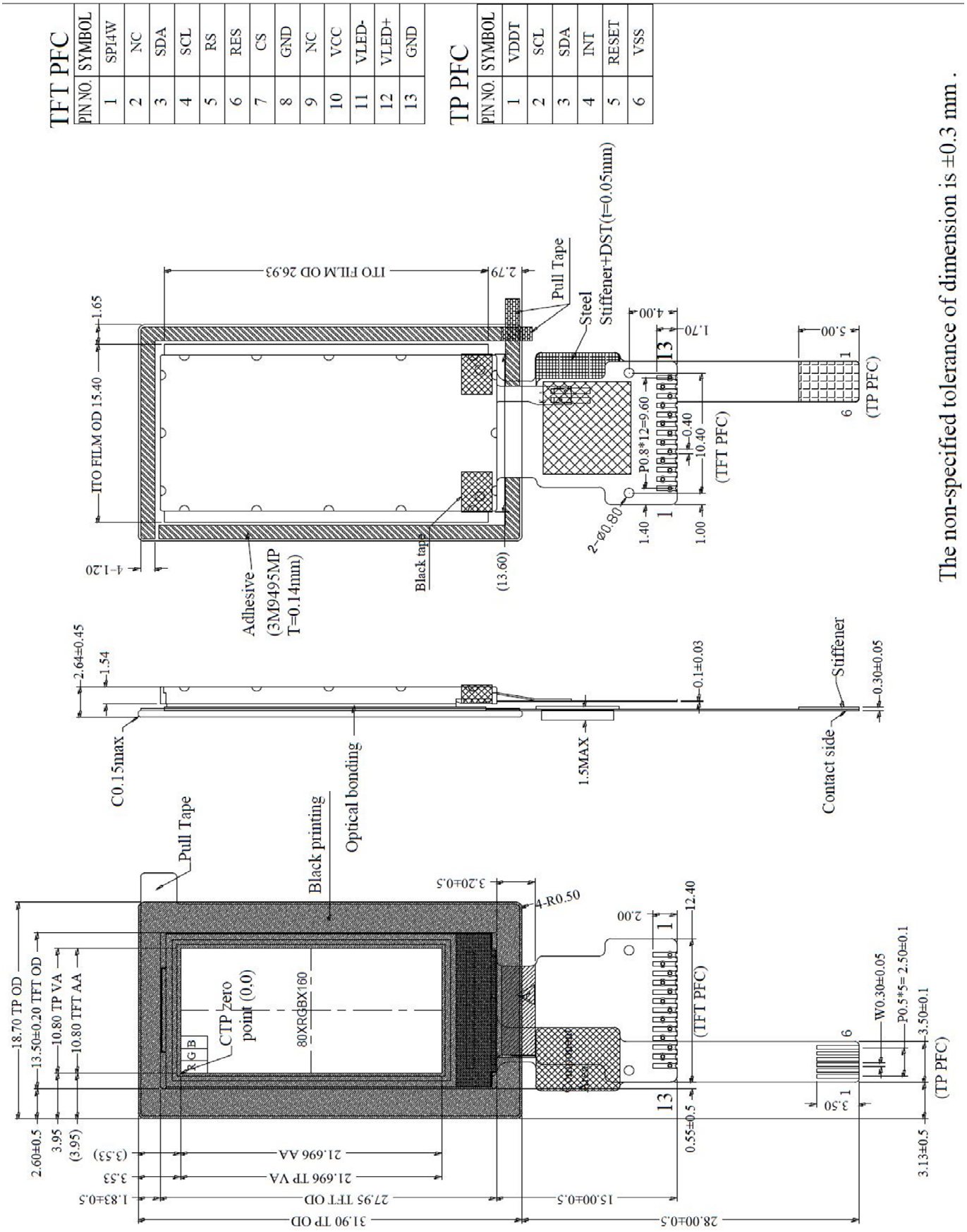
3.1. LCM PIN Definition

Pin	Symbol	Function	Remark
1	SPI4W	SPI4W='0', 3-wire SPI. SPI4W='1', 4-wire SPI.	
2	NC	No connection	
3	SDA	Serial interface data	
4	SCL	Serial interface clock	
5	RS	Data/command selection pin (4-wire SPI use)	
6	RES	Reset pin (low active)	
7	CS	Chip selection pin (low active)	
8	GND	Ground	
9	NC	No connection	
10	VCC	Power supply.	
11	VLED-	Back light cathode	
12	VLED+	Back light anode	
13	GND	Ground	

3.2. CTP PIN Definition

Pin	Symbol	Function	Remark
1	VDDT	Power supply	
2	SCL	IIC clock signal. Must be pulled high	
3	SDA	IIC data signal. Must be pulled high.	
4	INT	External interrupt to the host	
5	RESET	External Reset. Low is active	
6	VSS	Power ground.	

4. Contour Drawing



5. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	-	+70	°C
Storage Temperature	TST	-30	-	+80	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≤60°C, 90% RH MAX. Temp. > 60°C, Absolute humidity shall be less than 90% RH at 60°C

6. Electrical Characteristics

6.1. Operating conditions:

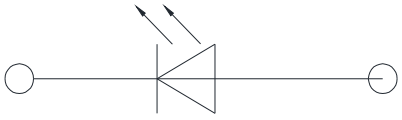
Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	3.0	3.3	3.6	V
Supply LCM current	ICC	-	2	3	mA
Supply CTP	VDDT	2.8	-	3.3	V
	I_{VDDT}	-	2	3	mA

Note:To avoid power supply noise, please avoid using driving conditions close to min. or max. value

6.2. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	ILED	-	20	-	mA	
LED Voltage	VLED	2.8	3.0	3.3	V	Note 1
LED Lifetime		-	50000	-	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



VLED- VLED+

Circuit diagram

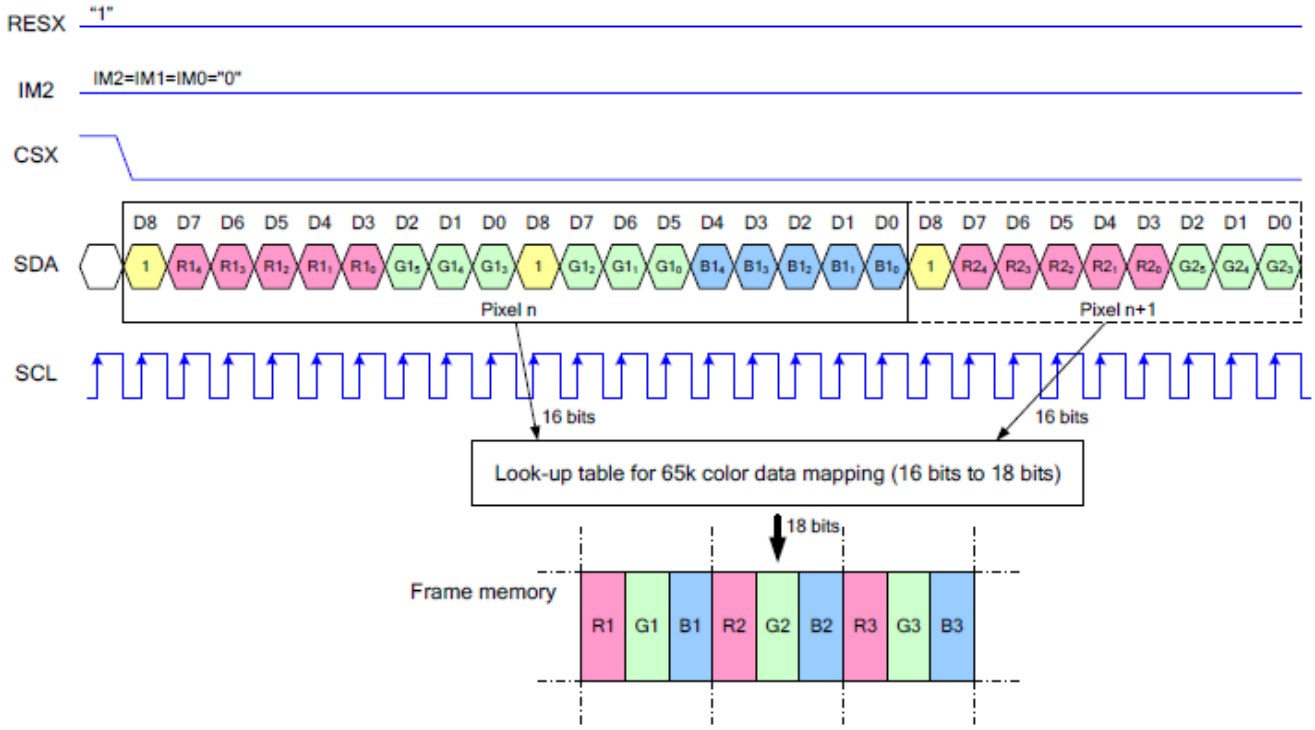
Note 2 : Ta = 25°C

Note 3 : Brightness to be decreased to 50% of the initial value

Note 4 : The single LED lamp case

7. Data Color Coding

7.1. 3-Wire SPI Mode: RGB 5-6-5-bit Input, 65K-Colors, 3AH="05h"

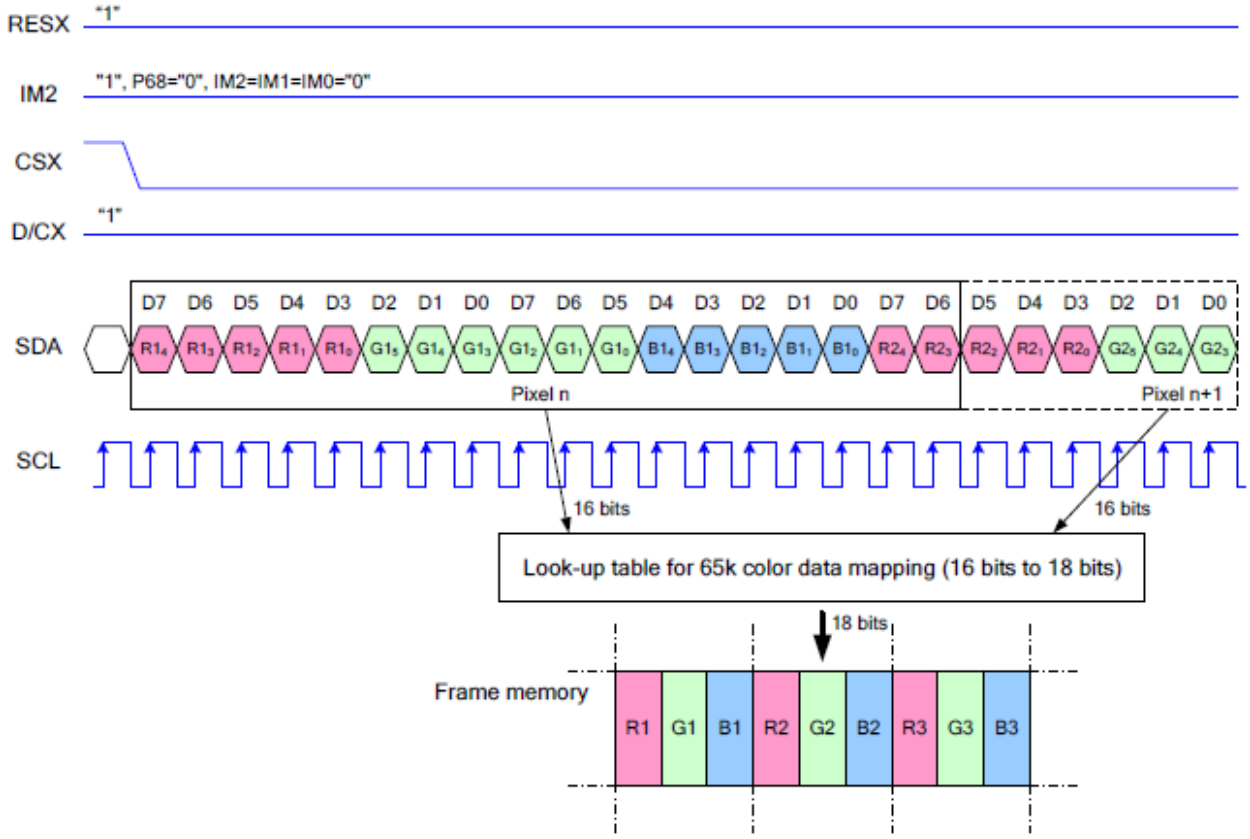


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.2. 4-Wire SPI Mode: RGB 5-6-5-bit Input, 65K-Colors, 3AH="05h"

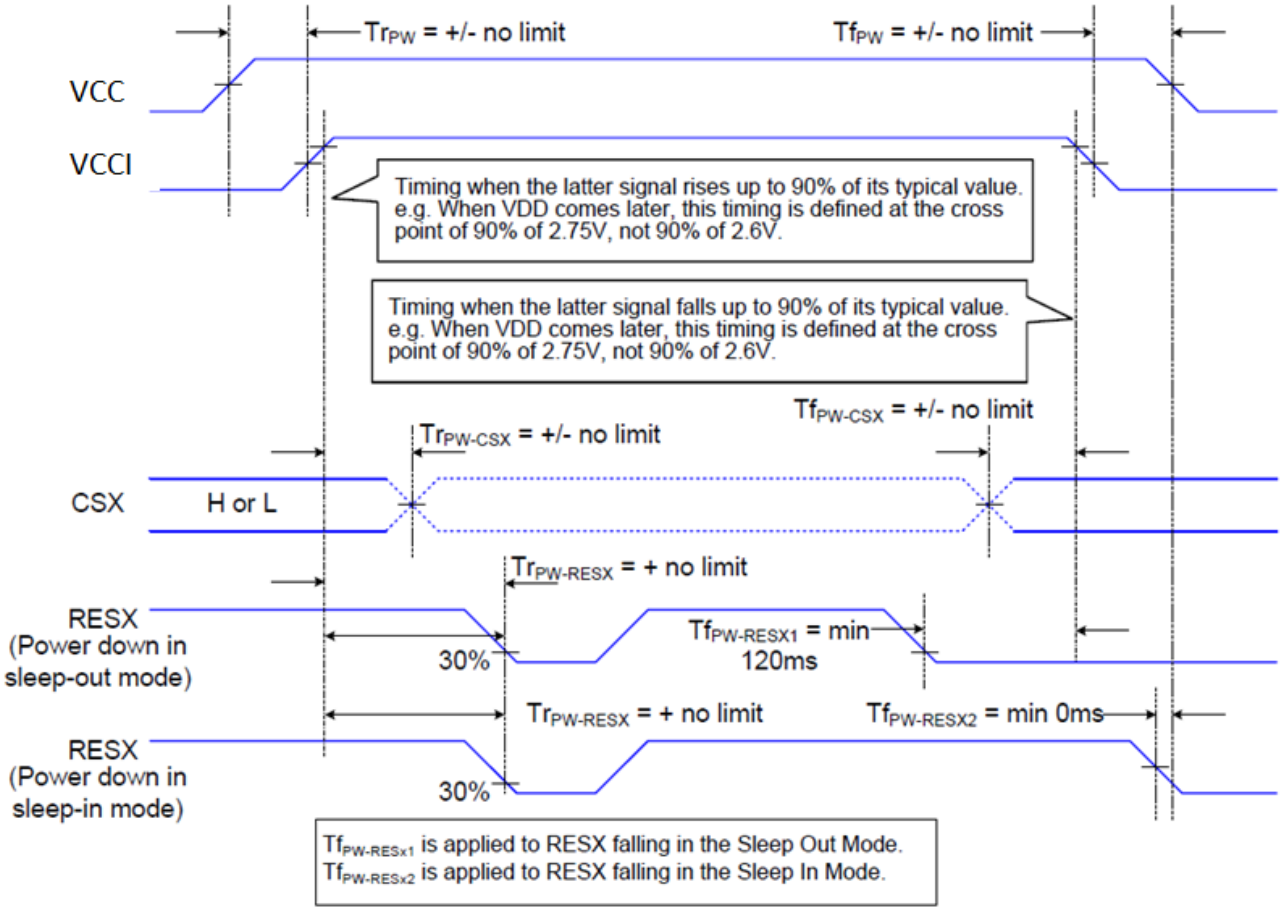


Note 1. Pixel data with the 16-bit color depth information

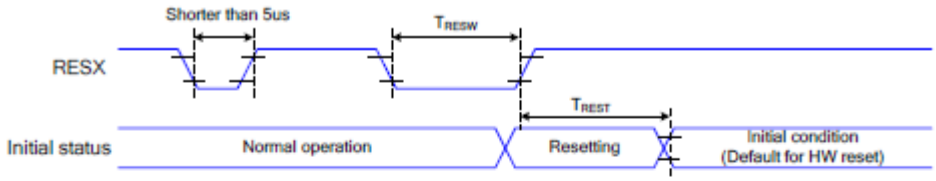
Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8. Power ON/OFF Sequence



9. Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	tRESW	Reset Pulse Duration	10	-	us
	tREST	Reset Cancel	-	5	ms
				120	ms

Table 14 Reset Timing

Notes:

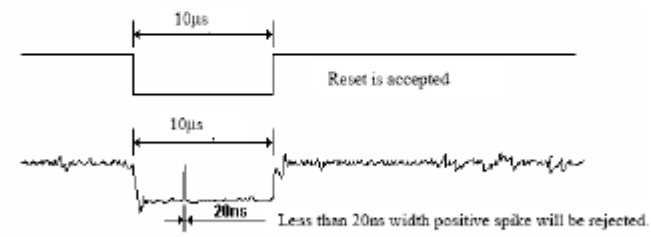
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

10. Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response Time		Tr	θ=0°、Φ=0°	-	30	40	.ms	Note 3
		Tf						
Contrast Ratio		CR	At optimized viewing angle	-	800	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.255	0.305	0.355		Note 2,6,7
		Wy		0.275	0.325	0.375		
Viewing Angle	Hor.	ΘR	CR≧10	-	80	-	Deg.	Note 1
		ΘL		-	80	-		
	Ver.	ΦT		-	80	-		
		ΦB		-	80	-		
Brightness		-	-	300	400	-	cd/m^2	Center of display
Uniformity		(U)	-	75	-	-	%	Note 5

Ta=25±2℃

Note 1: Definition of viewing angle range

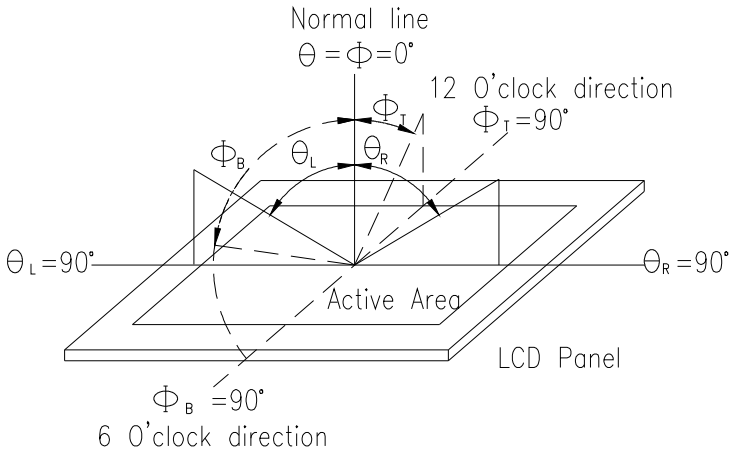


Fig.11.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

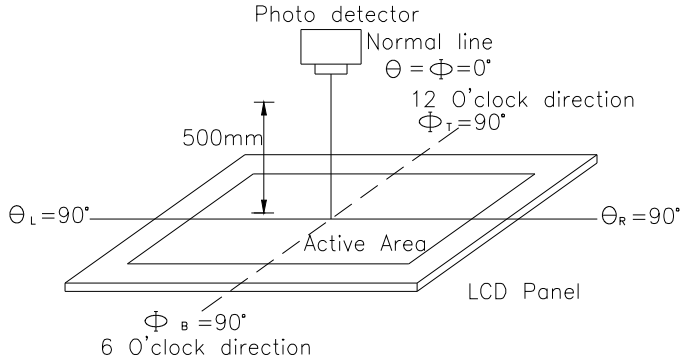
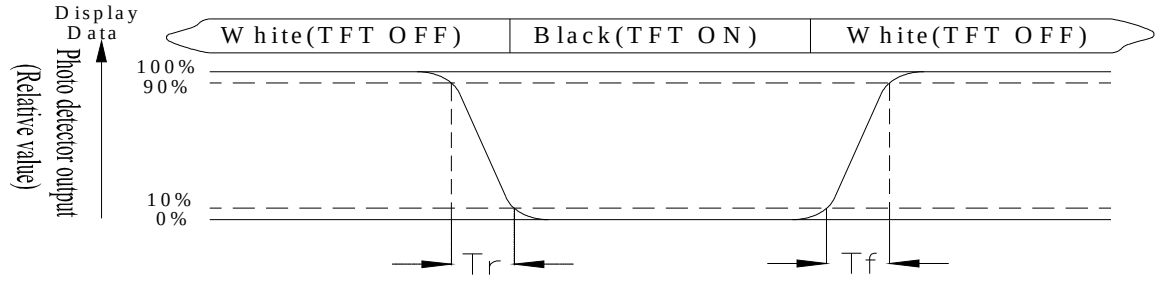


Fig. 11.2. Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity

Active area is divided into 3 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/Lmax x100%

L = Active area length

W = Active area width

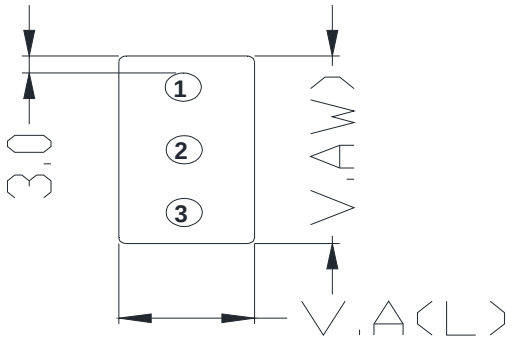


Fig11.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)

Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

11. Reliability

Content of Reliability Test (Wide temperature, -20°C~70°C)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature Storage	Endurance test applying the low storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60□,90%RH max	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation -20°C 25°C 70°C 30min 5min 30min 1 cycle	-20°C /70°C 10 cycles	——
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static Electricity Test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact) ,±800v(air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

12. Inspection Specification

1. Scope：TFT-LCD (The document shall be applied to TFT-LCD Module)

2. Inspection Standard ： MIL-STD-105EII(MIL-STD-105E Table Normal Inspection Single Sampling Level II)

3. Defect Level： AQL：0.65; AQL：2.5(Major Defect AQL:0.65;Minor Defect AQL:2.5)

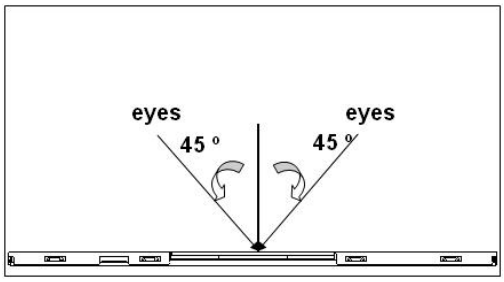
4. Test conditions:

(1) Temperature：15℃~25℃；(Humidity)：55 ±15%

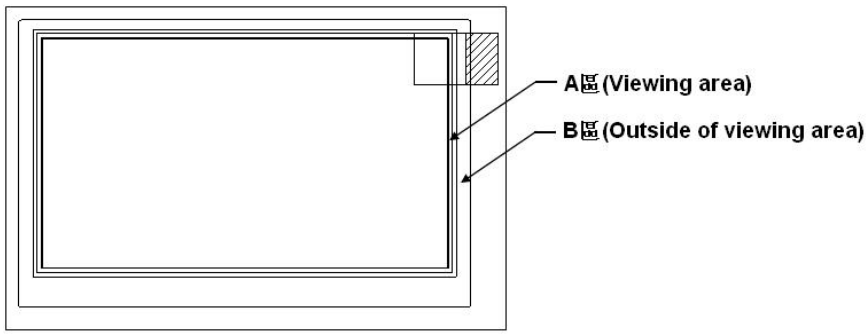
(2) Visual inspection：500 Lux：20cm~30cm (Illumination：More than 500 Lux; Inspection Distance: 20cm~30cm)

(3) Electrical inspection ： 100Lux~300Lux ； 20cm~30cm(Illumination ： 100Lux~300Lux; Inspection Distance: 20cm~30cm)

(4) Visual angle：45 º(The test direction is base on about around 45º of Vertical line）



(5) Definition of area:



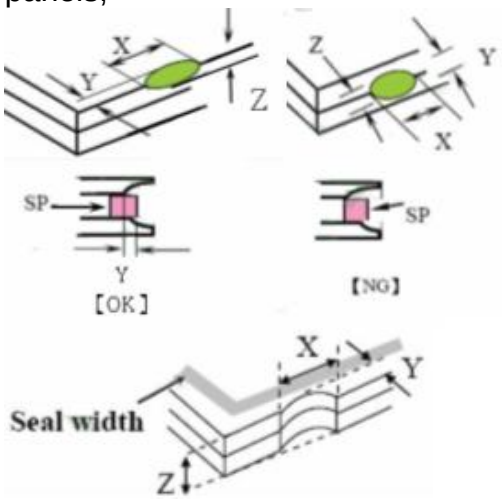
5. Pixel Definition:

R	G	B	R	G	B	R	G	B		Dot Defect
R	G	B	R	G	B	R	G	B		Adjacent Dot Defect
R	G	B	R	G	B	R	G	B		Cluster

Note 1:If pixel or partial sub-pixel defects exceed 50% of the affected pixel or sub-pixel area, it shall be considered as1 defect.

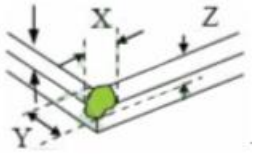
Note 2: There should be no distinct non-uniformity visible through 6% ND Filter within 2 sec inspection times.

5. Inspection Standard :

<table>
<tr><th>No</th><th>Inspection Item</th><th>Inspection Standard</th><th>Defect Level</th></tr>
<tr><td>1</td><td>Packing & Indicate</td><td>1.1. Mixed product types.
1.2. The part number is inconsistent with work order of production.
1.3. Assembled in inverse direction.
1.4. The quantity is inconsistent with work order of production.</td><td>Maj</td></tr>
<tr><td>2</td><td>Size</td><td>Product size and structure must meet the structure diagram</td><td>Maj</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">The crack of Glass</td><td>Symbols:
X:Symbols
Y:The width of crack.
Z:The thickness of crack.
W:Terminal length
T:The thickness of glass.
a:LCD LCD side length.</td><td rowspan="3">Min</td></tr>
<tr><td>3.1.一 General glass chip:
3.1.1.Chip on panel surface and crack between panels;
 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤a</td><td>VA Crack can't enter viewing area</td><td>≤1/2t</td></tr>
<tr><td>≤a</td><td>SP 一 Crack can't exceed the half of SP width</td><td>1/2t < Z≤2t</td></tr>
</table></td></tr>
<tr><td></td></tr>
</table>

3.1.2.邊角破損(Corner crack)：

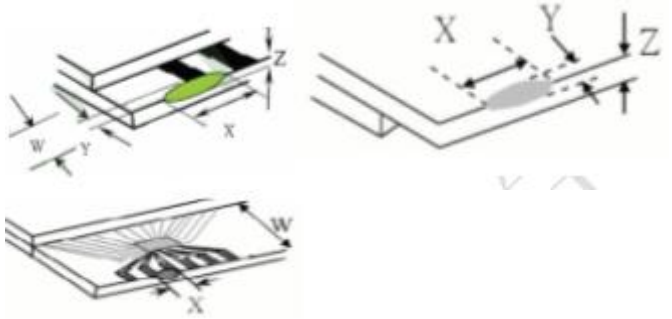


No	Inspection Item	Inspection Standard	Defect Level
3	The crack of Glass		Min

X	Y	Z
≤1/5a	Crack can't enter viewing area	≤1/2t
≤1/5a	SP 一 Crack can't exceed the half of SP width	1/2t < Z≤2t

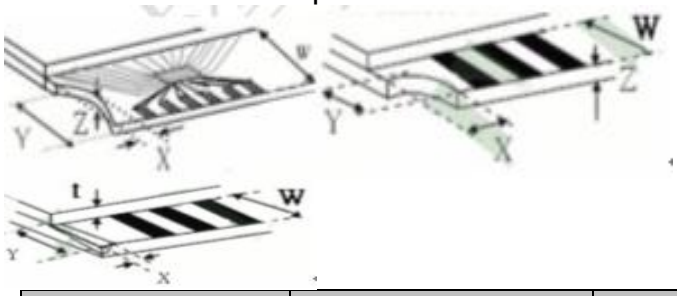
3.2.Protrusion over terminal:

3.2.1.Chip on electrode pad:



Position	X	Y	Z
Front	≤a	≤1/2W	≤t
Back	≤a	≤W	≤1/2t

3.2.2.Non-conductive portion:

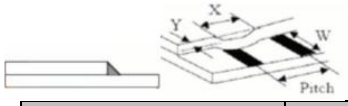


X	Y	Z
≤1/3a	≤W	≤t

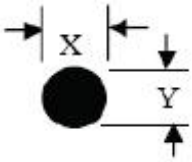
Note：

ITO ITO 1/3，If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.

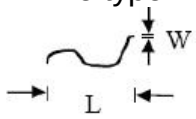
3.2.3.Glass remain:

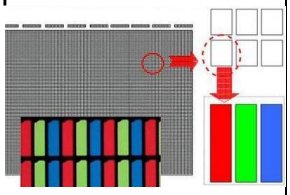


X	Y	Z
≤a	≤1/3W	≤t

No	Inspection item	Inspection Standard	Defect Level
4	Black or white dot Round type 	4.1 Round type(Non-display or display): distance >=5mm	Min

Size	Judging standard	Acceptance(Q'ty)
0.96”	D ≤0.1 mm	Ignore
	0.10mm < D ≤ 0.4mm	N≦3
	D > 0.4mm	N≦0

<table>
<tr><td>5</td><td>scratch、
contamination
Line type
  </td><td>5.1 Line type(Non-display or display):
<table>
<tr><th>Size</th><th colspan="2">Judging standard</th><th>Acceptance(Q'ty)</th></tr>
<tr><td rowspan="4">0.96”</td><td>W</td><td>L</td><td rowspan="2"></td></tr>
<tr><td>W≦ 0.03mm</td><td>—</td><td>Ignore</td></tr>
<tr><td>0.03mm < W≦0.05mm</td><td>L ≦ 5mm</td><td>N≦4</td></tr>
<tr><td>W > 0.05mm</td><td>L > 5mm</td><td>N≦0</td></tr>
</table>
distance >=5mm</td><td>Min</td></tr>
<tr><td>6</td><td>POL Polarizer Bubble</td><td>
<table>
<tr><th>area</th><th>Judging standard</th><th>Acceptance(Q'ty)</th></tr>
<tr><td rowspan="4">A 區
(Viewing area)</td><td>D < 0.2 mm</td><td>Ignore</td></tr>
<tr><td>0.2mm < D≦0.3mm</td><td>N≦3</td></tr>
<tr><td>0.3mm < D≦0.5mm</td><td>N≦1</td></tr>
<tr><td>0.5mm < D</td><td>N≦0</td></tr>
<tr><td>B (Outside of viewing area)</td><td>_</td><td>Ignore</td></tr>
</table>
</td><td>Min</td></tr>
<tr><th>No</th><th>Inspection item</th><th>Inspection Standard</th><th>Defect Level</th></tr>
<tr><td>7</td><td>POL The folding and peeled offin polarizer</td><td>The folding and peeled offin polarizer are not acceptable.</td><td>Min</td></tr>
<tr><td>8</td><td>Brightness and uniformity、Chroma</td><td>Shall be in accordance with the drawings and specification requirements specifications.</td><td>Maj</td></tr>
<tr><td>9</td><td>MURA</td><td>(5% ND Filter) 50%</td><td></td></tr>
<tr><td>10</td><td>Electrical Testing</td><td>1. Missing line character and icon.
2. No function or no display.
3. Display malfunction.
4.LCD (LCD viewing angle defect.
5. Current consumption exceeds product specifications.</td><td>Maj</td></tr>
</table>

11	Bright dot、Dark dot On-display Pixel： 3 dot in 1 pixel 	<table><tr><th>Size</th><th>Item</th><th>Judging standard</th><th>Acceptance(Q'ty)</th></tr><tr><td rowspan="5">0.96”</td><td rowspan="2">Bright dot</td><td>D≦1/2 Dot</td><td>Ignore</td></tr><tr><td>1/2 Dot < D≦1 Dot</td><td>N≦1</td></tr><tr><td rowspan="2">Dark dot</td><td>D≦1/2 Dot</td><td>Ignore</td></tr><tr><td>1/2 Dot < D≦1 Dot</td><td>N≦2</td></tr><tr><td colspan="2">Total</td><td>N≦2</td></tr></table> Dark and bright dot is defined more than 50% area of one dot.	Min

13. Initial Code for Reference

```
GATE = 160;
SOURCE = 80;

//RESET
SPI_RST = 1;                                    //RA0
delay1(10);
SPI_RST = 0;
delay1(1000);
SPI_RST = 1;
delay1(10);

//20180302 Brian add
//Sleep out
SPI_0096A_WrCmd(0x11);                          //Sleep out
delay(120);

//ST7735S Frame Rate Setting in normal mode: fosc/(((RTNA*2)+40)*(LINE+FPA+BPA+2))=80
 SPI_0096A_WrCmd(0XB1);                         // fosc=850KHz
SPI_0096A_WriteData(0X05);                      // RTNA=5
SPI_0096A_WriteData(0X3C);  //20180612         // FPA=58
SPI_0096A_WriteData(0X3C);  //20180612         // BPA=58

//ST7735S Frame Rate Setting in idle mode: fosc/(((RTNB*2)+40)*(LINE+FPB+BPB+2))=80
 SPI_0096A_WrCmd(0XB2);                         // fosc=850KHz
SPI_0096A_WriteData(0X05);                      // RTNB=5
SPI_0096A_WriteData(0X3C);  //20180612         // FPB=58
SPI_0096A_WriteData(0X3C);  //20180612         // BPB=58

//ST7735S Frame Rate Setting in parital mode (dot inverson): fosc/(((RTNC*2)+40)*(LINE+FPC+BPC+2))=80
//ST7735S Frame Rate Setting in parital mode (column inverson): fosc/(((RTNC*2)+40)*(LINE+FPC+BPC+2))=80
SPI_0096A_WrCmd(0XB3);                          // fosc=850KHz
SPI_0096A_WriteData(0X05);                      // RTNC=5
SPI_0096A_WriteData(0X3C);  //20180612         // FPC=58
SPI_0096A_WriteData(0X3C);  //20180612         // BPC=58
SPI_0096A_WriteData(0X05);                      // RTND=5
SPI_0096A_WriteData(0X3C);  //20180612         // FPD=58
SPI_0096A_WriteData(0X3C);  //20180612         // BPD=58

//ST7735S Display Inversion Control
SPI_0096A_WrCmd(0XB4);                          // Dot inversion: 20184019 modify from Sitronix initial code
SPI_0096A_WriteData(0X07);                      // 0xB4[2]=Inversion setting in normal mode
                                                // 0xB4[1]=Inversion setting in idle mode
                                                // 0xB4[0]=Inversion setting in partial mode
```

```
57.
58.
59. //ST7735S Power on Sequence
60. SPI_0096A_WrCmd(0XC0);                                   // power control 1
61. SPI_0096A_WriteData(0XE9);     //20180612                //
    {Par.3[0],Par.1[4:0]}=VRHP[5:0]=2→GVDD=4.6, Par.1[7:5]=AVDD [2:0]=6→AVDD=5.1
62. SPI_0096A_WriteData(0X09);      //20180612                //
    {Par.3[1],Par.2[4:0]}=VRHN[5:0]=2→GVCL=-4.6
63. SPI_0096A_WriteData(0X04);                              // Par.3[7:6]=MODE[1:0]=2X
64.
65. SPI_0096A_WrCmd(0XC1);                                  // power control 2
66. SPI_0096A_WriteData(0XC5);     //20180612                // Par.1
    [1:0]=VGHBT[1:0]=0→VGH=2*AVDD+VGH25-0.5
67.                                                         // Par.1
    [3:2]=VGLSEL[1:0]=0→VGL=-7.5
68.                                                         // Par.1
    [7:6]=VGLSEL[1:0]=3→VGH25=2.4
69.
70. SPI_0096A_WrCmd(0XC2);                                  // power control 3
71. SPI_0096A_WriteData(0X0D);    //20180612                // (Sitronix initial)
    {Par.1 [7:6],Par.2[7:0]=DCA[9:0]=000000000'b→Booster set up cycle BCLK/1 BCLK/3
    BCLK/1 BCLK/1 BCLK/1 in normal mode
72. SPI_0096A_WriteData(0X00);                              //
    Par.1[5:3]=SAPA[2:0]=001'b→ OP current is small in normal mode
73.                                                         //
    Par.1[2:0]=APA[2:0]=001'b→ OP current is Large in normal mode
74.
75. SPI_0096A_WrCmd(0XC3);                                  // power control 4
76. SPI_0096A_WriteData(0X8D); //20180612                   // (Sitronix
    initial){Par.1 [7:6],Par.2[7:0]=DCB[9:0]=1001101010'b→Booster set up cycle BCLK/2
    BCLK/1 BCLK/2 BCLK/2 BCLK/2 in idle mode
77. SPI_0096A_WriteData(0X6A);                              //
    Par.1[5:3]=SAPB[2:0]=001'b→ OP current is small in idle mode
78.                                                         //
    Par.1[2:0]=APB[2:0]=011'b→ OP current is Medium in idle mode
79.
80. SPI_0096A_WrCmd(0XC4);                                  // power control 5
81. SPI_0096A_WriteData(0X8D); //20180612                   // (Sitronix
    initial){Par.1 [7:6],Par.2[7:0]=DCC[9:0]=1011101110'b→Booster set up cycle BCLK/2
    BCLK/2 BCLK/2 BCLK/4 BCLK/2 in partial mode
82. SPI_0096A_WriteData(0XEE);                              //
    Par.1[5:3]=SAPC[2:0]=001'b→ OP current is small in partial mode
83.
84.
85. // ST7735S VCOM
86. SPI_0096A_WrCmd(0XC5);                                  // VCOM setting value
87. SPI_0096A_WriteData(0X15); //20180612                   //
    0XC5[5:0]=010010'b → VCOM=-0.875
88.
89.
90.
91. // ST7735 Memory data access control: add from Sitronix initial code
92. SPI_0096A_WrCmd(0X36);                                  // VCOM setting value
```

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SPI_0096A_WriteData(0XC8);
//ST7735 Display Inversion on
SPI_0096A_WrCmd(0X21);


// ST7735 Gamma Sequence
SPI_0096A_WrCmd(0XE0);                                  // Gamma setting value (Positive Polarity)
SPI_0096A_WriteData(0X07);  //20180612                  //  Par.1[5:0]=VRF0P[5:0]=000011'b (Variable Resistor VRHP)
SPI_0096A_WriteData(0X0E);    //20180612                //  Par.2[5:0]=VOS0P[5:0]=011011'b (Variable Resistor VRLP)
SPI_0096A_WriteData(0X08);  //20180612                  //  Par.3[5:0]=PK0P[5:0]=010010'b   (Voltage of V3 grayscale)
SPI_0096A_WriteData(0X07);  //20180612                  //  Par.4[5:0]=PK1P[5:0]=010001'b   (Voltage of V4 grayscale)
SPI_0096A_WriteData(0X10);    //20180612                  //  Par.5[5:0]=PK2P[5:0]=111111'b   (Voltage of V12 grayscale)
SPI_0096A_WriteData(0X07);  //20180612                  //  Par.6[5:0]=PK3P[5:0]=111010'b   (Voltage of V20 grayscale)
SPI_0096A_WriteData(0X02);   //20180612                 //  Par.7[5:0]=PK4P[5:0]=111010'b   (Voltage of V28 grayscale)
SPI_0096A_WriteData(0X07);  //20180612                  //  Par.8[5:0]=PK5P[5:0]=110100'b   (Voltage of V36 grayscale)
SPI_0096A_WriteData(0X09);  //20180612                  //  Par.9[5:0]=PK6P[5:0]=101111'b   (Voltage of V44 grayscale)
SPI_0096A_WriteData(0X0F);   //20180612                 //  Par.10[5:0]=PK7P[5:0]=101011'b   (Voltage of V52 grayscale)
SPI_0096A_WriteData(0X25);   //20180612                 //  Par.11[5:0]=PK8P[5:0]=110000'b   (Voltage of V56 grayscale)
SPI_0096A_WriteData(0X36);  //20180612                  //  Par.12[5:0]=PK9P[5:0]=111010'b   (Voltage of V60 grayscale)
SPI_0096A_WriteData(0X00);                              //  Par.13[5:0]=SELV0P[5:0]=000000'b   (Voltage of V0 grayscale)
SPI_0096A_WriteData(0X08);  //20180612                  //  Par.14[5:0]=SELV1P[5:0]=000001'b   (Voltage of V1 grayscale)
SPI_0096A_WriteData(0X04);    //20180612                //  Par.15[5:0]=SELV62P[5:0]=000010'b   (Voltage of V62 grayscale)
SPI_0096A_WriteData(0X10);  //20180612                  //  Par.16[5:0]=SELV63P[5:0]=001001'b   (Voltage of V63 grayscale)


SPI_0096A_WrCmd(0XE1);                                  // Gamma setting value (Negative Polarity)
SPI_0096A_WriteData(0X0A);  //20180612                  //  Par.1[5:0]=VRF0N[5:0]=000011'b (Variable Resistor VRHN)
SPI_0096A_WriteData(0X0D);    //20180612                //  Par.2[5:0]=VOS0N[5:0]=011011'b (Variable Resistor VRLN)
SPI_0096A_WriteData(0X08);  //20180612                  //  Par.3[5:0]=PK0N[5:0]=010010'b   (Voltage of V3 grayscale)
SPI_0096A_WriteData(0X07);  //20180612                  //  Par.4[5:0]=PK1N[5:0]=010001'b   (Voltage of V4 grayscale)
SPI_0096A_WriteData(0X0F);   //20180612                 //
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    Par.5[5:0]=PK2N[5:0]=110010'b   (Voltage of V12 grayscale)
124. SPI_0096A_WriteData(0X07);  //20180612                    //
    Par.6[5:0]=PK3N[5:0]=101111'b   (Voltage of V20 grayscale)
125. SPI_0096A_WriteData(0X02);   //20180612                   //
    Par.7[5:0]=PK4N[5:0]=101010'b   (Voltage of V28 grayscale)
126. SPI_0096A_WriteData(0X07);  //20180612                    //
    Par.8[5:0]=PK5N[5:0]=101111'b   (Voltage of V36 grayscale)
127. SPI_0096A_WriteData(0X09);  //20180612                    //
    Par.9[5:0]=PK6N[5:0]=101110'b   (Voltage of V44 grayscale)
128. SPI_0096A_WriteData(0X0F);   //20180612                      //
    Par.10[5:0]=PK7N[5:0]=101100'b   (Voltage of V52 grayscale)
129. SPI_0096A_WriteData(0X25);   //20180612                      //
    Par.11[5:0]=PK8N[5:0]=111001'b   (Voltage of V56 grayscale)
130. SPI_0096A_WriteData(0X35);                                  //
    Par.12[5:0]=PK9N[5:0]=111111'b   (Voltage of V60 grayscale)
131. SPI_0096A_WriteData(0X00);                                  //
    Par.13[5:0]=SELV0N[5:0]=000000'b   (Voltage of V0 grayscale)
132. SPI_0096A_WriteData(0X09);  //20180612                    //
    Par.14[5:0]=SELV1N[5:0]=000000'b   (Voltage of V1 grayscale)
133. SPI_0096A_WriteData(0X04);   //20180612                      //
    Par.15[5:0]=SELV62N[5:0]=000001'b   (Voltage of V62 grayscale)
134. SPI_0096A_WriteData(0X10);  //20180612                    //
    Par.16[5:0]=SELV63N[5:0]=001001'b   (Voltage of V63 grayscale)
135.
136. SPI_0096A_WrCmd(0XFC);                                  // Enable Gate power
    save mode
137. SPI_0096A_WriteData(0XC0);                                 //
    0XFC[7:6]=GCV_Enable[1:0]=10'b→ Gate Pump Clock Frequency disable
138.                                                             //
    0XFC[3:2]=CLK_Variable[1:0]=11'b→ Save Power Ability is Large
139. SPI_0096A_WrCmd(0X3A);
140. SPI_0096A_WriteData(0X05);                                 // 65K Mode
141.
142. SPI_0096A_WrCmd(0X2A);
143. SPI_0096A_WriteData(0X00);                                 // 65K Mode
144. SPI_0096A_WriteData(0X1A);                                  // 65K Mode
145. SPI_0096A_WriteData(0X00);                                 // 65K Mode
146. SPI_0096A_WriteData(0X69);                                 // 65K Mode
147.
148. SPI_0096A_WrCmd(0X2B);
149. SPI_0096A_WriteData(0X00);                                 // 6
150. SPI_0096A_WriteData(0X01);                                 //
151. SPI_0096A_WriteData(0X00);                                 //
152. SPI_0096A_WriteData(0XA0);                                  //
153.
154.
155. SPI_0096A_WrCmd(0X29);                                   // Display on
```