Datasheet

APM32F407VGT6S

Arm® Cortex® -M4F -based 32-bit MCU

Version: V0.5

1 Product Characteristics

- **Core**
  - 32-bit Arm® Cortex®-M4F core with FPU
  - Up to 168MHz working frequency
- **Memory and interface**
  - Flash: The capacity is up to 1MB
  - SRAM: System (192KB) + backup (4KB)
  - EMMC: Support CF card, SRAM, PSRAM, NOR and NAND memories
  - SDRAM: 2MB
- **Clock**
  - HSECLK: 4~26MHz external crystal/ceramic oscillator supported
  - LSECLK: 32.768KHz crystal/ceramic oscillator supported
  - HSICLK: 16MHz RC oscillator calibrated by factory
  - LSICLK: 28KHz RC oscillator supported
  - PLL1: Phase locked loop; output frequency is configured by four parameters
  - PLL2: Phase locked loop specially used to provide clock signals to I2S; output frequency is configured by three parameters
- **Reset and power management**
  - V_{DD} range: 1.8～3.6V
  - V_{DDA} range: 1.8～3.6V
  - V_{BAT} range of backup domain power supply: 1.65V～3.6V
  - Power-on/power-down/brown-out reset (POR/PDR/BOR) supported
  - Programmable power supply voltage detector (PVD) supported
- **Low-power mode**
  - Sleep, stop and standby modes supported
- **DMA**
  - Two DMA; each DMA has 8 data streams, 16 in total
- **Debugging interface**
  - JTAG
  - SWD
- **I/O**
  - Up to 75 I/Os
  - All I/Os can be mapped to external interrupt vector
  - Up to 73 FT input I/Os
- **Communication peripherals**
  - 4 USARTs, 2 UARTs, supporting ISO7816, LIN and IrDA functions
  - 3 I2Cs, supporting SMBus/PMBus
  - 3 SPIs (2 reusable I2Ss)
  - 2 CANs
  - 3 USB_OTG controllers
  - 1 SDIO interface
  - 1 个 Ethernet
- **Analog peripherals**
  - 3 12-bit ADCs
  - 2 12-bit DACs
- **Timer**
  - 2 16-bit advanced timers TMR1/8 that can provide 7-channel PWM output, support dead zone generation and braking input functions
  - 2 32-bit general-purpose timers TMR2/5, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
  - 8 16-bit general-purpose timers TMR/3/4/9/10/11/12/13/14, each with up to 2 independent channels to support input capture, output comparison, PWM, pulse count and other functions
  - 2 16-bit basic timers TMR6/7
  - 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
  - 1 24-bit auto decrement SysTick Timer
- **RTC**
  - Support calendar function
  - Alarm and regular wake-up from stop/standby mode
- **CRC computing unit**
- **96-bit unique device ID**

Contents

2 Product Information

See the following table for APM32F407VGT6S product functions and peripheral configuration.

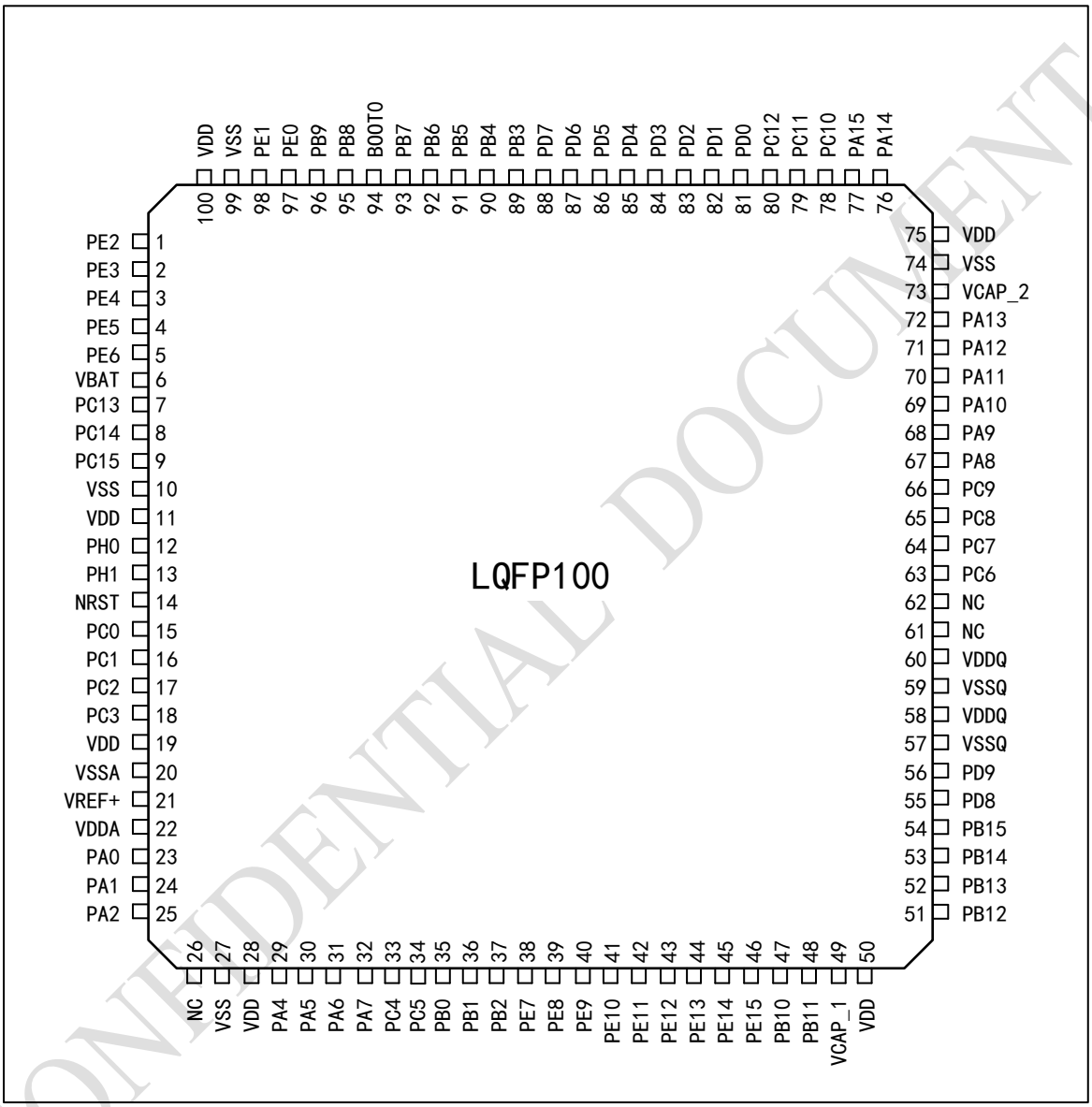
Table 1 Functions and Peripherals of APM32F407VGT6S Series Chips

Product		**APM32F407**
Model		VGT6S
Package		LQFP100
Core and maximum operating frequency		Arm® 32-bit Cortex®-M4F@168MHz
Operating voltage		1.8~3.6V
Flash(KB)		1024
System + backup SRAM(KB)		192+4
SDRAM		2MB
SMC		1
GPIOs		75
Communication interface	USART/UART	4/2
	SPI/I2S	3/2
	I2C	3
	OTG_FS	1
	OTG_HS	2
	CAN	2
	Ethernet	1
	SDIO	1
Timer	16-bit advanced	2
	32-bit general	2
	16-bit general	8
	16-bit basic	2
	System tick timer	1
	Watchdog	2
Real-time clock		1
DCI		1
RNG		1
12-bit ADC	Unit	3
	Channel	16
12 位 DAC	Unit	2
	Channel	2
Operating temperature		Ambient temperature: -40°C to 85°C Junction temperature: -40℃ to 105°C

3 Pin Information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32F407VGT6S Series LQFP100 Pins



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin

Name		Abbreviation	Definition
		I	Only input pin
		I/O	I/O pin
I/O structure		5T	FT I/O
		STDA	3.3V standard I/O, directly connected to ADC
		STD	3.3V standard I/O
		B	Dedicated Boot0 pin
		RST	Bidirectional reset pin with built-in pull-up resistor
Notes		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	
	Redefining function	Select this function through AFIO remapping register	

Table 3 Description of APM32F407VGT6S by Pin Number

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
PE2	I/O	5T	TRACECK, SMC_A23, ETH_MII_TXD3, EVENTOUT	-	1
PE3	I/O	5T	TRACED0, SMC_A19, EVENTOUT	-	2
PE4	I/O	5T	TRACED1, SMC_A20, DCI_D4, EVENTOUT	-	3
PE5	I/O	5T	TRACED2, SMC_A21, TMR9_CH1, DCI_D6, EVENTOUT	-	4
PE6	I/O	5T	TRACED3, SMC_A22, TMR9_CH2, DCI_D7, EVENTOUT	-	5
V_{BAT}	P	-	-	-	6
PC13	I/O	5T	EVENTOUT	RTC_OUT,	7

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
				RTC_TAMP1, RTC_TS	
PC14- OSC32_IN （PC14）	I/O	5T	EVENTOUT	OSC32_IN	8
PC15- OSC32_OUT （PC15）	I/O	5T	EVENTOUT	OSC32_OUT	9
V_{SS}	P	-	-	-	10
V_{DD}	P	-	Add VDD for connecting secondary PAD to SDR	-	11
PH0-OSC_IN (PH0)	I/O	5T	EVENTOUT	OSC_IN	12
PH1-OSC_OUT (PH1)	I/O	5T	EVENTOUT	OSC_OUT	13
NRST	I/O	RST	-	-	14
PC0	I/O	5T	OTG_HS_ULPI_STP, EVENTOUT	ADC123_IN10	15
PC1	I/O	5T	ETH_MDC, EVENTOUT	ADC123_IN11	16
PC2	I/O	5T	SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, I2S2ext_SD, EVENTOUT	ADC123_IN12	17
PC3	I/O	5T	SPI2_MOSI, I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, EVENTOUT	ADC123_IN13	18
V_{DD}	P	-	-	-	19
V_{SSA}	P	-	-	-	20
V_{REF+}	P	-	-	-	21
V_{DDA}	P	-	-	-	22
PA0-WKUP (PA0)	I/O	5T	USART2_CTS, UART4_TX, ETH_MII_CRS, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR,	WKUP, ADC123_IN0	23

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
			EVENTOUT		
PA1	I/O	5T	USART2_RTS, UART4_RX, ETH_RMII_REF_CLK, ETH_MII_RX_CLK, TMR5_CH2, TMR2_CH2, EVENTOUT	ADC123_IN1	24
PA2	I/O	5T	USART2_TX, TMR5_CH3, TMR9_CH1, TMR2_CH3, ETH_MDIO, EVENTOUT	ADC123_IN2	25
NC	-	-	-	-	26
V_{SS}	P	-	-	-	27
V_{DD}	P	-	-	-	28
PA4	I/O	STDA	SPI1_NSS, SPI3_NSS, USART2_CK, DCI_HSYNC, OTG_HS_SOF, I2S3_WS, EVENTOUT	DAC_OUT1, ADC12_IN4	29
PA5	I/O	STDA	SPI1_SCK, OTG_HS_ULPI_CK, TMR2_CH1_ETR, TMR8_CH1N, EVENTOUT	DAC_OUT2, ADC12_IN5	30
PA6	I/O	5T	SPI1_MISO, TMR8_BKIN, TMR13_CH1, DCI_PIXCLK, TMR3_CH1, TMR1_BKIN, EVENTOUT	ADC12_IN6	31
PA7	I/O	5T	SPI1_MOSI, TMR8_CH1N, TMR14_CH1,	ADC12_IN7	32

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
			TMR3_CH2, ETH_MII_RX_DV, TMR1_CH1N, ETH_RMII_CRS_DV, EVENTOUT		
PC4	I/O	5T	ETH_RMII_RX_D0, ETH_MII_RX_D0, EVENTOUT	ADC12_IN14	33
PC5	I/O	5T	ETH_RMII_RX_D1, ETH_MII_RX_D1, EVENTOUT	ADC12_IN15	34
PB0	I/O	5T	TMR3_CH3 TMR8_CH2N, OTG_HS_ULPI_D1, ETH_MII_RXD2, TMR1_CH2N, EVENTOUT	ADC12_IN8	35
PB1	I/O	5T	TMR3_CH4 TMR8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, TMR1_CH3N, EVENTOUT	ADC12_IN9	36
PB2-BOOT (PB2)	I/O	5T	EVENTOUT	-	37
PE7	I/O	5T	SMC_D4, TMR1_ETR, EVENTOUT	-	38
PE8	I/O	5T	SMC_D5, TMR1_CH1N, EVENTOUT	-	39
PE9	I/O	5T	SMC_D6, TMR1_CH1, EVENTOUT	-	40
PE10	I/O	5T	SMC_D7, TMR1_CH2N, EVENTOUT	-	41
PE11	I/O	5T	SMC_D8, TMR1_CH2, EVENTOUT	-	42

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
PE12	I/O	5T	SMC_D9, TMR1_CH3N, EVENTOUT	-	43
PE13	I/O	5T	SMC_D10, TMR1_CH3, EVENTOUT	-	44
PE14	I/O	5T	SMC_D11, TMR1_CH4, EVENTOUT	-	45
PE15	I/O	5T	SMC_D12, TMR1_BKIN, EVENTOUT	-	46
PB10	I/O	5T	SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, TMR2_CH3, EVENTOUT	-	47
PB11	I/O	5T	I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_RMII_TX_EN, ETH_MII_TX_EN, TMR2_CH4, EVENTOUT	-	48
V_{CAP_1}	P	-	-	-	49
V_{DD}	P	-	-	-	50
PB12	I/O	5T	SPI2_NSS, I2S2_WS, I2C2_SMBAI, USART3_CK, TMR1_BKIN, CAN2_RX, OTG_HS_ULPI_D5, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_HS_ID, EVENTOUT	-	51

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
PB13	I/O	5T	SPI2_SCK, I2S2_CK, USART3_CTS, TMR1_CH1N, CAN2_TX, OTG_HS_ULPI_D6, ETH_RMII_TXD1, ETH_MII_TXD1, EVENTOUT	OTG_HS_VBUS	52
PB14	I/O	5T	SPI2_MISO, TMR1_CH2N, TMR12_CH1, OTG_HS_DM, USART3_RTS, TMR8_CH2N, I2S2ext_SD, EVENTOUT	-	53
PB15	I/O	5T	SPI2_MOSI, I2S2_SD, TMR1_CH3N, TMR8_CH3N, TMR12_CH2, OTG_HS_DP, EVENTOUT	RTC_REFIN	54
PD8	I/O	5T	SMC_D13, USART3_TX, EVENTOUT	-	55
PD9	I/O	5T	SMC_D14, USART3_RX, EVENTOUT	-	56
VSSQ	P	-	-	-	57
VDDQ	P	-	-	-	58
VSSQ	P	-	-	-	59
VDDQ	P	-	-	-	60
NC	-	-	-	-	61
NC	-	-	-	-	62
PC6	I/O	5T	I2S2_MCK, TMR8_CH1, SDIO_D6,	-	63

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
			USART6_TX, DCI_D0, TMR3_CH1, EVENTOUT		
PC7	I/O	5T	I2S3_MCK, TMR8_CH2, SDIO_D7, USART6_RX, DCI_D1, TMR3_CH2, EVENTOUT	-	64
PC8	I/O	5T	TMR8_CH3, SDIO_D0, TMR3_CH3, USART6_CK, DCI_D2, EVENTOUT	-	65
PC9	I/O	5T	I2S_CKIN, MCO2, TMR8_CH4, SDIO_D1, I2C3_SDA, DCI_D3, TMR3_CH4, EVENTOUT	-	66
PA8	I/O	5T	USART1_CK, TMR1_CH1, MCO, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-	67
PA9	I/O	5T	USART1_TX, TMR1_CH2, I2C3_SMBAI, DCI_D0, EVENTOUT	OTG_FS_VBUS	68
PA10	I/O	5T	USART1_RX, TMR1_CH3, OTG_FS_ID, DCI_D1,	-	69

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
			EVENTOUT		
PA11	I/O	5T	USART1_CTS, CAN1_RX, TMR1_CH4, OTG_FS_DM, EVENTOUT	-	70
PA12	I/O	5T	USART1_RTS, CAN1_TX, TMR1_ETR, OTG_FS_DP, EVENTOUT	-	71
PA13 (JTMS-SWDIO)	I/O	5T	JTMS-SWDIO, EVENTOUT	PA13	72
V_{CAP_2}	P	-	-	-	73
V_{SS}	P	-	-	-	74
V_{DD}	P	-	-	-	75
PA14 (JTCK/SWCLK)	I/O	5T	JTCK-SWCLK, EVENTOUT	-	76
PA15 (JTDI)	I/O	5T	JTDI, SPI3_NSS, I2S3_WS, TMR2_CH1_ETR, SPI1_NSS, EVENTOUT	-	77
PC10	I/O	5T	SPI3_SCK, I2S3_CK, UART4_TX, SDIO_D2, DCI_D8, USART3_TX, EVENTOUT	-	78
PC11	I/O	5T	UART4_RX, SPI3_MISO, SDIO_D3, DCI_D4, USART3_RX, I2S3ext_SD, EVENTOUT	-	79
PC12	I/O	5T	UART5_TX,	-	80

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
			SDIO_CK, DCI_D9, SPI3_MOSI, I2S3_SD, USART3_CK, EVENTOUT		
PD0	I/O	5T	SMC_D2, CAN1_RX, EVENTOUT	-	81
PD1	I/O	5T	SMC_D3, CAN1_TX, EVENTOUT	-	82
PD2	I/O	5T	TMR3_ETR, UART5_RX, SDIO_CMD, DCI_D11, EVENTOUT	-	83
PD3	I/O	5T	SMC_CLK, USART2_CTS, EVENTOUT	-	84
PD4	I/O	5T	SMC_NOE, USART2_RTS, EVENTOUT	-	85
PD5	I/O	5T	SMC_NWE, USART2_TX, EVENTOUT	-	86
PD6	I/O	5T	SMC_NWAIT, USART2_RX, EVENTOUT	-	87
PD7	I/O	5T	SMC_NE1, SMC_NCE2, USART2_CK, EVENTOUT	-	88
PB3 (JTDO/TRACESWO)	I/O	5T	JTDO, TRACESWO, SPI3_SCK, I2S3_CK, TMR2_CH2, SPI1_SCK, EVENTOUT	-	89

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
PB4 (NJTRST)	I/O	5T	NJTRST, SPI3_MISO, TMR3_CH1, SPI1_MISO, I2S3ext_SD, EVENTOUT	-	90
PB5	I/O	5T	I2C1_SMBAI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TMR3_CH2, SPI1_MOSI, SPI3_MOSI, DCI_D10, I2S3_SD, EVENTOUT	-	91
PB6	I/O	5T	I2C1_SCL, TMR4_CH1, CAN2_TX, DCI_D5, USART1_TX, EVENTOUT	-	92
PB7	I/O	5T	I2C1_SDA, SMC_NL, DCI_VSYNC, USART1_RX, TMR4_CH2, EVENTOUT	-	93
BOOT0	I	B	-	V_{PP}	94
PB8	I/O	5T	TMR4_CH3, SDIO_D4, TMR10_CH1, DCI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-	95
PB9	I/O	5T	SPI2_NSS, I2S2_WS, TMR4_CH4,	-	96

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP100
			TMR11_CH1, SDIO_D5, DCI_D7, I2C1_SDA, CAN1_TX, EVENTOUT		
PE0	I/O	5T	TMR4_ETR, SMC_NBL0, DCI_D2, EVENTOUT	-	97
PE1	I/O	5T	SMC_NBL1, DCI_D3, EVENTOUT	-	98
V_{DD}	P	-	-	-	100

Note:

(1) PC13, PC14 and PC15 are powered through the power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:

① The speed shall not exceed 2MHz when the heavy load is 30pF;

② Not used for current source (e.g. driving LED).

3.3 GPIO Multiplexing Function Configuration

Table 4 GPIOA Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	TMR2_CH1_ETR	TMR5_CH1	TMR8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
PA1	-	TMR2_CH2	TMR5_CH2	-	-	-	-	USART2_RTS	UART4_RX	-	-	ETH_MII_RX_CLK ETH_RMII_REF_CLK	-	-	-	EVENTOUT
PA2	-	TMR2_CH3	TMR5_CH3	TMR9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCI_HSYNC	-	EVENTOUT
PA5	-	TMR2_CH1_ETR		TMR8_CH1N	-	SPI1_SCK	-	-	-		OTG_HS_ULPI_CK	-	-	-	-	EVENTOUT
PA6	-	TMR1_BKIN	TMR3_CH1	TMR8_BKIN	-	SPI1_MISO	-	-	-	TMR13_CH1	-	-	-	DCI_PIXCK	-	EVENTOUT
PA7	-	TMR1_CH1N	TMR3_CH2	TMR8_CH1N	-	SPI1_MOSI	-	-	-	TMR14_CH1	-	ETH_MII_RX_DV ETH_RMII_CRS_DV	-	-	-	EVENTOUT
PA8	MCO1	TMR1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
PA9	-	TMR1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-	-	-	-	DCI_D0	-	EVENTOUT
PA10	-	TMR1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCI_D1	-	EVENTOUT
PA11	-	TMR1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
PA12	-	TMR1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
PA13	JTMS_SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PA14	JTCK_SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PA15	JTDI	TMR2_CH1 TMR2_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2C3_WS	-	-	-	-	-	-	-	-	EVENTOUT

Table 5 GPIOB Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	TMR1_CH2N	TMR3_CH3	TMR8_CH2N	-	-	-	-	-	-	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	-	EVENTOUT
PB1	-	TMR1_CH3N	TMR3_CH4	TMR8_CH3N	-	-	-	-	-	-	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	-	EVENTOUT
PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO/TRACESWO	TMR2_CH2	-	-	-	SPI1_SCK	SPI3_SCK I2S3_CK	-	-	-	-	-	-	-	-	EVENTOUT
PB4	NJTRST	-	TMR3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	-	-	-	-	-	-	EVENTOUT
PB5	-	-	TMR3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	-	DCI_D10	-	EVENTOUT
PB6	-	-	TMR4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	-	DCI_D5	-	EVENTOUT
PB7	-	-	TMR4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	SMC_NL	DCI_VSYNC	-	EVENTOUT
PB8	-	-	TMR4_CH3	TMR10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDIO_D4	DCI_D6	-	EVENTOUT
PB9	-	-	TMR4_CH4	TMR11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCI_D7	-	EVENTOUT
PB10	-	TMR2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	-	EVENTOUT
PB11	-	TMR2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN ETH _RMII_TX_EN	-	-	-	EVENTOUT
PB12	-	TMR1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH_RMII_TXD0 ETH_MII_TXD0	OTG_HS_ID	-	-	EVENTOUT
PB13	-	TMR1_CH1N	-	-	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH_RMII_TXD1 ETH_MII_TXD1	-	-	-	EVENTOUT
PB14	-	TMR1_CH2N	-	TMR8_CH2N	-	SPI2_MISO	I2S2ext_SD	USART3_RTS	-	TMR12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
PB15	RTC_REFIN	TMR1_CH3N	-	TMR8_CH3N	-	SPI2_MOSI I2S2_SD	-	-	-	TMR12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT

Table 6 GPIOC Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_STP	-	-	-	-	EVENTOUT
PC1	-	-	-	-	-	-	-	-	-	-	-	ETH_MDC	-	-	-	EVENTOUT
PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	OTG_HS_ULPI_DIR	ETH_MII_TXD2	-	-	-	EVENTOUT
PC3	-	-	-	-	-	SPI2_MOSI I2S2_SD	-	-	-	-	OTG_HS_ULPI_NXT	ETH _MII_TX_CLK	-	-	-	EVENTOUT
PC4	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0 ETH_RMII_RXD0	-	-	-	EVENTOUT
PC5	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD1 ETH_RMII_RXD1	-	-	-	EVENTOUT
PC6	-	-	TMR3_CH1	TMR8_CH1	-	I2S2_MCK	-	-	USART6_TX	-	-	-	SDIO_D6	DCI_D0	-	EVENTOUT
PC7	-	-	TMR3_CH2	TMR8_CH2	-	-	I2S3_MCK	-	USART6_RX	-	-	-	SDIO_D7	DCI_D1	-	EVENTOUT
PC8	-	-	TMR3_CH3	TMR8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCI_D2	-	EVENTOUT
PC9	MCO2	-	TMR3_CH4	TMR8_CH4	I2C3_SDA	I2S_CKIN	-	-	-	-	-	-	SDIO_D1	DCI_D3	-	EVENTOUT
PC10	-	-	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX/	UART4_TX	-	-	-	SDIO_D2	DCI_D8	-	EVENTOUT
PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	-	-	-	SDIO_D3	DCI_D4	-	EVENTOUT
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCI_D9	-	EVENTOUT
PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 7 GPIOD Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	SMC_D2	-	-	EVENTOUT
PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	SMC_D3	-	-	EVENTOUT
PD2	-	-	TMR3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCI_D11	-	EVENTOUT
PD3	-	-	-	-	-	-	-	USART2_CTS	-	-	-	-	SMC_CLK	-	-	EVENTOUT
PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	SMC_NOE	-	-	EVENTOUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	SMC_NWE	-	-	EVENTOUT
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	SMC_NWAIT	-	-	EVENTOUT
PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	SMC_NE1/SMC_NCE2	-	-	EVENTOUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	SMC_D13	-	-	EVENTOUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	SMC_D14	-	-	EVENTOUT

Table 8 GPIOE Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	-	-	TMR4_ETR	-	-	-	-	-	-	-	-	-	SMC_NBL0	DCI_D2	-	EVENTOUT
PE1	-	-	-	-	-	-	-	-	-	-	-	-	SMC_NBL1	DCI_D3	-	EVENTOUT
PE2	TRACECLK	-	-	-	-	-	-	-	-	-	-	ETH_MII_TXD3	SMC_A23	-	-	EVENTOUT
PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	-	SMC_A19	-	-	EVENTOUT
PE4	TRACED1	-	-	-	-	-	-	-	-	-	-	-	SMC_A20	DCI_D4	-	EVENTOUT
PE5	TRACED2	-	-	TMR9_CH1	-	-	-	-	-	-	-	-	SMC_A21	DCI_D6	-	EVENTOUT
PE6	TRACED3	-	-	TMR9_CH2	-	-	-	-	-	-	-	-	SMC_A22	DCI_D7	-	EVENTOUT
PE7	-	TMR1_ETR	-	-	-	-	-	-	-	-	-	-	SMC_D4	-	-	EVENTOUT
PE8	-	TMR1_CH1N	-	-	-	-	-	-	-	-	-	-	SMC_D5	-	-	EVENTOUT
PE9	-	TMR1_CH1	-	-	-	-	-	-	-	-	-	-	SMC_D6	-	-	EVENTOUT
PE10	-	TMR1_CH2N	-	-	-	-	-	-	-	-	-	-	SMC_D7	-	-	EVENTOUT
PE11	-	TMR1_CH2	-	-	-	-	-	-	-	-	-	-	SMC_D8	-	-	EVENTOUT
PE12	-	TMR1_CH3N	-	-	-	-	-	-	-	-	-	-	SMC_D9	-	-	EVENTOUT
PE13	-	TMR1_CH3	-	-	-	-	-	-	-	-	-	-	SMC_D10	-	-	EVENTOUT
PE14	-	TMR1_CH4	-	-	-	-	-	-	-	-	-	-	SMC_D11	-	-	EVENTOUT
PE15	-	TMR1_BKIN	-	-	-	-	-	-	-	-	-	-	SMC_D12	-	-	EVENTOUT

Table 9 GPIOH Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

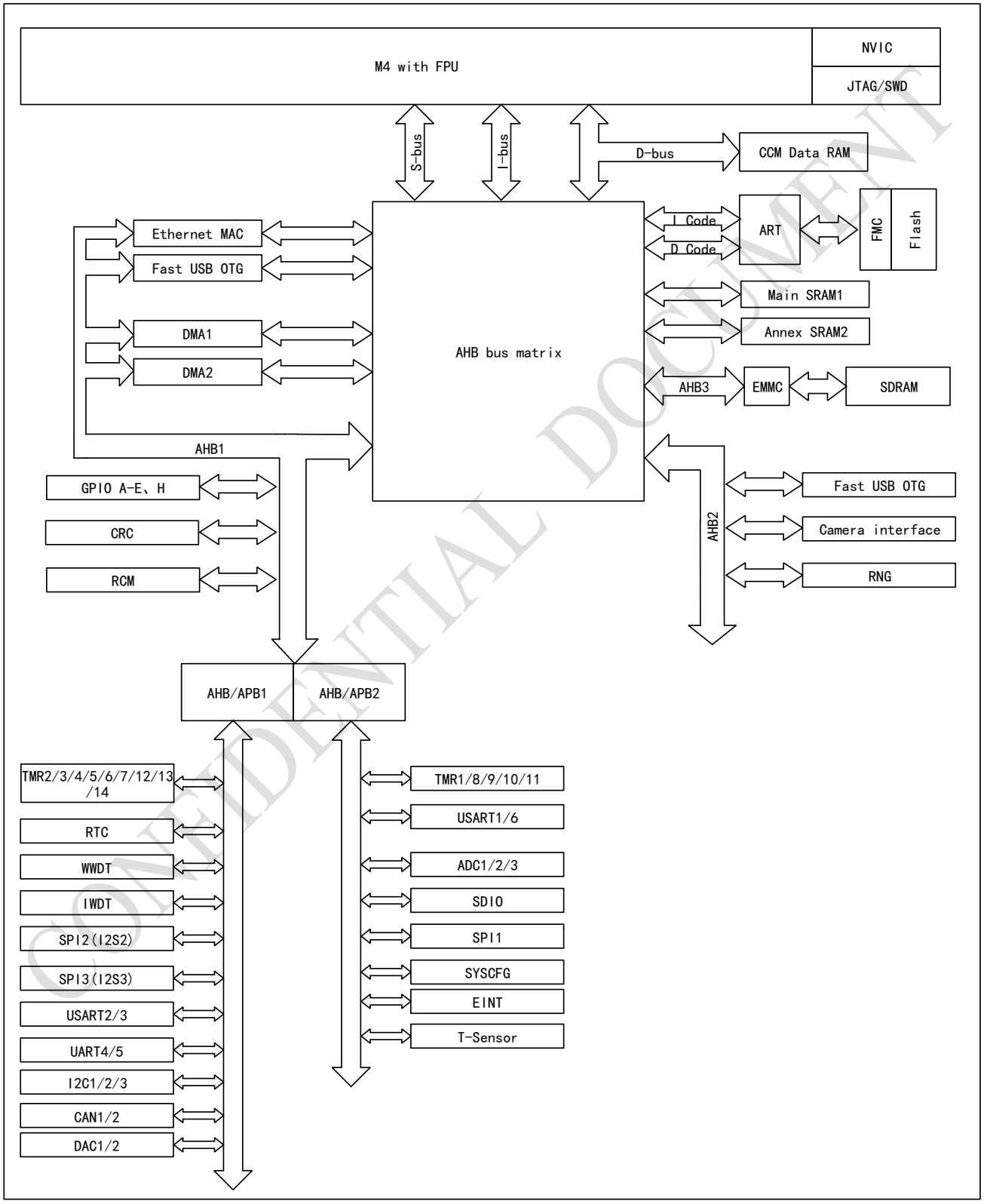
4 Function Description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32F407VGT6S series products; for information about the Arm® Cortex®-M4F core, please refer to the *Arm® Cortex®-M4F Technical Reference Manual*, which can be downloaded from Arm's website.

4.1 System architecture

4.1.1 System block diagram

Figure 2 APM32F407VGT6S System Block Diagram



4.1.2 Address mapping

Table 10 APM32F407VGT6S Series Address Mapping Diagram

Region	Start Address	Peripheral Name
Code	0x0000 0000	Code mapping area
Code	0x0800 0000	FLASH
Code	0x0810 0000	Reserve
Code	0x1FFF 0000	System memory area
Code	0x1FFF C000	Option byte
Code	0x1FFF C008	Reserve
SRAM	0x2000 0000	SRAM
—	0x2002 0000	Reserve
APB1 bus	0x4000 0000	TMR2
APB1 bus	0x4000 0400	TMR3
APB1 bus	0x4000 0800	TMR4
APB1 bus	0x4000 0C00	TMR5
APB1 bus	0x4000 1000	TMR6
APB1 bus	0x4000 1400	TMR7
APB1 bus	0x4000 1800	TMR12
APB1 bus	0x4000 1C00	TMR13
APB1 bus	0x4000 2000	TMR14
APB1 bus	0x4000 2400	Reserve
APB1 bus	0x4000 2800	RTC
APB1 bus	0x4000 2C00	WWDT
APB1 bus	0x4000 3000	IWDT
APB1 bus	0x4000 3400	I2S2ext
APB1 bus	0x4000 3800	SPI2/I2S2
APB1 bus	0x4000 3C00	SPI3/I2S3
APB1 bus	0x4000 4000	I2S3ext
APB1 bus	0x4000 4400	USART2
APB1 bus	0x4000 4800	USART3
APB1 bus	0x4000 4C00	UART4
APB1 bus	0x4000 5000	UART5
APB1 bus	0x4000 5400	I2C1
APB1 bus	0x4000 5800	I2C2
APB1 bus	0x4000 5C00	I2C3
APB1 bus	0x4000 6000	Reserve
APB1 bus	0x4000 6400	CAN1
APB1 bus	0x4000 6800	CAN2
APB1 bus	0x4000 6C00	Reserve

Region	Start Address	Peripheral Name
APB1 bus	0x4000 7000	PMU
APB1 bus	0x4000 7400	DAC
APB1 bus	0x4000 7800	Reserve
—	0x4000 8000	Reserve
APB2 bus	0x4001 0000	TMR1
APB2 bus	0x4001 0400	TMR8
APB2 bus	0x4001 0800	Reserve
APB2 bus	0x4001 1000	USART1
APB2 bus	0x4001 1400	USART6
APB2 bus	0x4001 1800	Reserve
APB2 bus	0x4001 2000	ADC1/2/3
APB2 bus	0x4001 2400	Reserve
APB2 bus	0x4001 2C00	SDI0
APB2 bus	0x4001 3000	SPI1
APB2 bus	0x4001 3400	Reserve
APB2 bus	0x4001 3800	SYSCFG
APB2 bus	0x4001 3C00	EINT
APB2 bus	0x4001 4000	TMR9
APB2 bus	0x4001 4400	TMR10
APB2 bus	0x4001 4800	TMR11
APB2 bus	0x4001 4C00	Reserve
—	0x4001 5800	Reserve
AHB bus	0x4002 0000	GPIOA
AHB bus	0x4002 0400	GPIOB
AHB bus	0x4002 0800	GPIOC
AHB bus	0x4002 0C00	GPIOD
AHB bus	0x4002 1000	GPIOE
AHB bus	0x4002 1C00	GPIOH
AHB bus	0x4002 2400	Reserve
AHB bus	0x4002 3000	CRC
AHB bus	0x4002 3400	Reserve
AHB bus	0x4002 3800	RCM
AHB bus	0x4002 3C00	FMC Reg.
AHB bus	0x4002 4000	Backups SRAM
AHB bus	0x4002 5000	Reserve
AHB bus	0x4002 6000	DMA1
AHB bus	0x4002 6400	DMA2
AHB bus	0x4002 6800	Reserve

Region	Start Address	Peripheral Name
AHB bus	0x4002 8000	MAC
AHB bus	0x4002 9400	Reserve
AHB bus	0x4004 0000	USB OTG_HS1/2
AHB bus	0x4008 0000	Reserve
AHB bus	0x5000 0000	USB OTG_FS
AHB bus	0x5004 0000	Reserve
AHB bus	0x5005 0000	DCI
AHB bus	0x5005 0400	Reserve
AHB bus	0x5006 0800	RNG
AHB bus	0x5006 0C00	Reserve
AHB bus	0xA000 0000	SMC Reg.
—	0xA000 1000	Reserve
Core	0xE000 0000	Core peripheral
—	0xE010 0000	Reserve

4.1.3 Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use serial interface to reprogram the user Flash if starting up from BootLoader.

4.2 Core

The core of APM32F407VGT6S is Arm® Cortex®-M4F with FPU computing unit. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 85 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M4F) and 8 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 23 edge detectors, and each detector

includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 75 GPIOs can be connected to 16 external interrupt lines.

4.4 On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program when leaving the factory and cannot be erased.

Table 11 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	1MB	Store user programs and data
SRAM	192 KB (System) + 4KB(backup)	CPU can access at 0 wait cycle (read/write)
System memory area	30KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode
SDRAM	2MB	Store a large amount of temporary data, which can be cached and read

4.4.1 Static memory controller (SMC)

APM32F407VGT6S series integrates SMC module and supports PC card, SRAM, PSRAM, NorFlash and NandFlash.

Function introduction:

- Can be logically or connected to NVIC units
- Write FIFO
- The code can run in off-chip memories except NAND flash and PC card
- Connect to LCD

4.4.2 LCD parallel interface (LCD)

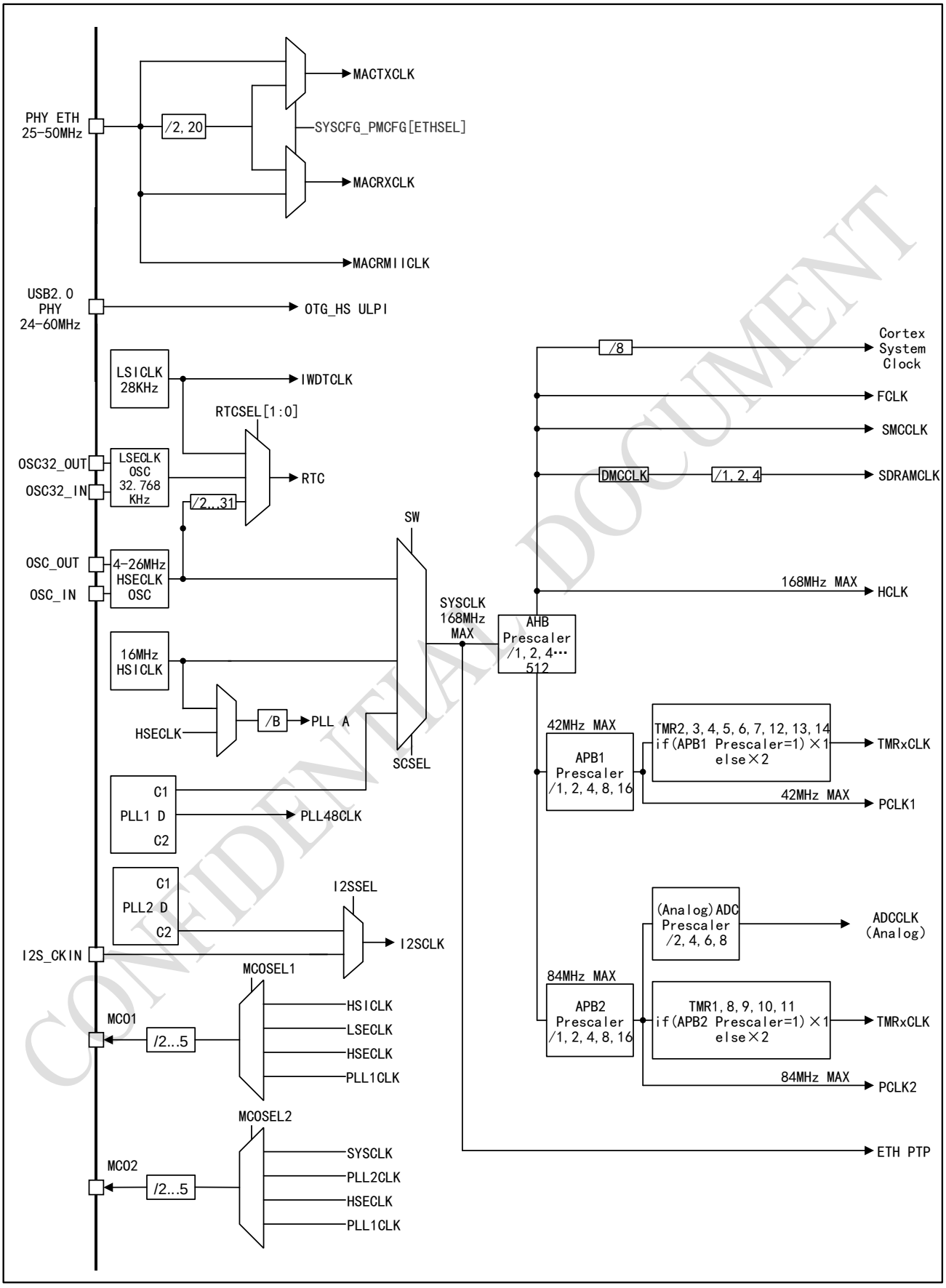
SMC can be configured to seamlessly connect with most graphic LCD controllers, and supports the modes of Intel 8080 and Motorola 6800, and can flexibly connect with specific LCD interface. This LCD parallel interface can be used to easily build a simple graphics application environment or the high-performance scheme of the special acceleration controller can be used.

4.5 Clock

4.5.1 Clock tree

Clock tree of APM32F407VGT6S is shown in the figure below:

Figure 3 APM32F407VGT6S Clock Tree



4.5.2 Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; besides, some modules may have additional clock source pins to obtain the required clock frequency through external circuits.

4.5.3 System clock

HSICLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be HSICLK or HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency division factor.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.4 Bus clock

AHB, APB1 and APB2 buses are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency division factor. The maximum frequency of AHB is 168MHz, the maximum frequency of APB2 is 84MHz, and the maximum frequency of APB1 is 42MHz.

4.5.5 Phase locked loop

APM32F407VGT6S series product has two PLL, one is PLL (PLL1), and the other is PLL (PLL2) specially used to provide specific clock frequency for I2S. They all need to generate different clock frequencies by configuring parameters. Please refer to the *User Manual* for specific parameters and configuration registers.

4.6 Power and power management

4.6.1 Power supply scheme

Table 12 Power Supply Scheme

Name	Voltage range	Description
V_{DD}	1.8～3.6V	I/O (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDA}/V_{SSA}	1.8～3.6V	Supply power for ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is used, V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.
V_{BAT}	1.8～3.6V	When V_{DD} is disabled, RTC, external 32KHz oscillator and backup register are powered through internal power switch.

4.6.2 Voltage regulator

Table 13 Regulator Operating Mode

Name	Description
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode; when the voltage regulator has high-impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power supply voltage monitor

Power-on reset (POR), power-down reset (PDR) and brown-out reset circuits are integrated inside the product. These three circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable power supply voltage monitor (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7 Low-power mode

APM32F407VGT6S supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 14 Low-power Mode

Mode	Description
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the lowest power consumption can be achieved in stop mode; The clock of the internal 1.3V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be disabled, and the voltage regulator can be configured in normal mode or low-power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USB_OTG.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.3V power supply modules are powered down, HSECLK crystal resonator, and HSICLK clocks are disabled, SRAM and register data disappear, RTC area and backup register contents remain, and the standby circuit still works;

Mode	Description
	The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8 DMA

2 built-in DMA, 16 data streams in total. Each data stream corresponds to 8 channels, but each data stream can only use 1 channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" data transmission (the memory includes Flash、SRAM、SDRAM).

4.9 GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input and output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.10 Communication peripherals

4.10.1 USART/UART

Up to 6 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART1/6 interfaces can communicate at a rate of 10.5Mbit/s, while other USART/UART interfaces can communicate at a rate of 5.25Mbit/s. All USART/UART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; they all can support DMA. USART/UART function differences are shown in the table below:

Table 15 USART/UART Function Differences

USART mode/function	USART1	USART2	USART3	UART4	UART5	USART6
Hardware flow control of modem	√	√	√	—	—	√
Smart card mode	√	√	√	—	—	√
IrDA SIR coder-encoder functions	√	√	√	√	√	√
LIN mode	√	√	√	√	√	√
Standard characteristics	√	√	√	√	√	√
SPI host	√	√	√	—	—	√
Maximum baud rate under 16-time oversampling (Mbit/s)	5.25	2.62	2.62	2.62	2.62	5.25

USART mode/function	USART1	USART2	USART3	UART4	UART5	USART6
Maximum baud rate under 8-time oversampling (Mbit/s)	10.50	5.25	5.25	5.25	5.25	10.5
APB mapping	APB2	APB1	APB1	APB1	APB1	APB2

Note: √ = support.

4.10.2 I2C

I2C1/2/3 bus interfaces are built-in and they all can work in multiple-master or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

4.10.3 SPI/I2S

3 built-in SPI, support full-duplex and half-duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and 3 SPI can communicate at a rate of up to 42Mbit/s, 21MBit/s and 21MBit/s respectively.

2 built-in I2S (multiplexed with SPI2 and SPI3 respectively), support half-duplex communication in master mode and slave mode, support synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transfer with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~192kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256-time sampling frequency.

4.10.4 CAN

2 built-in CAN, compatible with 2.0A and 2.0B (active) specification, and can communicate at a rate of up to 1Mbit/s. It can receive and transmit standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes and 2 receiving FIFO, and 14 3-level adjustable filters.

4.10.5 USB_OTG

Three USB controllers, namely, one OTG_FS and two OTG_HS, are embedded in the product. They all can support both host and slave functions to comply with the On-The-Go supplementary standard of USB 2.0 specification, and can also be configured as "Host only" or "Slave only" mode, to fully comply with USB 2.0 specification. OTG_FS clock (48MHz) is output by specific PLL, and OTG_HS clock (60MHz) is provided by external PHY.

4.10.6 Ethernet

Provides an IEEE-802.3-2002 compatible MAC for Ethernet LAN communication over MII or RMII. This MCU requires a PHY connection to a physical LAN bus. The PHY connects to the MII port, uses 17 signals for MII or 9 signals for RMII, and can use a 25MHz clock (MII) from the kernel.

4.10.7 SDIO

The secure digital input/output interface can connect SD card, SD I/O card, multi-media card (MMC) and CE-ATA card master interfaces, and provide data transmission between APB2 system bus and SD memory card, SD I/O card, MMC and CE-ATA device.

4.11 Analog peripherals

4.11.1 ADC

3 built-in ADC with 12-bit accuracy, up to 16 external channels and 3 internal channels for each ADC. The internal channels measure the temperature sensor voltage, reference voltage and backup voltage respectively. A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16-bit data register; they support analog watchdog, and DMA.

4.11.1.1 Temperature sensor

1 temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature and the converted voltage value can be obtained by ADC and converted into temperature.

4.11.1.2 Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel; V_{REFINT} can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.11.2 DAC

2 built-in 12-bit DAC, each corresponding to an output channel, which can be configured as 8-bit and 12-bit modes, and the DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion and the trigger mode supports external signal trigger and internal timer update trigger.

4.12 Timer

2 built-in 16-bit advanced timers (TMR1/8), 8 16-bit general-purpose timers (TMR3/4/9/10/11/12/13/14), 2 32-bit general timers (TMR2/5), 2 16-bit basic timers (TMR6/7), 1 independent watchdog timer, 1 window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 16 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	System tick timer	Basic timer	General-purpose timer			Advanced timer
Timer name	Sys Tick Timer	TMR6/7	TMR2/5	TMR3/4	TMR9/10/11/12/13/14	TMR1/8
Counter resolution	24 bits	16 bits	32 bits	16 bits	16 bits	16 bits
Counter type	Down	Up	Up, down, up/down		Up	Up, down, up/down
Prescaler factor	-	Any integer between 1 and 65536	Any integer between 1 and 65536			Any integer between 1 and 65536
Generate DMA request	-	OK	OK			OK
Capture/compare register	-	-	4			4
Complementary output	-	None	None			Yes
Pin characteristics	-	-	1-way external trigger signal input pin; 4-way non-complementary channel pin.			1-way external trigger signal input pin; 1-way braking input signal pin; 3-pair complementary channel pins; 1-way non-complementary channel pin.
Function Description	Special for real-time operating system. Automatic reloading function supported. When the counter is 0, it can generate a maskable system interrupt.	Used to generate DAC trigger signals. Can be used as a 16-bit general-purpose timebase counter.	Synchronization or event chaining function provided. Timers in debug mode can be frozen. Can be used to generate PWM output. Each timer has independent DMA request mechanism. It can handle incremental encoder signals.			It has complementary PWM output with dead band insertion. When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen,

Timer type	System tick timer	Basic timer	General-purpose timer	Advanced timer
	Can program the clock source.			and PWM output is disabled. Synchronization or event chaining function provided.

Table 17 Function Comparison between IWDT and WWDT

Name	Counter resolution	Counter type	Prescaler factor	Function description
Independent watchdog	12 bits	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 28KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7 bits	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.13 RTC

1 RTC is built in, and there are LSECLK signal input pins (OS32_IN and OS32_OUT) and 2 TAMP input signal detection pins (RTC_TAMP1/2); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is powered by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data will not be lost in case of system reset, software reset and power-on reset; it supports clock and calendar functions.

4.13.1 Backup domain

4KB backup SRAM and 20 backup registers are built in, and are powered by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system reset, software reset and power-on reset.

4.14 RNG

A RNG is embedded, and it provides 32-bit random number generated by the integrated simulation.

4.15 DCI

DCI is used to receive high-speed data streams from CMOS camera. It supports different data formats and is applicable to black-and-white cameras, X24 cameras and so on.

4.16 CRC

1 CRC (cyclic redundancy check) computing unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5 Electrical Characteristics

5.1 Test conditions of electrical characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2 Typical value

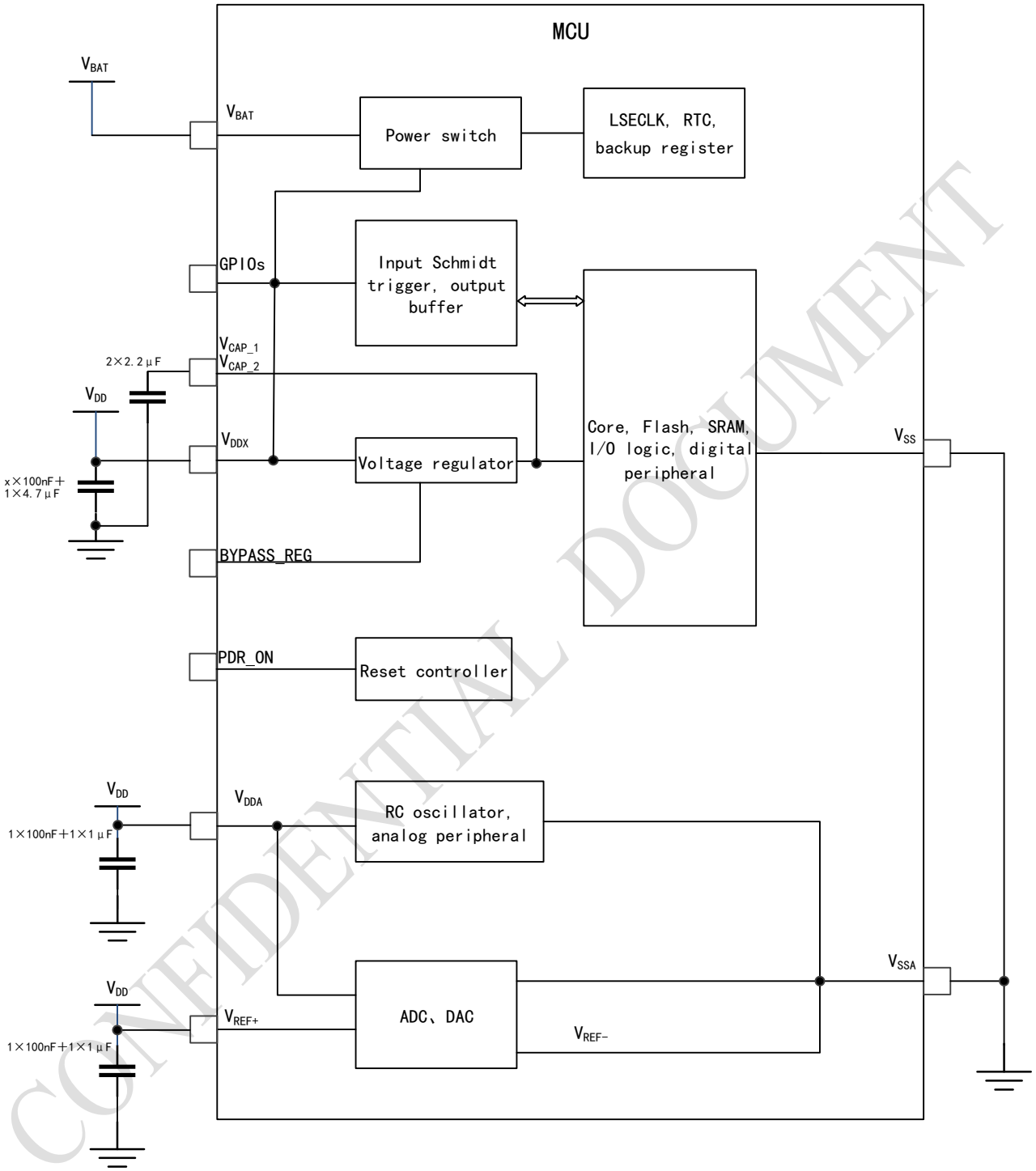
Unless otherwise specified, typical data are measured based on T_A=25℃, V_{DD}=V_{DDA}=3.3V. These data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4 Power supply scheme

Figure 4 Power Supply Scheme



Notes: V_{DDx} in the figure means the number of V_{DD} is x

5.1.5 Load capacitance

Figure 5 Load conditions when measuring pin parameters

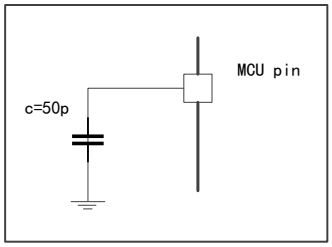


Figure 6 Pin Input Voltage Measurement Scheme

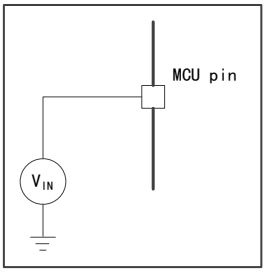
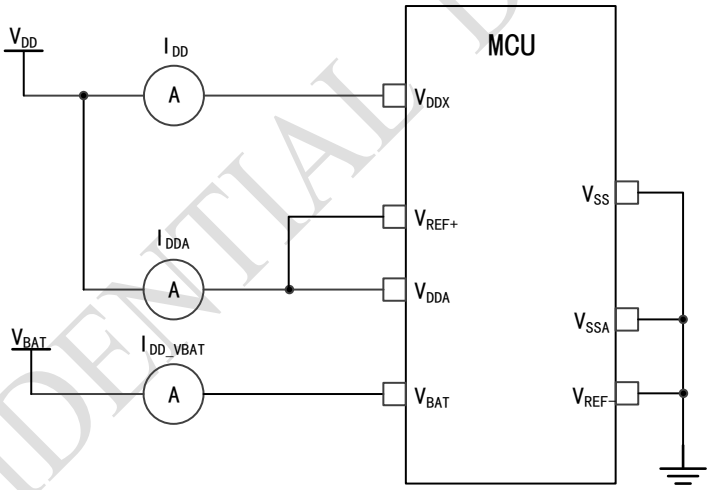


Figure 7 Power Consumption Measurement Scheme



5.2 Test under general operating conditions

Table 18 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	168	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	42	
f_{PCLK2}	Internal APB2 clock frequency	-	-	84	
V_{DD}	Main power supply voltage	-	1.8	3.6	V
V_{DDA}	Analog power supply voltage	Must be the same	1.8	2.4	V

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
	(When neither ADC nor DAC is used)	as V_{DD}			
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.65	3.60	V
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	℃

5.3 Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1 Maximum temperature characteristics

Table 19 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65 ~ +150	℃
T_J	Maximum junction temperature	105	℃

5.3.2 Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 20 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on FT pins	V_{SS}-0.3	V_{DD}+4	
	Input voltage on other pins	V_{SS}-0.3	4.0	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different grounding pins	-	50	

5.3.3 Maximum rated current characteristics

Table 21 Current Characteristics

Symbol	Description	Maximum value	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) (1)	240	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) (1)	240	

Symbol	Description	Maximum value	Unit
I_{IO}	Sink current on any I/O and control pin	25	
	Source current on any I/O and control pin	25	
$I_{INJ(PIN)}$ (2)	Injection current of 5T pin	-5/+0	
	Injection current of other pins	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (4)	±25	

1. All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) must always be within the allowed range.
2. The outflow current will interfere with the analog performance of the device.
3. I/O cannot be injected positively: when $V_{IN}<V_{SS}$, $I_{INJ(PIN)}$ cannot exceed the maximum allowable input voltage value.
4. If V_{IN} exceeds the maximum value, IINJ(PIN) must be externally limited not to exceed the maximum value. When $V_{IN}> V_{DD}$, the current flows into the pins; when $V_{IN}<V_{SS}$, the current flows out of the pins.
5. When the current is injected into several I/O ports at the same time, the maximum value of ΣIINJ(PIN) is the sum of instantaneous absolute value of inflow current and outflow current.

5.3.4 Electro-static discharge (ESD)

Table 22 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Range	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	TA=+25 ℃, conforming to JESD22-A114	±4000	V

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5 Static latch-up (LU)

Table 23 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A=+85℃, conforming to JESD78A	±200mA

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4 On-chip memory

5.4.1 Flash characteristics

Table 24 Flash Memory Characteristics

Symbol	Parameter		Conditions	Minimum value	Typical value	Maximum value	Unit
t_{prog}	8/16/32-bit programming time		T_A = -40~85℃ V_{DD}=2.4~3.6V	-	43	60	μs
t_{ERASE1}	Page (16KBytes) erase time	8 bits	T_A = -40~85℃ V_{DD}=2.4~3.6V	-	60	120	ms
		16 bits		-	60	120	
		32 bits		-	60	120	

Symbol	Parameter		Conditions	Minimum value	Typical value	Maximum value	Unit
t_{ERASE2}	Page (64KBytes) erase time	8 bits		-	250	500	
		16 bits		-	250	500	
		32 bits		-	250	500	
t_{ERASE3}	Page (128KBytes) erase time	8 bits		-	500	1000	
		16 bits		-	500	1000	
		32 bits		-	500	1000	
t_{ME}	Mass erase time	8 bits	T_A = -40~85℃ V_{DD}=2.4~3.6V	-	10	20	ms
		16 bits		-	10	20	
		32 bits		-	10	20	
V_{prog}	Voltage of 8-bit programming		T_A = -40~85℃	1.8	-	3.6	V
	Voltage of 16-bit programming			2.1	-	3.6	
	Voltage of 32-bit programming			2.7	-	3.6	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5 Clock

5.5.1 Characteristics of external clock source

5.5.1.1 High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 25 HSECLK4~26MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	26	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, C_L=10pF@8MHz	-	-	0.5	mA
$t_{SU(HSECLK)}$	Start-up Time	V_{DD} is stable	-	2	-	ms

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5.1.2 Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 26 LSECLK Oscillator Characteristics (f_{LSECLK} =32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	-	32.768	-	KHz
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	-	1	μA
$t_{SU(LSECLK)}$(1)	Start-up Time	V_{DD} is stable	-	2	-	s

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

(1) $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured by using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2 Characteristics of internal clock source

5.5.2.1 High-speed internal (HSICLK) RC oscillator

Table 27 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	16	-	MHz
$A_{CC(HSICLK)}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~85℃	-2	-	4	%
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	100	120	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V，T_A=-40~85℃		-	3.7	5	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5.2.2 Low-speed internal (LSICLK) RC oscillator

Table 28 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD}=2-3.6V, T_A =-40~85℃)	20	28	35	KHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.4	0.6	μA
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator, (V_{DD}=3.3V，T_A=-40~85℃)	-	16	40	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5.3 PLL Characteristics

Table 29 PLL1 Characteristics

Symbol	Parameter	Value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL1_IN}	PLL1 input clock	0.92	1	2.1	MHz
	PLL1 input clock duty cycle	40	-	60	%
f_{PLL1_OUT}	PLL1 frequency multiplier output clock (V_{DD}=3.3V, T_A=-40~85℃)	24	-	168	MHz
$f_{PLL1\_48\_OUT}$	PLL1 frequency multiplier output 48MHz clock (V_{DD}=3.3V, T_A=-40~85℃)	-	48	75	MHz
t_{LOCK1}	PLL1 phase locking time	60	-	120	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Table 30 PLL2 Characteristics

Symbol	Parameter	Value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL2_IN}	PLL2 input clock	0.92	1	2.1	MHz
	PLL2 input clock duty cycle	40	-	60	%
f_{PLL2_OUT}	PLL2 frequency multiplier output clock (V_{DD}=3.3V, T_A=-40~85℃)	20	-	144	MHz
t_{LOCK1}	PLL phase locking time	82	-	150	μs

5.6 Reset and power management

5.6.1 Test of Embedded Reset and Power Control Module Characteristics

Table 31 Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.68	1.70	1.70	V
		Rising edge	1.71	1.72	1.73	V
V_{BOR1}	Under-voltage threshold level 1	Falling edge	2.19	2.21	2.24	V
		Rising edge	2.27	2.29	2.30	V
V_{BOR2}	Under-voltage threshold level 2	Falling edge	2.49	2.51	2.55	V
		Rising edge	2.56	2.58	2.59	V
V_{BOR3}	Under-voltage threshold level 3	Falling edge	2.81	2.84	2.87	V
		Rising edge	2.89	2.91	2.92	V
$V_{BORhyst}$	BOR hysteresis	-	-	100	-	mV

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{PDRhyst}$	PDR hysteresis	-	-	40.00	50.00	mV
$T_{RSTTEMPO}$	Reset duration	-	0.70	0.95	1.48	ms

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Table 32 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.14	-	2.18	V
		PLS[2:0]=000 (falling edge)	2.03	-	2.10	V
		PLS[2:0]=000 (PVD hysteresis)	80.00	-	120.00	mV
		PLS[2:0]=001 (rising edge)	2.30	-	2.34	V
		PLS[2:0]=001 (falling edge)	2.18	-	2.23	V
		PLS[2:0]=001 (PVD hysteresis)	90.00	-	120.00	mV
		PLS[2:0]=010 (rising edge)	2.44	-	2.48	V
		PLS[2:0]=010 (falling edge)	2.32	-	2.37	V
		PLS[2:0]=010 (PVD hysteresis)	110	-	120	mV
		PLS[2:0]=011 (rising edge)	2.58	-	2.63	V
		PLS[2:0]=011 (falling edge)	2.49	-	2.53	V
		PLS[2:0]=011 (PVD hysteresis)	90	-	100	mV
		PLS[2:0]=100 (rising edge)	2.75	-	2.80	V
		PLS[2:0]=100 (falling edge)	2.64	-	2.68	V
		PLS[2:0]=100 (PVD hysteresis)	110	-	120	mV
		PLS[2:0]=101 (rising edge)	2.91	-	2.97	V
		PLS[2:0]=101 (falling edge)	2.81	-	2.86	V
		PLS[2:0]=101 (PVD hysteresis)	100	-	110	mV
		PLS[2:0]=110 (rising edge)	3.02	-	3.08	V
		PLS[2:0]=110 (falling edge)	2.90	-	2.96	V
		PLS[2:0]=110 (PVD hysteresis)	110	-	120	m.V
		PLS[2:0]=111 (rising edge)	3.12	-	3.19	V
		PLS[2:0]=111 (falling edge)	3.00	-	3.07	V
		PLS[2:0]=111 (PVD hysteresis)	110	-	120	mV

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.7 Power consumption

5.7.1 Power consumption test environment

（1） The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

（2） All I/O pins are in analog input mode and are connected to a static level at V_{DD} or V_{SS} (no load)

（3） Unless otherwise specified, all peripherals are disabled

（4） The relationship between Flash wait cycle setting and f_{HCLK}:

- 0~30MHz: 0 wait cycle
- 30~60MHz: 1 wait cycle
- 60~90MHz: 2 wait cycles
- 90~120MHz: 3 wait cycles
- 120~150MHz: 4 wait cycles
- 150~168MHz: 5 wait cycles

（5） When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/4$, $f_{PCLK2}=f_{HCLK}/2$

5.7.2 Power consumption in run mode

Table 33 Power Consumption in Run Mode when the Program is Executed in Flash (ART is turned on)

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=85℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2) , enabling all peripherals (3)	168MHz	751.56	74.73	802.2	81.69
		144MHz	693.94	58.29	745.2	63.69
		120MHz	637.4	49.20	691.1	54.59
		90MHz	780.88	38.07	831.7	43.58
		60MHz	636.86	26.51	689.6	31.83
		30MHz	636.62	14.88	689.4	20.17
		25MHz	115.372	12.18	127.76	17.45
		16MHz	115.418	8.20	127.93	13.36
		8MHz	115.36	4.59	127.77	9.71
		4MHz	115.328	2.81	127.78	7.93
		2MHz	115.36	1.90	127.82	7.05
	HSECLK bypass (2) , disabling all peripherals	168MHz	750.88	31.45	801.4	38.05
		144MHz	692.84	24.49	744.7	29.92
		120MHz	636.82	20.66	691.1	26.09
		90MHz	779.8	16.16	831.9	21.50
		60MHz	636.52	11.31	689.8	16.68
		30MHz	636.4	6.59	690.2	11.88
		25MHz	115.318	5.08	128.66	10.29
		16MHz	115.344	3.58	128.44	8.70
		8MHz	115.358	2.31	127.8	7.39
		4MHz	115.348	1.66	127.84	6.79
		2MHz	115.36	1.36	127.86	6.47

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The external clock is 4MHz; when f_{HCLK}>25MHz, turn on PLL; otherwise, turn off PLL.

(3) When the analog peripherals such as ADC, DAC, HSECLK, LSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

Table 34 Power Consumption in Run Mode when the Program is Executed in Flash (ART is turned off)

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=85℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2) , enabling all peripherals (3)	168MHz	751.66	70.94	802	77.84
		144MHz	693.58	56.46	745.3	61.92
		120MHz	637.26	48.65	690.2	54.08
		90MHz	780.86	38.67	831.4	44.23
		60MHz	636.78	27.79	689.4	33.15
		30MHz	636.66	16.03	689	21.51
		25MHz	115.362	13.24	127.72	18.66
		16MHz	115.362	8.88	127.75	14.04
		8MHz	115.35	4.96	127.8	10.16
		4MHz	115.35	2.96	127.88	8.11
		2MHz	115.362	1.99	127.76	7.17
	HSECLK bypass (2) , disabling all peripherals	168MHz	750.94	27.45	801.4	34.20
		144MHz	692.82	22.50	744.7	27.96
		120MHz	636.76	20.02	689.8	25.46
		90MHz	780.46	16.80	831.6	22.27
		60MHz	636.46	12.57	689.8	18.00
		30MHz	636.38	7.73	689.9	13.11
		25MHz	115.33	6.05	128.5	11.43
		16MHz	115.32	4.28	127.96	9.57
		8MHz	115.364	2.62	127.82	7.74
		4MHz	115.35	1.84	127.68	6.99
		2MHz	115.532	1.44	127.9	6.66

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The external clock is 4MHz; when f_{HCLK}>25MHz, turn on PLL; otherwise, turn off PLL.

(3) When the analog peripherals such as ADC, DAC, HSECLK, LSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

Table 35 Power Consumption in Run Mode when the Program is Executed in RAM

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=85℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2) , enabling all peripherals (3)	168MHz	752.14	77.58	803.8	76.51
		144MHz	693.74	60.47	745.5	84.43
		120MHz	637.6	51.11	690.4	65.97
		90MHz	781	39.50	832	56.5
		60MHz	637.02	27.43	689.8	44.85
		30MHz	636.74	15.38	689.2	32.87
		25MHz	115.42	12.62	127.85	20.72
		16MHz	115.374	8.43	127.88	17.89
		8MHz	115.37	4.72	127.81	13.69
		4MHz	115.376	2.89	127.72	9.98
		2MHz	115.347	1.95	127.76	8.10
	HSECLK bypass (2) , disabling all peripherals	168MHz	751.38	34.40	802.4	7.16
		144MHz	693	26.79	744.7	41.28
		120MHz	636.88	22.60	689.8	32.28
		90MHz	780.56	17.66	931.6	28.01
		60MHz	636.68	12.28	690	23.08
		30MHz	636.62	7.07	689.7	17.65
		25MHz	115.364	5.49	128.42	12.39
		16MHz	115.348	3.85	128.79	10.69
		8MHz	115.378	2.43	127.76	9.14
		4MHz	115.364	1.73	127.73	7.64
		2MHz	115.34	1.39	127.74	6.90

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The external clock is 4MHz, and when f_{HCLK}>25MHz, turn on PLL, otherwise, turn off PLL.

(3) When the analog peripherals such as ADC, DAC, HSECLK, LSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

5.7.3 Power consumption in sleep mode

Table 36 Power Consumption in Sleep Mode when the Program is Executed in Flash (ART is turned off)

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=85℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in sleep mode	HSECLK bypass (2), enabling all peripherals	168MHz	751.34	59.86	802.1	66.63
		144MHz	693.26	46.74	745	52.10
		120MHz	637.24	39.59	689.8	44.85
		90MHz	780.6	30.72	831.2	36.06
		60MHz	636.72	21.53	689.2	26.83
		30MHz	636.46	12.39	689.2	17.64
		25MHz	115.356	10.12	127.77	15.33
		16MHz	115.34	6.85	127.71	12.01
		8MHz	115.334	3.93	127.78	9.08
		4MHz	115.332	2.46	127.84	7.60
		2MHz	115.352	1.74	127.82	6.88
	HSECLK bypass (2) , disabling all peripherals	168MHz	750.52	15.57	801	22.11
		144MHz	692.58	12.17	743.9	17.46
		120MHz	636.46	10.39	689	15.65
		90MHz	780.24	8.45	830.6	13.69
		60MHz	636.42	6.13	689	11.34
		30MHz	636.36	3.98	688.8	9.17
		25MHz	115.374	2.92	127.84	8.05
		16MHz	115.346	2.23	127.74	7.37
		8MHz	115.354	1.62	127.83	6.77
		4MHz	115.36	1.32	127.86	6.46
		2MHz	115.422	1.18	127.84	6.35

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The external clock is 4MHz; when f_{HCLK}>25MHz, turn on PLL; otherwise, turn off PLL.

5.7.4 Power consumption in stop mode

Table 37 Power Consumption in Stop Mode

Conditions		Typical value [1], (T_A=25℃)						Maximum value [1], (V_{DD}=3.6V)	
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=85℃	
		I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
The regulator is in run mode, and all oscillators are in off state	Flash is in stop mode, and RC internal oscillator and high-speed oscillator are turned off (with no independent watchdog)	9.28	1.02	9.80	1.03	10.05	1.05	12.36	22.26
	Flash is in power-down mode, and RC internal oscillator and high-speed oscillator are turned off (with no independent watchdog)	9.23	1.02	9.72	1.03	10	1.03	12.35	22.26
The regulator is in low-power mode, and all oscillators are in off state	Flash is in stop mode, and RC internal oscillator and high-speed oscillator are turned off (with no independent watchdog)	4.18	0.50	4.65	0.50	4.87	0.50	5.91	16.76
	Flash is in power-down mode, and RC internal oscillator and high-speed oscillator are turned off (with no independent watchdog)	4.19	0.48	4.64	0.48	4.86	0.48	5.86	16.76

Note: It is tested in comprehensive evaluation instead of in production.

5.7.5 Power consumption in standby mode

Table 38 Power Consumption in Standby Mode

Conditions		Typical value [1], (T_A=25℃)						Maximum value [1], (V_{DD}=3.6V)	
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=85℃	
		I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
Power supply current in standby mode	The backup SRAM is turned on, and the low-speed oscillator and RTC are turned on	2.15	9.48	2.56	10.97	2.83	11.47	3.76	65.59
	The backup SRAM is turned off, and the low-speed oscillator and RTC are turned on	2.15	4.14	2.62	5.17	2.81	5.89	3.48	35.46

Conditions		Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)	
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=85℃	
		I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
	The backup SRAM is turned on, and the RTC is turned off	2.13	8.33	2.62	9.33	2.81	9.77	3.45	64.33
	The backup SRAM is turned off, and the RTC is turned off	2.13	3.03	2.61	3.91	2.78	4.31	3.45	21.38

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.7.6 Peripheral power consumption

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 39 Peripheral Power Consumption

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
		168MHz	
AHB1 (up to 168MHz)	DMA1	5.4	μA/MHz
	DMA2	5.56	
	ETH	3	
	OTG_HS	4.21	
	GPIOA	0.32	
	GPIOB	0.31	
	GPIOC	0.32	
	GPIOD	0.3	
	GPIOE	0.31	
	GPIOH	0.3	
	CRC	0.03	
	BAKPR	0.07	
AHB2 (up to 168MHz)	OTG_FS	3.12	
	DCI	0.79	
	RNG	0.16	
	HASH	1.3	
	CRYP	0.25	
AHB3 (up to 168MHz)	SMC	1.68	
APB1 (up to 42MHz)	TMR2	0.46	

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
		168MHz	
	TMR3	0.35	
	TMR4	0.34	
	TMR5	0.46	
	TMR6	0.08	
	TMR7	0.08	
	TMR12	0.19	
	TMR13	0.14	
	TMR14	0.14	
	WWDT	0.02	
	SPI2/I2S2	0.12	
	SPI3/I2S3	0.12	
	USART2	0.11	
	USART3	0.12	
	UART4	0.11	
	UART5	0.11	
	I2C1	0.12	
	I2C2	0.12	
	I2C3	0.12	
	CAN1	0.18	
	CAN2	0.16	
	PMU	0.01	
	DAC	0.08	
APB2 (up to 84MHz)	SDIO	0.41	
	TMR1	0.99	
	TMR8	0.97	
	TMR9	0.41	
	TMR10	0.27	
	TMR11	0.26	
	ADC1	0.27	
	ADC2	0.27	
	ADC3	0.28	
	SPI1	0.12	

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
		168MHz	
	USART1	0.22	
	USART6	0.21	
	SYSCFG	0.05	
SDRAM		300	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.7.7 Backup Domain Power Consumption

Table 40 V_{BAT} Power Consumption

Symbol	Parameter	Conditions	Typical value (1), T_A=25℃		Maximum value (1), V_{BAT}=3.6V	Unit
			V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=85℃	
I_{DD_VBAT}	LSECLK and RTC are in ON state	The backup SRAM is turned on, and the low-speed oscillator and RTC are turned on	2.35	2.75	6.86	μA
		The backup SRAM is turned off, and the low-speed oscillator and RTC are turned on	1.45	1.82	3.56	
		The backup SRAM is turned on, and the RTC is turned off	1.28	1.49	5.76	
		The backup SRAM is turned off, and the RTC is turned off	0.29	0.40	2.46	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.8 Wake-up time in low-power mode

The measurement of wake-up time in low-power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 41 Wake-up Time in Low-power Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up from sleep mode	-	39.00	59	61.20	ns
t_{WUSTOP}	Wake up from the stop mode	The regulator is in run mode, and Flash is in stop state	12.51	13.602	14.99	μs
		The regulator is in low-power mode, and Flash is in stop state	15.51	19.552	22.93	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		The regulator is in run mode, and Flash is in deep power-down mode	125.63	133.156	135.16	
		The regulator is in low-power mode, and Flash is in deep power-down mode	133.52	136.956	139.60	
$t_{WUSTDBY}$	Wake up from standby mode	-	173.03	214.056	227.96	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.9 I/O port characteristics

Table 42 DC Characteristics (T_A=-40℃-85℃, V_{DD}=2~3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	STD and STDA I/O	-	-	$0.3V_{DD}$-0.04	V
		5T and 5Tf I/O	-	-	$0.3V_{DD}$	
		Boot0 pin	-	-	$0.1V_{DD}$+0.1	
V_{IH}	High-level input voltage	STD and STDA I/O	$0.45V_{DD}$+0.3	-	-	V
		5T and 5Tf I/O	$0.7V_{DD}$	-	-	
		Boot0 pin	$0.17V_{DD}$+0.7	-	-	
V_{hys}	Schmidt trigger hysteresis	STD, STDA and 5T, 5Tf I/O	10% V_{DD}	-	-	mV
		Boot0 pin	0.1	-	-	
I_{lkg}	Input leakage current	STDA in digital mode, $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	±1	μA
		5T and 5Tf I/O, $V_{DDIOx} \le V_{IN} \le 5V$	-	-	3	
R_{PU}	Weak pull-up equivalent resistance	Except PA10 and PB12, $V_{IN}=V_{SS}$	30	40	50	kΩ
		PA10 and PB12	7	10	14	
R_{PD}	Weak pull-down equivalent resistance	Except PA10 and PB12, $V_{IN}=V_{DD}$	30	40	50	
		PA10 and PB12	7	10	14	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Table 43 AC Characteristics (T_A=25℃)

SPEED[1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency	CL=50pF,V_{DD}＞2.7V	-	4	MHz
			CL=50pF,V_{DD}＞1.8V	-	2	
			CL=10pF,V_{DD}＞2.7V	-	8	

SPEED[1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
			CL=10pF,V_{DD}＞1.8V	-	4	
	$t_{f(IO)out}$/$t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=50 pF,V_{DD}=1.8 V-3.6V	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency	CL=50pF,V_{DD}＞2.7V	-	25	MHz
			CL=50pF,V_{DD}＞1.8V	-	12.5	
			CL=10pF,V_{DD}＞2.7V	-	50	
			CL=10pF,V_{DD}＞1.8V	-	20	
	$t_{f(IO)out}$/$t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	CL=30pF,V_{DD}＞2.7V	-	10	ns
			CL=30pF,V_{DD}＞1.8V	-	20	
			CL=10pF,V_{DD}＞2.7V	-	6	
			CL=10pF,V_{DD}＞1.8V	-	10	
10	$f_{max(IO)out}$	Maximum frequency	CL=30pF,V_{DD}＞2.7V	-	50	MHz
			CL=30pF,V_{DD}＞1.8V	-	25	
			CL=10pF,V_{DD}＞2.7V	-	100	
			CL=10pF,V_{DD}＞1.8V	-	50	
	$t_{f(IO)out}$/$t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	CL=30pF,V_{DD}＞2.7V	-	6	ns
			CL=30pF,V_{DD}＞1.8V	-	10	
			CL=10pF,V_{DD}＞2.7V	-	4	
			CL=10pF,V_{DD}＞1.8V	-	6	
11	$f_{max(IO)out}$	Maximum frequency	CL=30pF,V_{DD}＞2.7V	-	100	MHz
			CL=30pF,V_{DD}＞1.8V	-	50	
			CL=10pF,V_{DD}＞2.7V	-	180	
			CL=10pF,V_{DD}＞1.8V	-	100	
	$t_{f(IO)out}$/$t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	CL=30pF,V_{DD}＞2.7V	-	4	ns
			CL=30pF,V_{DD}＞1.8V	-	6	
			CL=10pF,V_{DD}＞2.7V	-	2.5	
			CL=10pF,V_{DD}＞1.8V	-	4	
-	$t_{EINTIpw}$	Pulse width of external signal detected by EINT controller	-	10	-	

Figure 8 I/O AC Characteristics Definition

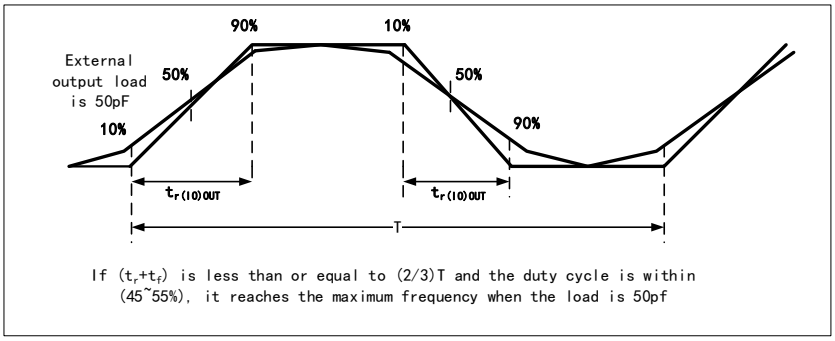


Table 44 Output Drive Voltage Characteristics (T_A=25℃)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	I/O pin outputs low voltage	CMOS port, $\|I_{IO}\|$=8mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}	I/O pin outputs high voltage		V_{DD}-0.4	-	
V_{OL}	I/O pin outputs low voltage	TTL port, $\|I_{IO}\|$=20mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH}	I/O pin outputs high voltage		2.4	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20mA, 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}	I/O pin outputs high voltage		V_{DD}-1.3	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=6mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH}	I/O pin outputs high voltage		V_{DD}-0.4	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.10 NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor RPU.

Table 45 NRST Pin Characteristics (T_A=-40~85℃, V_{DD}=2~3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST low-level input voltage	TTL port, 2.7V≤V_{DD}≤3.6V	-	-	0.8	V
$V_{IH(NRST)}$	NRST high-level input voltage		2	-	-	
$V_{IL(NRST)}$	NRST low-level input voltage	CMOS port, 1.8V≤V_{DD}≤3.6V	-	-	0.3V_{DD}	
$V_{IH(NRST)}$	NRST high-level input voltage		0.7V_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$	NRST input filter pulse	-	-	-	100	ns
$V_{NF(NRST)}$	NRST input unfiltered pulse	V_{DD}＞2.7V	300	-	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{NRST_OUT}	Generated reset pulse duration	Reset internal source	20	-	-	μs

5.11 Communication peripherals

5.11.1 I2C peripheral characteristics

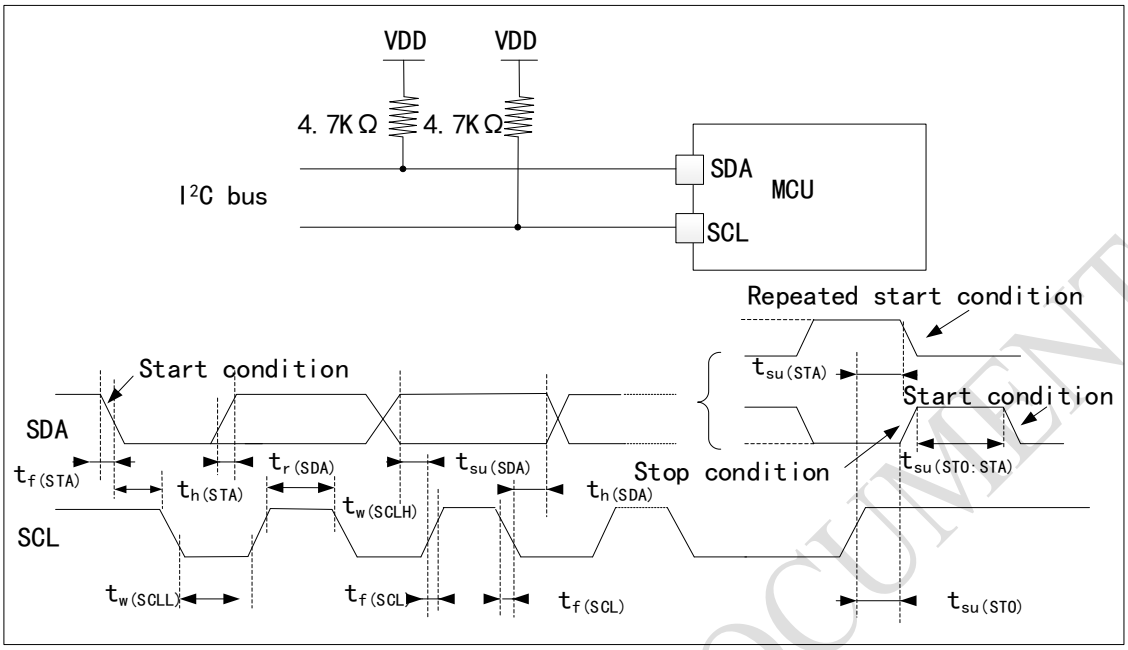
To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

Table 46 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1C_b	300	
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Setup time of repeated start condition	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.0	-	0.6	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (the bus is idle)	4.7	-	1.3	-	
C_b	Capacitive load of each bus	-	400	-	400	pF

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 9 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11.2 SPI peripheral characteristics

Table 47 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	SPI clock frequency	Master mode, SPI1, 2.7V<V_{DD}<3.6V	-	42	MHz
		Slave mode, SPI1, 2.7V<V_{DD}<3.6V	-	42	
$1/t_{c(SCK)}$		Master mode, SPI1/2/3, 1.7V<V_{DD}<3.6V	-	21	
		Slave mode, SPI1/2/3, 1.7V<V_{DD}<3.6V	-	21	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: C=15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4T_{PCLK}$	-	
$t_{h(NSS)}$	NSS hold time	Slave mode	$2T_{PCLK}$ + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK}=36MHz, Prescaler factor=4	$T_{PCLK}/2-2$	$T_{PCLK}/2+1$	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	4	-	
		Slave mode	5	-	

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK}=20MHz	0	$3T_{PCLK}$	
$t_{dis(SO)}$	Disable time of data output	Slave mode	0	18	
$t_{v(SO)}$	Effective time of data output	Slave mode (after enabling the edge)	-	22.5	
$t_{v(MO)}$	Effective time of data output	Master mode (after enabling the edge)	-	6.97	
$t_{h(SO)}$	Data output hold time	Slave mode (after enabling the edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enabling the edge)	1	-	
$DuCy_{(SCK)}$	SPI clock frequency duty cycle	Slave mode	25	75	%

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 10 SPI Timing Diagram - Slave Mode and CPHA=0

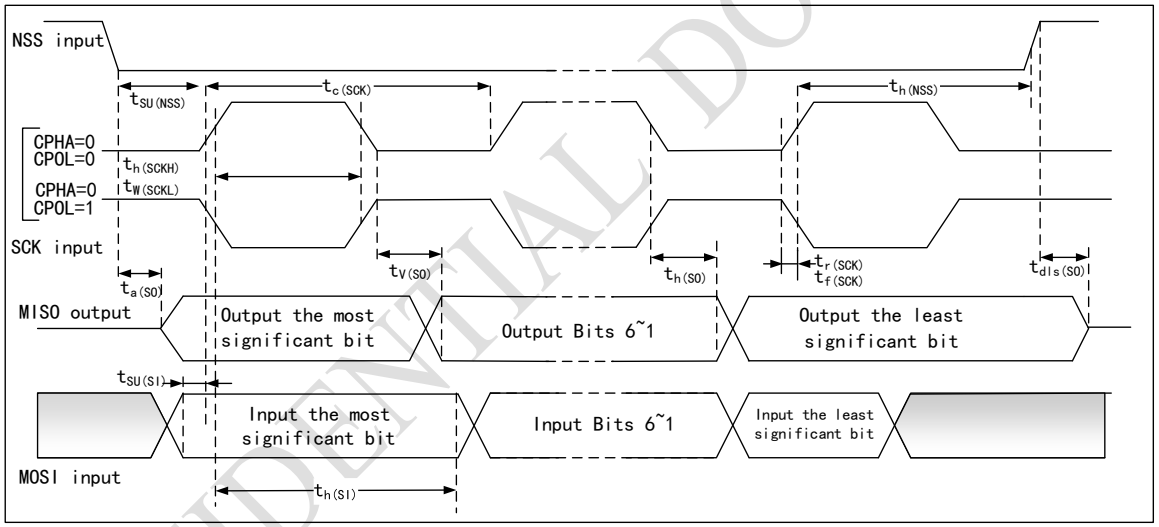
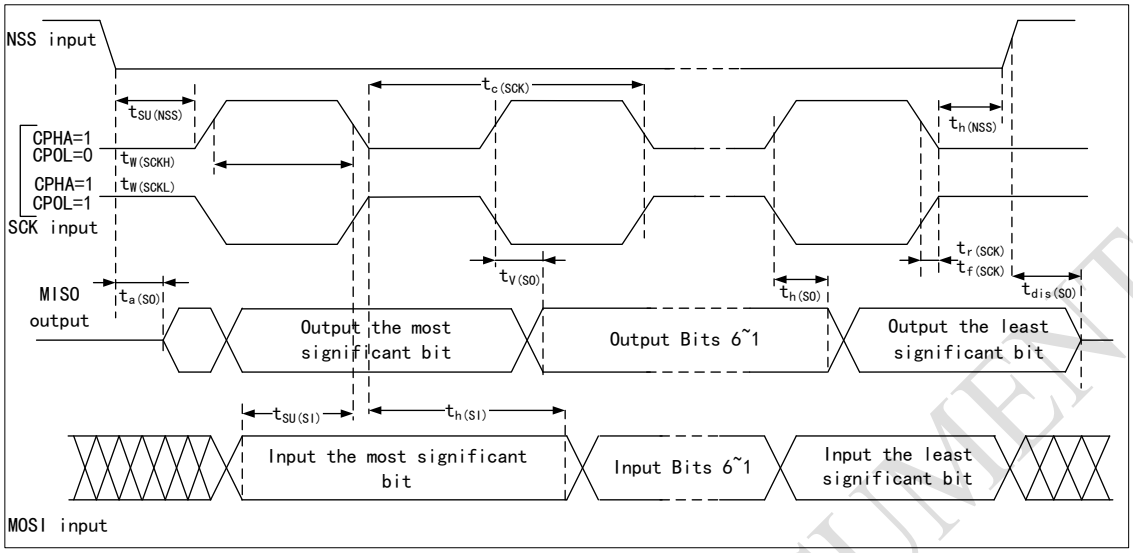
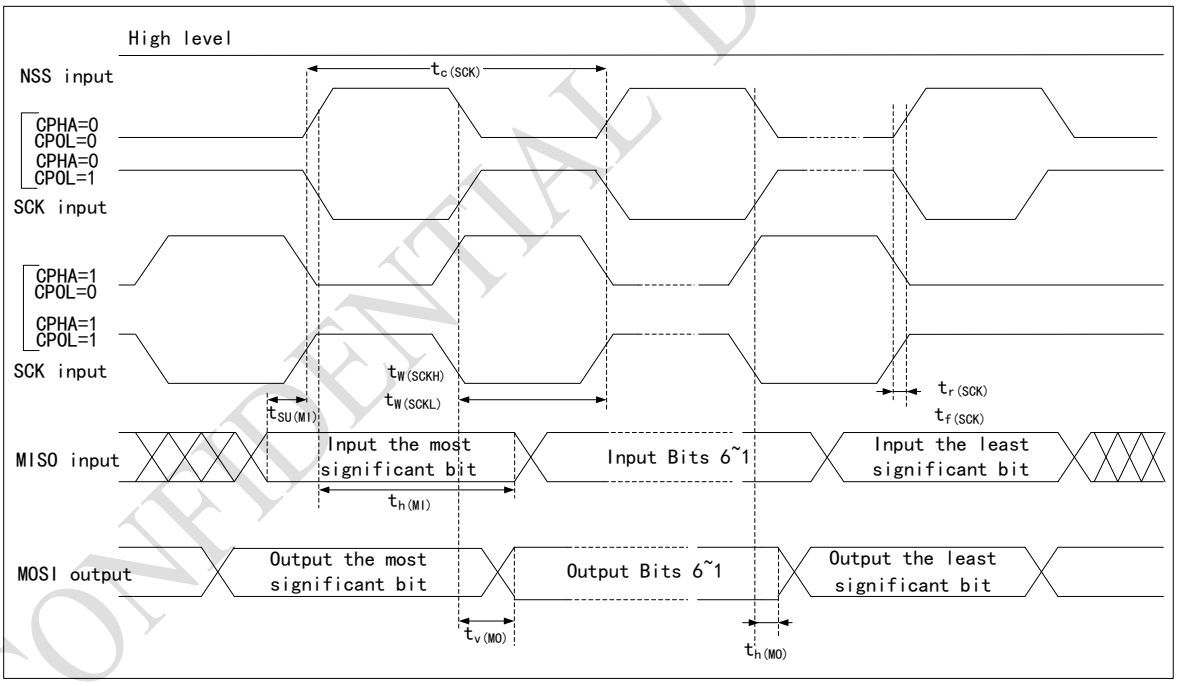


Figure 11 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 12 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.12 Analog peripherals

5.12.1 ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second
- Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.12.1.1 12-bit ADC characteristics

Table 48 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply voltage	-	1.8	-	3.6	V
I_{DDA}	ADC power consumption	-	-	1.6	1.8	mA
f_{ADC}	ADC frequency	V_{DDA}=1.8~2.4V	0.6	15	18	MHz
		V_{DDA}=2.4~3.6V	0.6	30	36	
C_{ADC}	Internal sampling and holding capacitance	-	-	4	-	pF
R_{ADC}	Sampling resistor	-	-	-	6000	Ω
t_S	Sampling time	f_{ADC}=30MHz	0.1		16	μs
		-	3		480	1/f_{ADC}
T_{CONV}	Sampling and conversion time	f_{ADC}=30MHz 12-bit resolution	0.50	-	16.40	μs
		f_{ADC}=30MHz 10-bit resolution	0.43	-	16.34	μs
		f_{ADC}=30MHz 8-bit resolution	0.37	-	16.27	μs
		f_{ADC}=30MHz 6-bit resolution	0.30	-	16.20	μs

Table 49 12-bit ADC Accuracy

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Composite error	f_{PCLK}=56MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~85℃	±2	±5	LSB
E_O	Offset error		±1.5	±2.5	
E_G	Gain error		±1.5	±3	
E_D	Differential linear error		±1	±2	
E_L	Integral linear error		±1.5	±3	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.12.1.2 Test of Built-in Reference Voltage Characteristics

Table 50 Built-in Reference Voltage Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < T_A < +85℃	1.19	1.20	1.20	V
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	10	-	-	μs
V_{RERINT}	Built-in reference voltage extends to temperature range	V_{DD}=3V	-	3	5	mV
T_{coeff}	Temperature coefficient	-	-	30	50	ppm/℃

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.12.2 DAC

Test parameter description:

- DNL differential non-linear error: the deviation between two consecutive codes minus 1LSB
- INL integral non-linear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table 51 DAC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage	-	1.8	-	3.6	V
R_{LOAD}	Resistive load	The buffer is turned on	5	-	-	kΩ
R_O	Output impedance	The resistive load between DAC_OUT and V_{SS} is 1.5MΩ with buffer off	-	-	15	kΩ
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF
DAC_OUT min	Low DAC_OUT voltage with buffer	Maximum output offset of DAC, (0x0E0) corresponding to 12-bit input code to V_{REF+}= (0xF1C) at 3.6V and V_{REF+}= (0x1C7) at 1.8V and (0xE38)	0.2	-	-	V
DAC_OUT max	Higher DAC_OUT voltage with buffer		-	-	V_{DDA}-0.2	V
DAC_OUT min	Low DAC_OUT voltage without buffer	Maximum output offset of DAC	-	0.5	-	mV
DAC_OUT max	Higher DAC_OUT voltage without buffer		-	-	V_{REF+}-1LSB	V
DNL	Differential non-linear error	Configured with 12-bit DAC	-	-	±2	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-	-	±4	LSB
Offset	Offset error	V_{REF+}=3.6V, configuring 12-bit DAC	-	-	±12	LSB

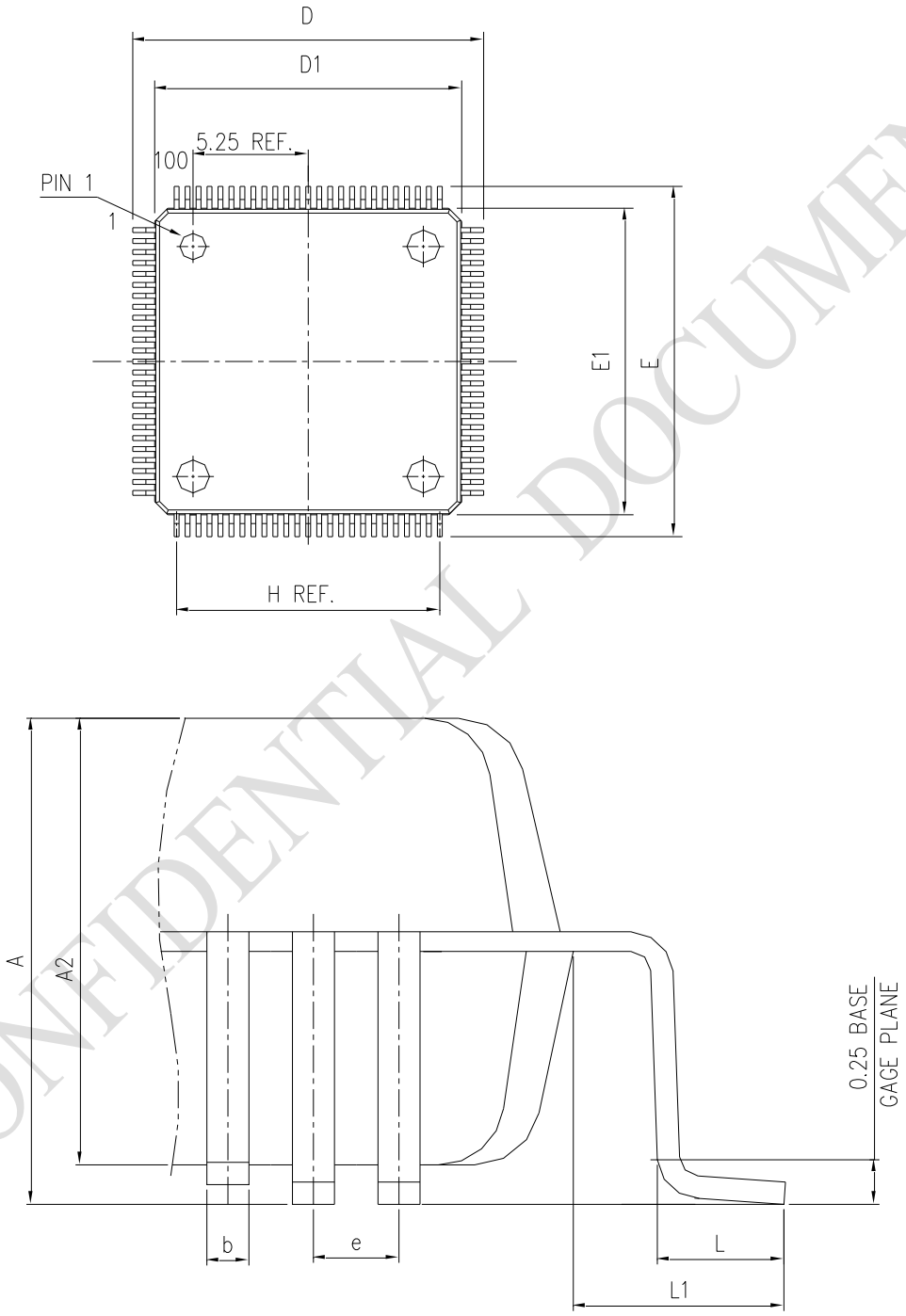
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain error	Gain error	Configured with 12-bit DAC	-	-	±0.5	%

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

6 Package Information

6.1 LQFP100 package information

Figure 13 LQFP100 Package Diagram



（1） The figure is not drawn to scale.

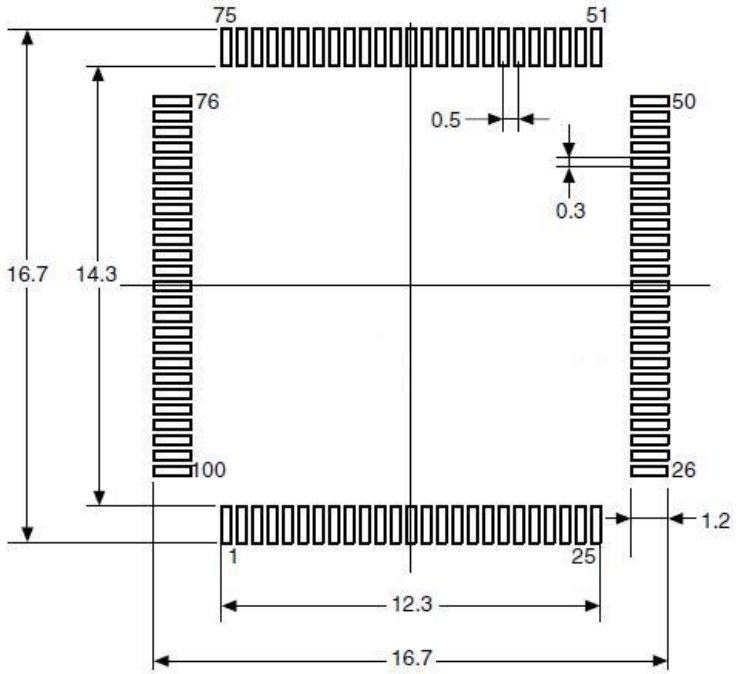
（2） All pins should be soldered to the PCB.

Table 52 LQFP100 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（12.00）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

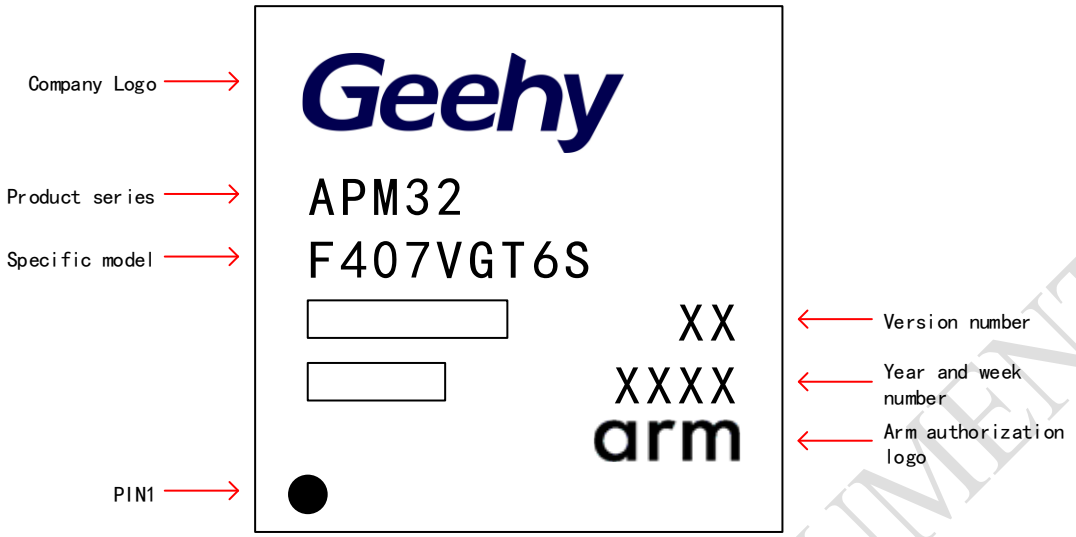
Note: Dimensions are marked in millimeters.

Figure 14 LQFP100 - 100 Pins, 14 x 14mm Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

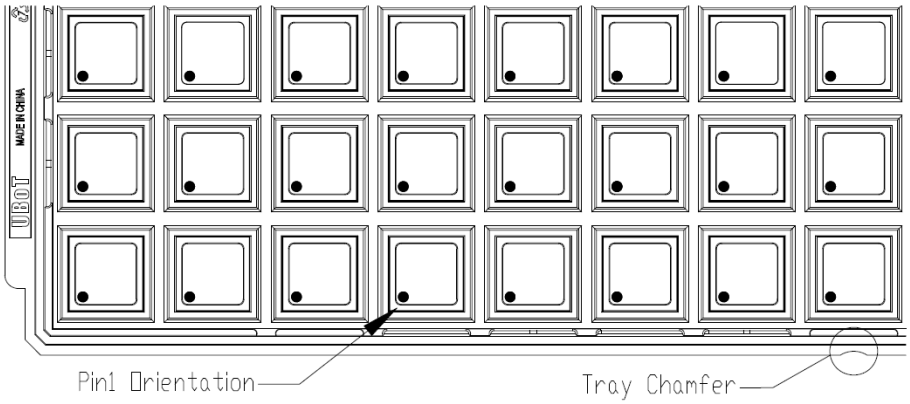
Figure 15 LQFP100 - 100 Pins, 14 x 14mm Package Schematic Diagram



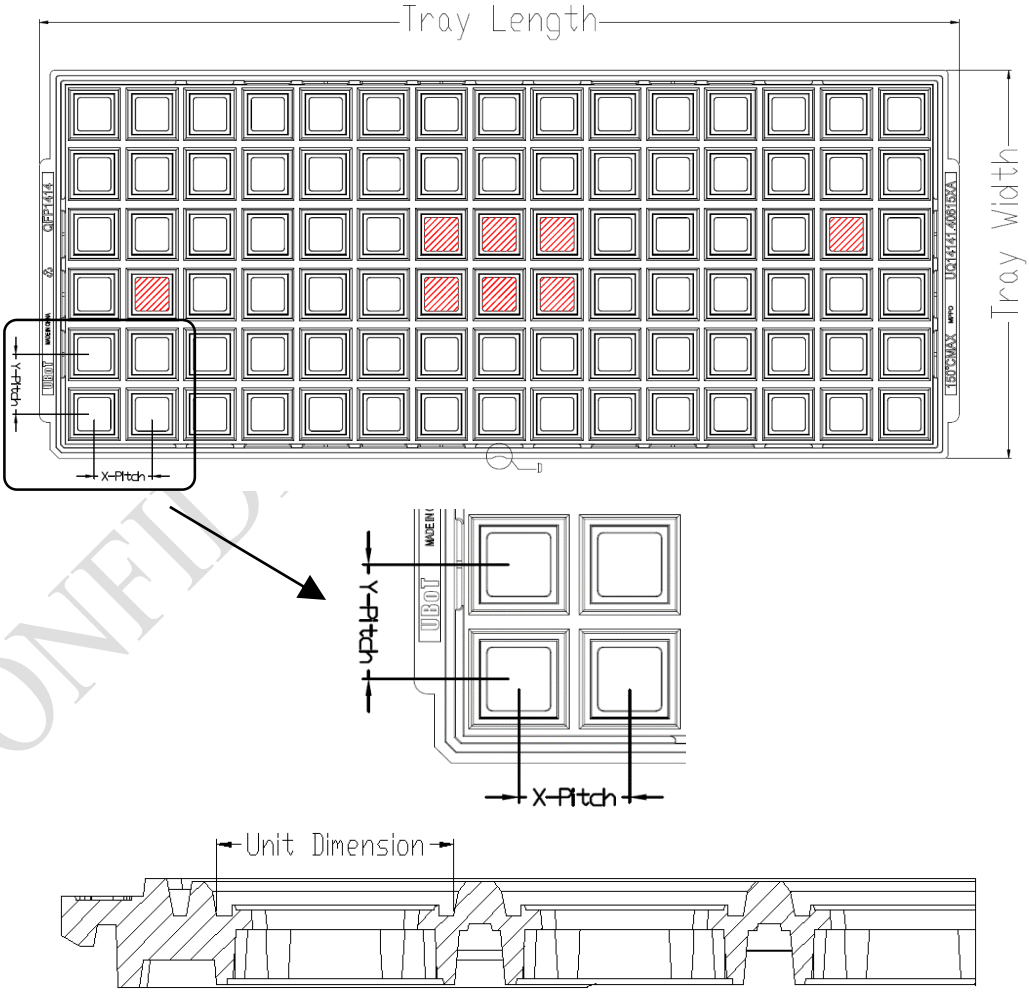
7 Packaging Information

7.1 Tray packaging

Figure 16 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product

Table 53 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension（mm）	Y-Dimension（mm）	X-Pitch（mm）	Y-Pitch（mm）	Tray Length（mm）	Tray Width（mm）
APM32F407VGT6S	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9

8 Ordering Information

Figure 17 APM32F407VGT6S Series Ordering Information Diagram

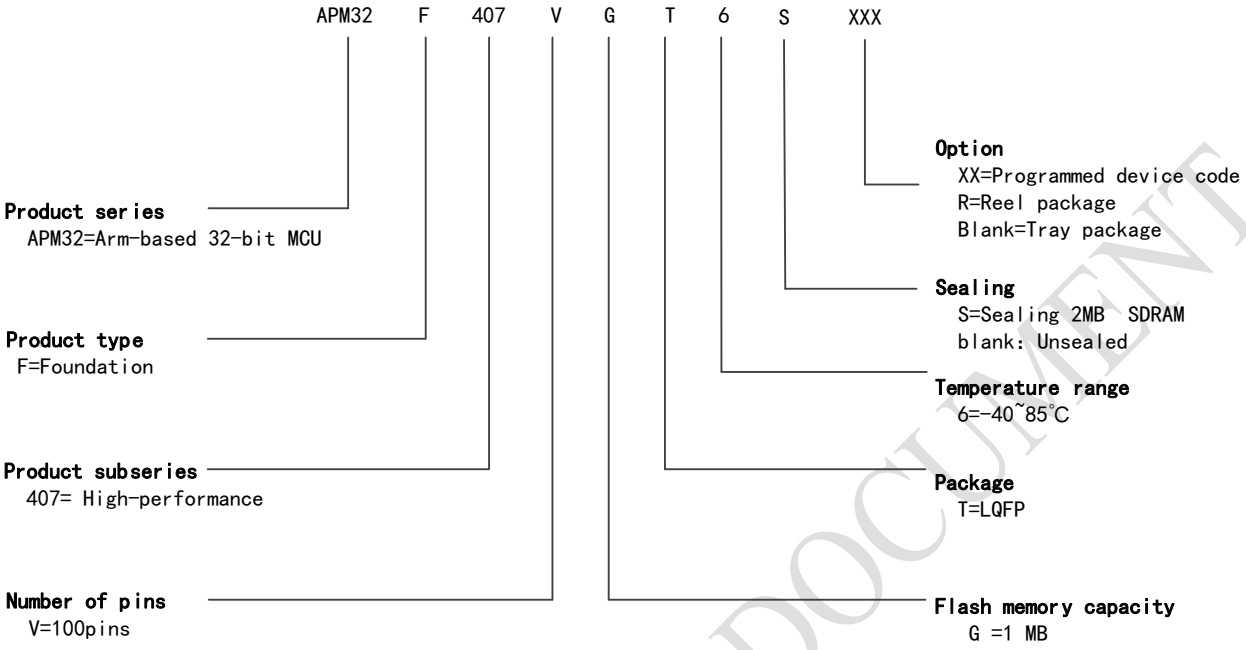


Table 54 Ordering Information Table

Order code	FLASH（KB）	SRAM（KB）	Package	SPQ	Range of temperature
APM32F407VGT6S	1024	192+4	LQFP100	900	-40℃~85℃

9 Commonly Used Function Module Denomination

Table 55 Commonly Used Function Module Denomination

Full name	Abbreviations
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
Static memory controller	SMC
Controller local area network	CAN
I2C Interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC
Secure Digital Input and Output	SDIO
Digital Camera Interface	DCI

10 Version History

Table 56 Document Version History

Date	Version	Change History
2022.8	0.1	NEW
2022.9	0.2	Correction of GPIOB multiplexing function configuration table
2022.10.28	0.3	Modify the pin function description table
2023.4.14	0.4	(1) Modify the PA3 pin description to be compatible with the new version (2) Modify Table 1: APM32F407VGT6S Series Chip Functions and Peripherals
2023.11.9	0.5	(1) Revise the format of Chapter 7 (2) Delete information related to GPIO E/F and add GPIOH multiplexing function configuration (3) Modify Address Mapping (4) Modify the number of maskable interrupt channels (5) Modify TMR9/10/11/12/13/14 counter type (6) Add Ethernet description to product features (7) Modify the I/O structure of PB5 pin and the number of FT input I/Os

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.