ADATA®
INDUSTRIAL

DDR5 SO-DIMM

(Photo for reference only.)

Version 1.1

Jan. 24, 2024

PC5-4800 | 1.1V | CL40

16GB

Revision History

Revision	Date	Description	Editor
1.0	Feb. 15, 2023	Initial release	Alan Peng
1.1	Jan. 24, 2024	Formal release, Add IDD Specification	Alan Peng

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1.0 General Description

AD5S480016G8-BADZ is DDR5-4800(CL40)-39-39 SDRAM memory module. The SPD is programmed to JEDEC standard latency 4800Mbps timing of 40-39-39 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 262pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 262 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

2.0 Key Features

- **Power supply (Normal)**
  - Vin_Bulk = 5V
  - VDD & VDDQ = 1.1V (+0.066V / -0.033V)
  - VPP = 1.8V (+0.108V / -0.054V)
  - VDDSPD = 1.8V (1.7V to 1.98V)
- **1.1V Pseudo open-drain I/O**
- **Burst Length (BL) 16 and 8 with Burst Chop(BC)**
- **Decision feedback equalization (DFE)**
- **32 internal banks; 8 groups of 4 banks each**
- **Tc of 0°C to 95°C**
  - 32ms,8192-cycle refresh at 0°C to 85°C
  - 16ms,8192-cycle refresh at 85°C to 95°C
- **All bank and same bank refresh**
- **Multi-purpose command (MPC)**
- **Loopback mode**
- **Data bus Write CRC**
- **CS/CA training mode**
- **On-die ECC**
- **ZQ Calibration**
- **1N/2N mode support for Commands**
- **Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination(ODT)**
- **JEDEC Standard Compliant.**
- **Serial presence detect hub (SPD Hub) with Integrated temperature sensor**
- **Lead-free and Halogen-free products are RoHS Compliant.**

3.0 Pin Assignment and Descriptions

Table 3-1 Pin Assignment

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VIN_BULK	89	VSS	175	CB3_B	2	HSA	90	VSS	176	CB2_B
3	VIN_BULK	91	DQ30_A	177	VSS	4	HSCL	92	DQ31_A	178	VSS
5	RFU	93	VSS	179	DQ0_B	6	HSDA	94	VSS	180	DQ1_B
7	PWR_GOOD	95	CB0_A	181	VSS	8	PWR_EN	96	CB1_A	182	VSS
9	VSS	97	VSS	183	DQ2_B	10	VSS	98	VSS	184	DQ3_B
11	DQ0_A	99	CB2_A	185	VSS	12	DQ1_A	100	DQS4_A_c	186	VSS
13	VSS	101	VSS	187	DM0_B_n	14	VSS	102	DQS4_A_t	188	DQS0_B_c
15	DQ2_A	103	CB3_A	189	VSS	16	DQ3_A	104	VSS	190	DQS0_B_t
17	VSS	105	VSS	191	DQ4_B	18	VSS	106	CS0_A_n	192	VSS
19	DM0_A_n	107	CA0_A	193	VSS	20	DQS0_A_c	108	ALERT_n	194	DQ5_B
21	VSS	109	CA1_A	195	DQ6_B	22	DQS0_A_t	110	CS1_A_n	196	VSS
23	DQ4_A	111	VSS	197	VSS	24	VSS	112	VSS	198	DQ7_B
25	VSS	113	CA2_A	199	DQ8_B	26	DQ5_A	114	CA3_A	200	VSS
27	DQ6_A	115	CA4_A	201	VSS	28	VSS	116	CA5_A	202	DQ9_B
29	VSS	117	VSS	203	DQ10_B	30	DQ7_A	118	VSS	204	VSS
31	DQ8_A	119	CA6_A	205	VSS	32	VSS	120	CA7_A	206	DQ11_B
33	VSS	121	CA8_A	207	DQS1_B_c	34	DQ09_A	122	CA9_A	208	VSS
35	DQ10_A	123	VSS	209	DQS1_B_t	36	VSS	124	VSS	210	DM1_B_n
37	VSS	125	CA10_A	211	VSS	38	DQ11_A	126	CA11_A	212	VSS
39	DQS1_A_c	KEY		213	DQ12_B	40	VSS	KEY		214	DQ13_B
41	DQS1_A_t	127	CA12_A	215	VSS	42	DM1_A_n	128	RFU	216	VSS
43	VSS	129	VSS	217	DQ14_B	44	VSS	130	VSS	218	DQ15_B
45	DQ12_A	131	CK0_A_t	219	VSS	46	DQ13_A	132	CK1_A_t	220	VSS
47	VSS	133	CK0_A_c	221	DQ16_B	48	VSS	134	CK1_A_c	222	DQ17_B
49	DQ14_A	135	VSS	223	VSS	50	DQ15_A	136	VSS	224	VSS
51	VSS	137	CK0_B_t	225	DQ18_B	52	VSS	138	CK1_B_t	226	DQ19_B
53	DQ16_A	139	CK0_B_c	227	VSS	54	DQ17_A	140	CK1_B_c	228	VSS
55	VSS	141	VSS	229	DM2_B_n	56	VSS	142	VSS	230	DQS2_B_c
57	DQ18_A	143	RFU	231	VSS	58	DQ19_A	144	CA12_B	232	DQS2_B_t
59	VSS	145	CA11_B	233	DQ20_B	60	VSS	146	CA10_B	234	VSS
61	DM2_A_n	147	VSS	235	VSS	62	DQS2_A_c	148	VSS	236	DQ21_B
63	VSS	149	CA9_B	237	DQ22_B	64	DQS2_A_t	150	CA8_B	238	VSS
65	DQ20_A	151	CA7_B	239	VSS	66	VSS	152	CA6_B	240	DQ23_B
67	VSS	153	VSS	241	DQ24_B	68	DQ21_A	154	VSS	242	VSS
69	DQ22_A	155	CA5_B	243	VSS	70	VSS	156	CA4_B	244	DQ25_B
71	VSS	157	CA3_B	245	DQ26_B	72	DQ23_A	158	CA2_B	246	VSS
73	DQ24_A	159	VSS	247	VSS	74	VSS	160	VSS	248	DQ27_B
75	VSS	161	CS0_B_n	249	DQS3_B_c	76	DQ25_A	162	CA1_B	250	VSS
77	DQ26_A	163	RESET_n	251	DQS3_B_t	78	VSS	164	CA0_B	252	DM3_B_n
79	VSS	165	CS1_B_n	253	VSS	80	DQ27_A	166	VSS	254	VSS
81	DQS3_A_c	167	VSS	255	DQ28_B	82	VSS	168	CB0_B	256	DQ29_B
83	DQS3_A_t	169	DQS4_B_c	257	VSS	84	DM3_A_n	170	VSS	258	VSS
85	VSS	171	DQS4_B_t	259	DQ30_B	86	VSS	172	CB1_B	260	DQ31_B
87	DQ28_A	173	VSS	261	VSS	88	DQ29_A	174	VSS	262	VSS

Table 3-2 Pin Descriptions

Pin Name	Description	Pin Name	Description
CA0_A - CA12_A CA0_B - CA12_B	SDRAM Command/Address bus	HSCL	Side Band bus clock
CS0_A_n - CS1_A_n CS0_B_n - CS1_B_n	SDRAM Chip Select	HSDA	Side Band bus data
DQ0_A - DQ31_A DQ0_B - DQ31_B	DIMM memory data bus	HSA	Side Band bus address
CB0_A - CB3_A CB0_B - CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t - DQS4_A_t DQS0_B_t - DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set DRAMs to a Known State
DQS0_A_c - DQS4_A_c DQS0_B_c - DQS4_B_c	SDRAM data strobes (negative line of differential pair)	VIN_BULK	5 V power input supply
DM0_A_n - DM3_A_n DM0_B_n - DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR_GOOD	Power good indicator
CK0_A_c, CK1_A_c CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
		RFU	Reserved for future use

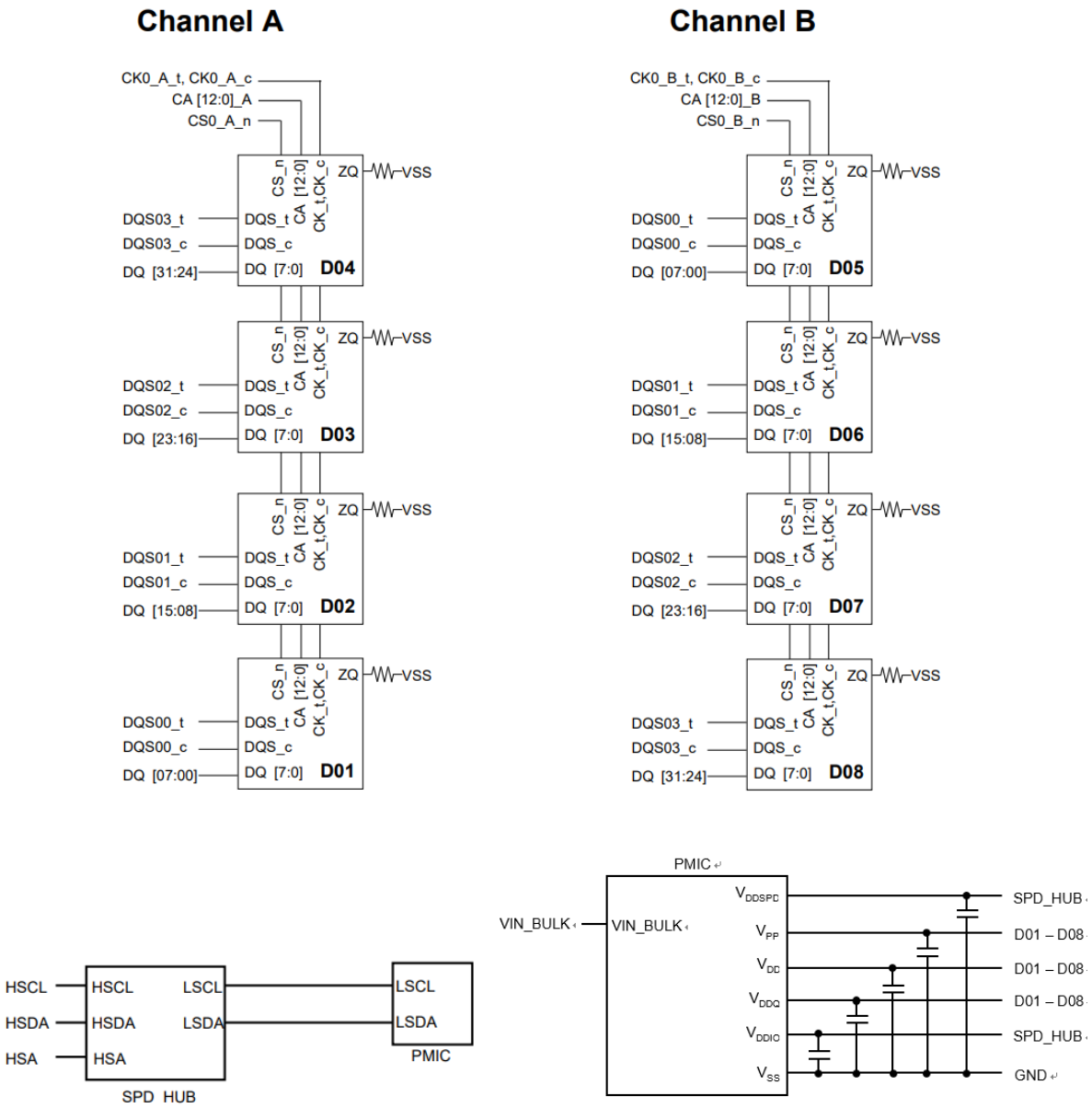
Notes:

DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.

The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B

4.0 Function Block Diagram

Figure 4-1 1Rank, x8 DDR5 SDRAMs



Note : ZQ resistors are 240 Ω ± 1%.

5.0 Absolute Maximum Ratings

Table 5-1 Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit
Voltage on VDD supply relative to Vss	VDD	-0.3 ~ 1.4	V
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 2.1	V
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V
Storage temperature	TSTG	-55 ~ +100	℃

Notes:

DDR5 SDRAM component specification.

6.0 Operation Temperature Condition

Table 6-1 Operation Temperature Condition

Parameter	Symbol	Value	Unit	Note
Normal Operating Temperature Range	TC	0~+85	℃	
Extended Temperature Range (Optional)	TC	+85~+95	℃	1

Notes:

(1) Refresh commands must be doubled in frequency, reducing the refresh interval tREFI to 1.95 μs

7.0 DC Operating Condition

Voltage referenced to Vss=0V,VDD&VDDQ=1.1V(+0.066V/-0.033V),Tc = 0 to 85 ℃

Table 7-1 DC Operating Condition

Parameter	Symbol	Min.	Typ.	Max	Unit	Note
Host Supply Voltage	VIN_BULK	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	VDD	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.746	1.8	1,908	V	3
PMIC Output Supply Voltage	VDDSPD	1.70	1.8	1.98	V	

Notes:

(1) VDD must be within 66mv of VDDQ

(2) AC parameters are measured with VDD and VDDQ tied together.

(3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.

8.0 AC & DC Input Measurement Levels

Overshoot and Undershoot specifications for CAC - No Ballot

9.0 IDD Specification

Table 9-1 VDDQ = VDD = 1.1V(1.067V~1.166V),PC5-4800

Symbol	Condition	16GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	150	mA
IDD0F	Operating Four Bank Active-Precharge Current	240	mA
IDD2N	Precharge Standby Current	117	mA
IDD2P	Precharge Power-Down Current	95	mA
IDD3N	Active standby current	237	mA
IDD3P	Active Power-Down Current	213	mA
IDD4R	Burst Read Current	623	mA
IDD4W	Burst write current	812	mA
IDD5B	Burst Refresh Current (1x REF)	575	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	259	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	119	mA
IDD7	Bank interleave read current	788	mA
IDD8	Maximum power-down current	54	mA

10.0 Timings used for IDD, IPP and IDDQ Measurement

Table 10-1 Timings used for IDD, IPP and IDDQ Measurement

Symbol	DDR5-4400	DDR5-4800	DDR5-5200	DDR5-5600	DDR5-6000	DDR5-6400	Units
Bin(CL-tRCD-tRP)	36-36-36	40-39-39	42-42-42	46-45-45	48-48-48	52-52-52	
Parameter	Min	Min	Min	Min	Min	Min	
tCK	0.454	0.416	0.385	0.357	0.333	0.312	ns
CL	36	40	42	46	48	52	nCK
CWL	36	39	42	45	48	52	nCK
nRCD	36	49	42	45	48	52	nCK
nRC	70	77	83	89	96	102	nCK
nRAS	106	115	125	134	144	153	nCK
nRP	36	39	42	45	48	52	nCK
nRFC 8Gb	430	469	506	546	586	625	nCK
nRFC 16Gb	650	709	766	826	886	946	nCK
nRFC 32Gb	TBD	TBD	TBD	TBD	TBD	TBD	nCK

11.0 Timing Parameters

Table 11-1 Timing Parameters

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Timing									
Clock period average	tCK (AVG)	0.5	<0.500	0.4	<0.454	0.4	<0.416	ns	1
Command and Address Timing									
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	nCK,ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	nCK,ns	
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	–	8	–	8	–	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	–	8	–	8	–	nCK	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2,4,6

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	–	8	–	8	–	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	–	8	–	8	–	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 14.545ns)	–	Max(32nCK, 13.333ns)	–	Max(32nCK, 12.307ns)	–	nCK,ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 18.181ns)	–	Max(40nCK, 16.666ns)	–	Max(40nCK, 15.384ns)	–	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	nCK,ns	
Precharge to Precharge command delay	tPPD	2	–	2	–	2	–	nCK	7
Write recovery time	tWR	30	–	30	–	30	–	ns	

Notes:

1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms,

   nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).
3. RBL: Read burst length associated with Read command

   RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

4. WBL: Write burst length associated with Write command

   WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

5. 5 - The following is considered for tRTW equation

   1tCK needs to be added due to tDQS2CK

   Read DQS offset timing can pull in the tRTW timing

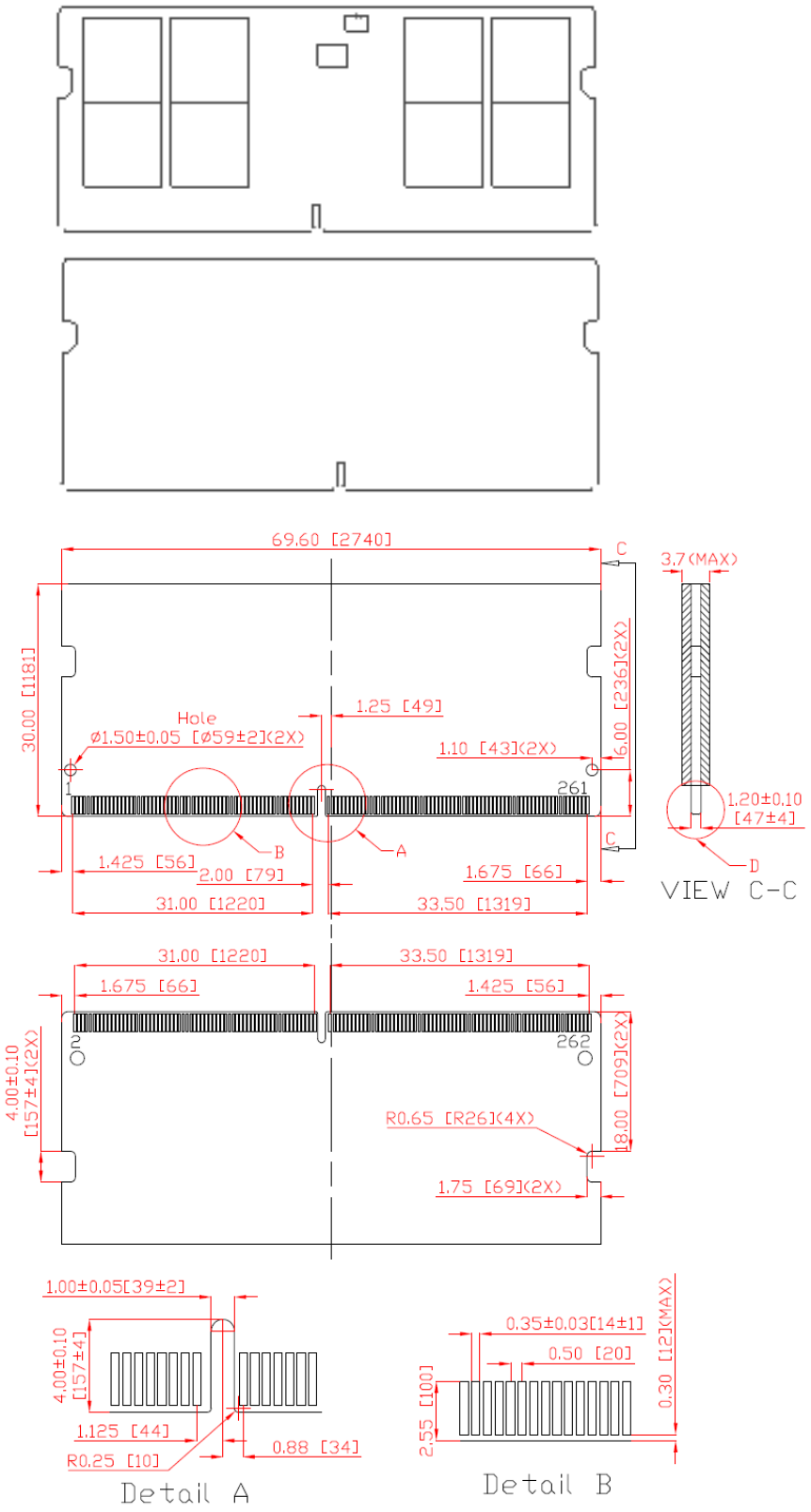
   1tCK needs to be added when 1.5tCK postamble

6. CWL=CL-2

7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

12.0 Physical Dimensions

Figure 12-1 Physical Dimensions



Notes:

All dimensions are in millimeters (mils) and should be kept within a tolerance of ± 0.15(5.91), unless otherwise specified.

13.0 Ordering Information

Figure 13-1 Ordering Information